Watt-Level Ka- and Q-Band MMIC Power Amplifiers Operating at Low Voltages

Youngwoo Kwon, *Member, IEEE*, Kyungjin Kim, Emilio A. Sovero, *Member, IEEE*, and Don S. Deakin

***Abstract*—Ka- and Q-band watt-level monolithic power amplifiers (PA's) operating at a low drain bias of 3.6 V are presented in this paper. Design considerations for low-voltage operation have been carefully studied, with an emphasis on the effect of device models. The deficiency of conventional table-based models for low-voltage operation is identified. A new nonlinear device model, which combines the advantages of conventional analytical models and table-based models, has been developed to circumvent the numerical problems and, thus, to predict optimum load impedance accurately. The model was verified with the load–pull measurements at 39 GHz. To implement a low-voltage 1-W monolithic-microwave integrated-circuit amplifier, careful circuit design has been performed using this model. A Q-band two-stage amplifier showed 1-W output power with a high power gain of 15 dB at 3.6-V drain bias. The peak power-added efficiency (PAE) was 28.5% and 1-dB compression power ($P_{1\,\mathrm{dB}}$) was 29.7 dBm. A Ka-band two-stage amplifier showed a $P_{1\,\mathrm{dB}}$ of 30 dBm with 24.5-dB associated gain and 32.5% PAE. Under very low dc power conditions ($P_{\mathrm{dc}} < 2$ W, $V_{\mathrm{ds}} = 3.4$ V), the amplifiers showed 29-dBm output power and PAE close to 36%, demonstrating ultimate low-power operation capability. To the best of our knowledge, this is the first demonstration of watt-level PA's under 3.6-V operation at 26 and 40 GHz. Compared with the published data, this work also represents state-of-the-art performance in terms of power gain, efficiency, and chip size.**

***Index Terms*—HEMT, millimeter-wave, MMIC, power amplifier.**

I. Introduction

A POWER amplifier (PA) is one of the most important components of many microwave systems. Especially for handheld phones utilizing 0.9–2-GHz frequency range, PA's play key roles. The battery lifetime and the overall size of the handsets depend largely on the efficiency of the PA's. Moreover, for modern digital communication systems such as code-division multiple-access (CDMA) schemes, the phone quality depends heavily on the linearity of PA's. The bias voltage is also another crucial parameter for mobile applications. Low dc voltage means small battery size and reduced handset size and weight. However, at the same time, it is theoretically very difficult to optimize the PA's for high-efficiency low-voltage operation and superior linearity. For example, best linearity is normally achieved under class-A operation, which, on the other hand, limits the efficiency. Low-voltage operation also comes at the cost of reduced efficiency and linearity, as will be discussed in detail in Section II. Therefore, successful implementation of linear PA's with high efficiency, and also capable of low-voltage operation requires careful design and optimization efforts.

Over the past few years, emerging commercial wireless applications at millimeter-wave frequency bands have resulted in increased monolithic-microwave integrated-circuit (MMIC) research activities at Ka-band and above. These applications include point-to-point digital radios up to 40 GHz, local multipoint distribution system (LMDS) at Ka-band, and satellite services at Q-band. Major obstacles against the rapid deployment of these millimeter-wave wireless systems had been the lack of cost-effective PA's. Thanks to major development efforts, tremendous improvement has recently been achieved in millimeter-wave MMIC PA's. Komiak *et al.* presented a 4-W Ka-band PA [1]. 0.15-μm power pseudomorphic high electron-mobility transistor (pHEMT) technology produced 25%–31% power-added efficiency (PAE) with 14-dB power gain at 29–31 GHz. Siddiqui *et al.* showed high-efficiency PA's for LMDS applications [2]. A peak PAE of 37% has been demonstrated together with an output power of 32 dBm and a high power density (PD) of 640 mW/mm.

Thus far, millimeter-wave PA research has been focused on improving the output power level, efficiency, and PD. Unlike the cases of low-frequency PA's, little attention has been paid to reducing the operating voltage or to minimizing the chip size for cost effectiveness. However, for commercial mobile applications, low-voltage operation and small die size are as important as any other parameters. On the modeling side, little effort has been exerted to develop adequate nonlinear device models for milllimeter-wave PA's. Some of the amplifiers have been designed using small-signal models together with optimum load data, while others have utilized less sophisticated nonlinear device models.

In this paper, watt-level MMIC PA's operating at 3.6 V have been developed at Ka- and Q-bands through careful circuit design and modeling efforts. A sophisticated nonlinear device model was developed to facilitate low-voltage operation. Design considerations for low-voltage operation are discussed in Section II, followed by the device models in Section III. The circuit design and measured performance are presented in Sections IV and V, respectively.

II. Design Considerations for Low-Voltage Operation

There is an increasing demand for smaller, lighter, and longer-lasting batteries due to the rapid growth of portable wireless applications. Long battery lifetime requires high PAE. Small and

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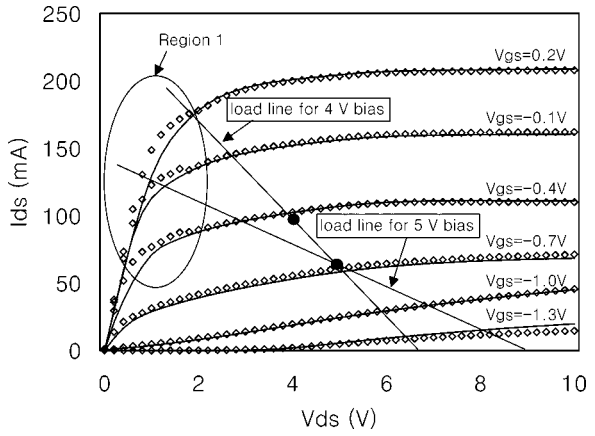


Fig. 1. Calculated microwave current characteristics for 320-μm pHEMT. Points represent the current calculated using the conventional table-based methods, and solid lines are from the modified model presented in Section III. Region 1 is where the conventional models have numerical problems shown in (1). Also shown are two load lines to achieve 0.4-W/mm output power for 4- and 5-V operation.

light batteries mean low-voltage operation. A low-voltage requirement, however, is a big challenge for RF PA designers, especially at millimeter waves. Typical millimeter-wave amplifiers have thus far operated at the drain biases of 4–6 V [3], [4], which is far greater than the dc voltages required by commercial handheld phones at 1–2 GHz. In order for the millimeter-wave PA's to be successfully inserted into millimeter-wave portable applications, it is imperative to limit the bias voltages below 4 V.

The low-voltage requirement of PA's imposes numerous constraints and calls for innovative ideas in device modeling and circuit design. Major difficulties in the circuit design arise from the extremely low impedance levels of the power devices. The output power is determined by the product of voltage swing (ΔV) and current swing (ΔI). As the bias voltage is reduced, the voltage swing decreases. Therefore, the only way to produce the required output power is to increase the dc current level and current swing, which is normally achieved by employing devices with larger gate periphery. Increased device size implies reduced load impedance levels for maximum output power. Matching 50 Ω to such a low impedance is inevitably narrow banded and results in high sensitivity to parameter variations. Proper matching network topology should be devised to alleviate this problem.

Low-voltage operation also comes at the cost of reduced PAE. This point is illustrated in Fig. 1. Fig. 1 shows the microwave current versus voltage relationship of the 320-μm device used in our MMIC design. The microwave current was calculated using the method shown in the following section. Also shown in Fig. 1 are the load lines to achieve 130 mW (0.4 W/mm) for two bias voltages of 5 and 4 V. Class-A operation is assumed for both cases. The peak current is 125 mA for 5-V bias and 190 mA for 4-V bias, producing steeper load lines for 4-V operation. It can be shown from Fig. 1 that the lower limit of drain voltage, defined by the knee voltage, is also higher for 4-V bias, limiting overall voltage swing. The dc power consumption is 312 mW (5 V $\times$ 62.5 mA) for 5 V and 380 mW (4 V $\times$ 95 mA) for 4 V. Thus, the corresponding PAE is 40% for 5 V and 33% for 4 V, showing 7% reduction. In summary, for low-voltage operation, the voltage swing is limited due to higher knee voltage and, therefore, larger current swing together with elevated bias current is required to produce comparable output power, degrading the overall efficiency.

A steep load line for low-voltage operation also calls for careful modeling efforts. The device stays at the low $V_{\rm ds}$ and high $I_{\rm ds}$ region (region 1 in Fig. 1) for a significant time during the swing. This means that the device model for low $V_{\rm ds}$ and high $V_{\rm gs}$ biases has to be very accurate for power simulations. It is, however, nontrivial to achieve accurate device models in this bias region due to the difficulties in measurement and parameter extraction. Further complication arises from the questionable validity of the conventional nonlinear device models in this region; local conservation of drain current may not be satisfied to within an acceptable degree of precision in region 1, as will be shown in the following section. Low-voltage operation also makes the conventional load-line techniques for determining the optimum load impedance impractical [5]. Under high-bias voltage, the effect of knee voltage is negligible and a clear-cut load line that maximizes $\Delta V \times \Delta I$ can be easily defined. However, when the bias voltage is forced close to the knee voltage, significant distortion in the current waveform occurs near the knee voltage, making the optimum load line hard to define. Instead, accurate load–pull simulations are needed to predict optimum load. The accuracy of the nonlinear models is again a very important factor for this purpose. The nonlinear device model to circumvent these difficulties is described in Section III.

III. Nonlinear Device Model

Two different nonlinear device models are currently available for microwave computer-aided design (CAD): analytical models [6] and table-based models [7]. Analytical models express I–V and Q–V characteristics using predefined formulas with fitting parameters. Curve fitting is needed to build the complete model. On the other hand, table-based models are directly constructed from the measured data by numerical integration and interpolation. Curve fitting is, in this way, unnecessary. In principle, this model is capable of reproducing the device characteristics with very high accuracy as long as the voltage is within the measurement region. However, the conventional table-based models may give erroneous results or cause ambiguity in I–V characteristics in the low-voltage region (region 1 in Fig. 1) due to the numerical problems, as shown in Fig. 2. Following the method shown in [8], the closed-contour integral [see (1)] has been evaluated for microwave drain current over the entire bias ranges in Fig. 2. The error function indicating departure from ideal conservation law is calculated as

$$\varepsilon(V_{\rm gs},\, V_{\rm ds}) = \left| \oint \vec{\mathcal{F}}(V_{\rm gs},\, V_{\rm ds}) \cdot (\vec{V_{\rm gs}}\, dV_{\rm gs} + \vec{V_{\rm ds}}\, dV_{\rm ds}) \right| \quad (1)$$

where integrand $\vec{\mathcal{F}}(V_{\rm gs},\, V_{\rm ds})$ is

$$\vec{\mathcal{F}}(V_{\rm gs},\, V_{\rm ds}) = \vec{V_{\rm gs}} Y_{21}^{\rm real}(V_{\rm gs},\, V_{\rm ds}) + \vec{V_{\rm ds}} Y_{22}^{\rm real}(V_{\rm gs},\, V_{\rm ds}) \quad (2)$$

where $Y^{\rm real}$ is the real part of the measured intrinsic Y-parameter after de-embedding the parasitic elements. The error func-

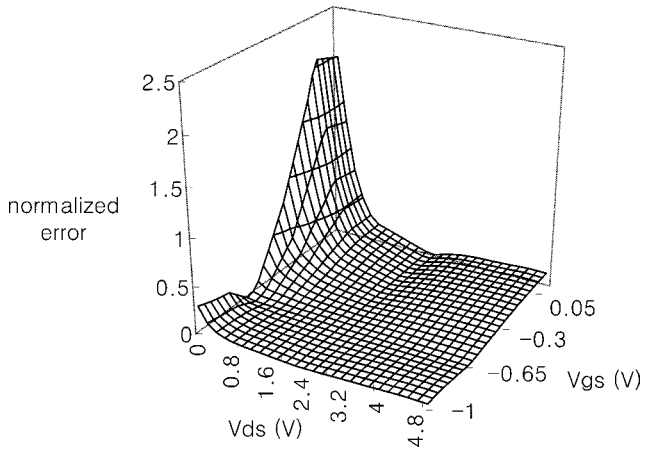


Fig. 2. Three-dimensional plot of error function [see (1)] for two-dimensional gate and drain bias plane, calculated using conventional table-based models.

tion $(\varepsilon(V_{\rm gs},\, V_{\rm ds}))$ is within an acceptable value, except for the drain bias below knee voltage and the gate bias above 0 V (region 1 in Fig. 1), where the error can be more than 50%. This means that the drain current calculated by integrating (2) in this region is not conservative, and depending on the integration paths, different values can be obtained. This may cause significant errors when simulating power performance under low-voltage operation. It is also worthwhile to point out that the table-based models are slower than the analytical models. For simple circuits consisting of a few small transistors, this may not matter much. However, for PA's that involve tens of transistors, the analysis speed is another practical concern. Therefore, a nonlinear device model with high accuracy over the whole bias region and also with high speed is needed for accurate design of millimeter-wave PA's operating at low voltages.

To meet these requirements, a modified table-based model that combines the advantages of both models is developed. Instead of using cubic spline polynomials to interpolate between the measurement points, an analytical formula is used as a fitting function. Furthermore, to circumvent the aforementioned conservation problems at low-$V_{\rm ds}$/high-$I_{\rm ds}$ bias region, fitting is carried out with weighting factors that are determined based on the validity of the data points. In other words, over the bias ranges where error function $(\varepsilon(V_{\rm gs},\, V_{\rm ds}))$ stays under an acceptable value, the microwave current is calculated by integrating (2), and employed for fitting with a full weighting factor. On the other hand, for the bias regions where the current calculated by integration is questionable, the current is determined simply from the analytical I–V formula [shown in (3)]. In this way, numerical problems due to integration could be avoided during harmonic-balance simulation. The current evaluation is also fast since this model is described by analytical formulas with a set of fitting coefficients. Overall analysis speed turns out to improve significantly.

For this model to be numerically stable and highly accurate, it is important to select an analytical I–V formula that is smooth with continuous derivatives, satisfies the conservation relationship, and is capable of predicting higher order derivatives as well as the current data. We have employed the empirical current model developed for fitting dc I–V characteristics by Chen *et al.* [9]. The drain current is expressed as

$$I_{\rm ds}(V_{\rm gs},\, V_{\rm ds}) = (1/I_{\rm max} + 1/I_{\rm ds0})^{-1}. \tag{3}$$

The two individual current terms are

$$I_{\rm max}(V_{\rm ds}) = I_{PK} \cdot \tanh(V_{\rm ds}/V_K) \cdot (1 + \lambda \cdot V_{\rm ds}) \tag{4}$$

$$I_{\rm ds0} = \exp(\psi(V_{\rm gs},\, V_{\rm ds})) \tag{5}$$

where

$$\psi(V_{\rm gs},\, V_{\rm ds}) = \sum_{i=0,\,m} a_i \cdot V_{\rm gs}^i \tag{6}$$

$$a_i(V_{\rm ds}) = \sum_{j=0,\,n} a_{ij} \cdot V_{\rm ds}^j \tag{7}$$

I_{PK}, V_K, λ, and a_{ij}'s are parameters that are determined by fitting to the microwave current data set with weighting factors. This model satisfies the requirements listed above, and yields satisfactory results over the whole measurement bias ranges. This formula also satisfies the following current conservation relationship required for numerical stability.

$$\frac{\partial^2 I_{\rm ds}}{\partial V_{\rm ds}\partial V_{\rm gs}} = \frac{\partial^2 I_{\rm ds}}{\partial V_{\rm gs}\partial V_{\rm ds}}. \tag{8}$$

The I–V curves were extracted for 320-μm devices, and are shown in Fig. 1 together with the microwave current data calculated by conventional table-based method. Good match between the two was found over the entire region, except for region 1, where the fitting was deliberately skipped due to the lack of the data reliability.

The nonlinear terminal charges ($Q_{\rm gs}$, $Q_{\rm ds}$) were also modeled similarly using the modified table-based methods. The fitting formulas for charges were the same form as $I_{\rm ds0}$ in (5). The complete model also includes the dispersion and thermal effect. The dispersion effect has been taken into account by employing a separate current source for dc. Thermal effects have been represented by the decrease in the drain current that is estimated from the power dissipation inside the device. The accuracy of the model has been verified by comparing measured load–pull data with simulation. Fig. 3 shows measured and simulated load pull data of 320-μm power devices under 4-V bias. Load–pull measurements were made on-wafer at 39 GHz using the Hewlett-Packard load–pull measurement setup. The optimum load is indicated by the points and the contours represent 1-dB power backoff. Very good match was found between measurement and simulation. The ultimate test for the nonlinear device models, however, is the comparison between the measured and simulated circuit performances, which will be presented in Section V.

IV. Circuit Design

The PA's were designed using a commercial harmonic-balance simulator. The nonlinear device model described in the previous section was linked to the simulator as a custom library

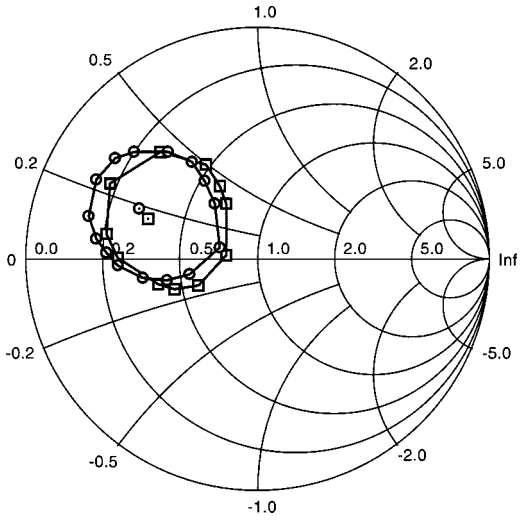


Fig. 3. Simulated and measured load–pull characteristics at 39 GHz. Circular points are for simulation and square points are for measured data. Contours represent load conditions under 1-dB power backoff.

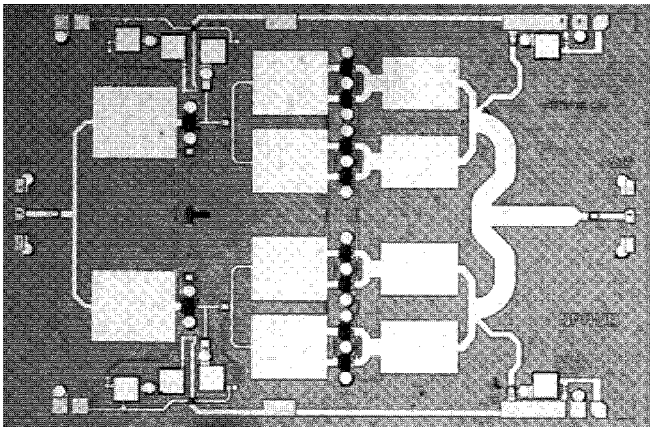


Fig. 4. Photograph of the Q-band MMIC amplifier chip. Chip size is 3.8 mm $\times$ 2.5 mm.

element and employed in the design. Amplifiers were designed at Ka- and Q-bands.

The photograph of the Q-band amplifier is shown in Fig. 4. As a first step, the device size and bias voltages were determined. A low drain bias and high gain approach was taken in this work. Drain bias was fixed at 3.6 V and gate bias was selected to be -0.7 V, which corresponds to class-A/B operation. With the application of 3.6-V drain bias, a small-signal gain higher than 8 dB was possible from each stage. Thus, two stages were enough to achieve more than 15-dB small-signal gain. The gate periphery of the output transistors was chosen on the basis of simulated load–pull results, which showed a PD of 400 mW/mm at 3.6-V bias. For 1-W output power, the output stage was thus composed of eight 320-μm devices. Each device had eight 40-μm-wide gate fingers. Assuming 6-dB power gain for the output stage, 0.25-W output power was needed in the first stage. Two 400-μm devices with eight 50-μm-wide gate fingers were used for this purpose. The resulting interstage ratio was 1 : 3.2. The aggressive interstage ratio helped to improve the efficiency of the amplifier.

The matching circuit was designed in the following order: output, interstage, and input. The output matching network was most important in that it determined the output power and efficiency. The output matching circuit also included the power-combining structures. Power combining can occur either after or before output matching. In the former case, each transistor has its own output matching network and a single final power-combing structure is required for power combining. A large number of matching circuits results in large chip size and makes this approach impractical for monolithic applications. On the contrary, for smaller chip size, all the transistors can be combined first and a single matching network can be employed to provide optimum power match. However, matching in this case may be narrow banded due to extremely low impedance of these massively parallel devices. Besides, the matching circuits may require excessively wide lines, which may run into transverse resonance. In this work, to avoid these extremes, two 320-μm-wide transistors were combined using short transmission lines and odd-mode killing resistors. In the subsequent simulations, this combined structure was treated as a basic building block or unit cell. Thus, the load impedance for optimum output power ($Z_{\rm opt}$) was determined based on the load–pull simulation results of this unit cell. Given $Z_{\rm opt}$, the matching network consisting of three-section transmission lines was designed to transform 50 Ω to $Z_{\rm opt}$. This matching network also serves as power-combining structures. In order to improve the bandwidth, modified three-section quarter-wavelength transmission lines were used for binary power combining and matching. The intermediate impedances were determined to achieve maximum bandwidth using the theory of small reflections [10].

The interstage matching circuit was designed to transform the low input impedance of the output transistors to the optimum load impedance of the first-stage transistors. For stability concerns, parallel feedback consisting of a metal–insulator–metal (MIM) capacitor and a thin-film resistor was employed for the first-stage transistors. The feedback values were chosen to ensure absolute stability while minimizing the effect of gain degradation. The details of the feedback design were presented in [11]. Short-circuited stubs realized with MIM capacitors were employed for interstage matching. This short-circuited stubs also served as a drain bias circuit. In order to suppress the excessive low-frequency gain, a lossy matching structure was also inserted into this bias circuit.

The input matching circuit was designed to transform the low impedance of the first-stage transistor to 50 Ω. In order to improve the matching bandwidth, two-section high/low $\lambda/4$ transmission lines were used. Several measures were taken to prevent unwanted oscillations. The gate bias was applied through the on-chip 20-Ω resistors. Combined with a 5.9-pF on-chip capacitor and 47-pF off-chip capacitor, this damping resistor helped to suppress out-of-band oscillations. For the same reason, the drain bias circuit contained on-chip and off-chip *RC* networks in parallel with 0.7-pF capacitor used for RF ground. The odd-mode oscillations were suppressed by placing thin-film resistors between the transistors. For Q-band design, MIM capacitors were avoided for critical RF matching and used only for dc biasing to minimize sensitivity to process variations. For ease of on-wafer testing, the amplifier was designed to operate with one common

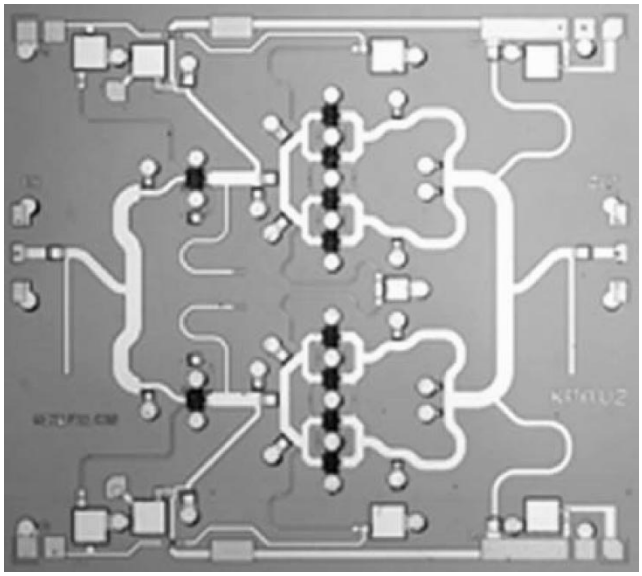


Fig. 5. Photograph of the Ka-band MMIC amplifier chip. Chip size is 2.8 mm $\times$ 2.5 mm.

drain and one common gate bias. In addition, the bias structure was designed to be symmetric so that biasing can be applied from either side of the chip. This feature makes it easier to build high-power modules by paralleling two identical MMIC's. The chip size of the Q-band amplifier was 3.8 mm $\times$ 2.5 mm.

The Ka-band power MMIC was designed using the same design methodology, except for the matching networks. In order to reduce the size of the amplifier and thus chip cost, most of the bulky transmission lines was replaced with the lumped elements, i.e., MIM capacitors. The photograph of the Ka-band PA is shown in Fig. 5. The output and interstage matching was realized with two-pole low-pass structures consisting of microstrip lines and shunt capacitors. An open-ended stub was incorporated in the interstage matching circuit for tuning. Thanks to the lumped-element design, a small chip size of 2.8 mm $\times$ 2.5 mm was possible for Ka-band amplifiers.

V. Measured Results

The MMIC amplifiers were fabricated with a Rockwell power pHEMT process. The starting material was a 4-in wafer with double-modulation-doped structures. The layer structure is shown in Table I. The dual channels were used to improve the power characteristics of the devices. To achieve high breakdown voltage ($\sim$10 V), the gates were double recessed with the final etch done with a selective dry etching [12]. Dry etching improved the uniformity of the devices to better than 5% across the entire wafer, as judged from the threshold voltage variation. The Rockwell International Science Center MMIC process included a 0.2-μm E-beam defined T-gate, microstrip transmission lines, MIM capacitors using PECVD Si_3N_4, evaporated air bridges, and via holes on 75-μm-thick GaAs substrate.

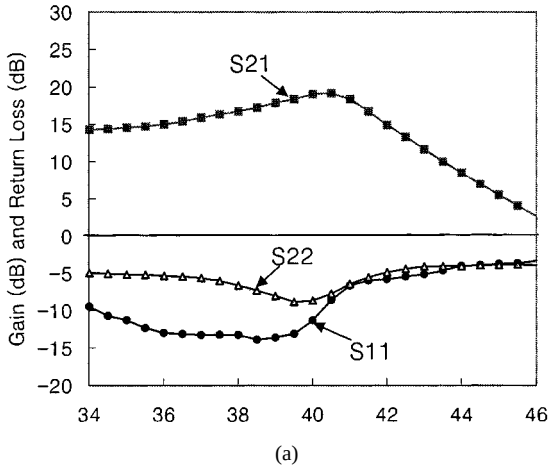
Small-signal characteristics of the amplifiers were tested by on-wafer probing. The bias voltages were set to $V_{\rm gs} = -0.4$ V and $V_{\rm ds} = 3.0$ V for this measurement. A reduced drain bias of

TABLE I
Layer Structure of Double-Doped pHEMT Structures

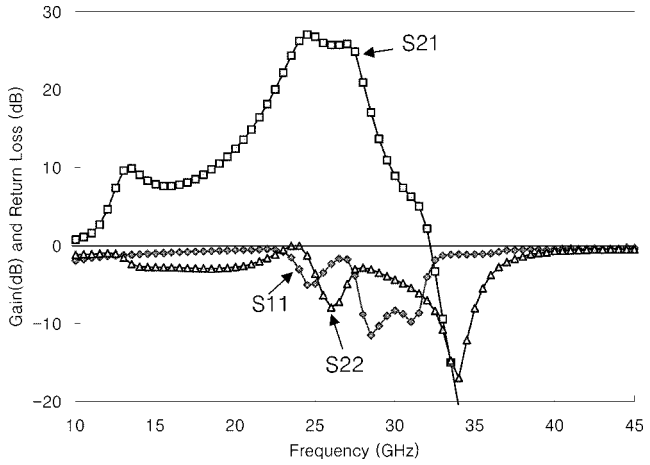
Structure	Dopant
GaAs	N+
Al_xGaAs	N-
Si Pulse Doped	5×10^{12}
Al_xGaAs	--
In_xGaAs	--
Al_xGaAs	--
Si Pulse Doped	1×10^{12}
Al_xGaAs	--
GaAs	--
Superlattice buffer	--
GaAs Substrate	--

3 V instead of the design value of 3.6 V was used for on-wafer testing to avoid thermal stress. Measured small-signal gain and return loss are shown in Fig. 6(a) and (b) for Q- and Ka-band designs, respectively. For Q-band design, gain was higher than 15 dB from 36 to 42 GHz, and showed a peak value of 19 dB at 40 GHz. This gain number translates to 9.5 dB/stage, which is among the highest small-signal gain ever achieved at this frequency from watt-level PA's. The Ka-band amplifier also showed a very high gain of 25 dB from 23.5 to 27.5 GHz. The high gain of the amplifiers is attributed to low-voltage operation as well as optimum feedback and matching circuit design. The low-voltage operation helps to achieve high small-signal gain by utilizing the bias regions where $f_{\rm max}$ is highest; $f_{\rm max}$ shows highest values around 2.5–3.5 V and tends to decrease at high drain biases due to the excessive extension of gate–drain depletion region, and subsequent increase in the effective gate length. The input return loss of the Q-band amplifier was better than 10 dB from 34 to 40.5 GHz. The output return loss was worse than the input return loss by about 5 dB, as expected from the large-signal output matching design.

Power measurement was performed using a waveguide setup employing a traveling-wave tube (TWT) as a power source. The MMIC chip was mounted on a jig using indium solder for efficient heat dissipation. A spectrum analyzer was also used during the power measurement to monitor oscillations. The amplifier was stable under any RF drive conditions. First, the transistor was biased at the designed drain voltage of 3.6 V. Fig. 7(a) and (b) shows the measured output power, PAE, and associated gain ($G_{\rm ass}$) as a function of input power for Q- and Ka-band amplifiers, respectively. For the Q-band amplifier, the output power reached 30 dBm at an input power level of 15 dBm. The associated power gain ($G_{\rm ass}$) was thus 15 dB, which corresponds to the highest power gain (7.5 dB/stage) reported for watt-level PA's at Q-band. The peak PAE was 28.5% at an input power level of 16.5 dBm, which is also among the highest values for 40 GHz PA's. The output power level at 1-dB gain compression ($P_{1\,\rm dB}$: defined with respect to the small-signal gain of 17.5 dB) was 29.7 dBm. The relatively high $P_{1\,\rm dB}$ level compared with the saturation power ($P_{\rm sat} = 30.2$ dBm) is due to the optimum output circuit design based on accurate estimation of optimum load impedance. Fig. 7(a) also shows simulated output power calculated using the nonlinear device models presented in Section III. The measured output power was in excellent agreement

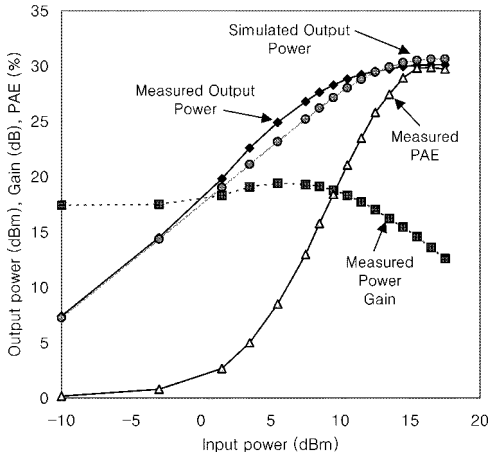


(a)

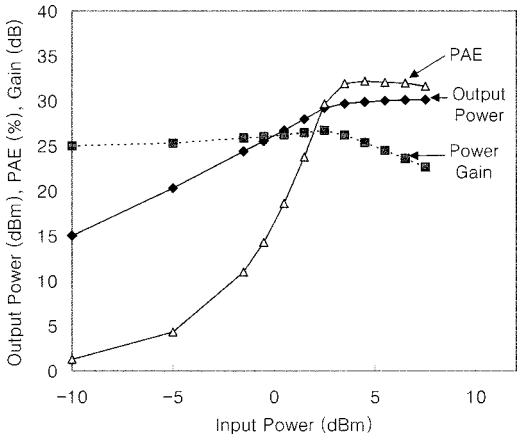


(b)

Fig. 6. Measured small-signal characteristics of: (a) Q- and (b) Ka-band amplifiers. Measurement was made on-wafer at $V_{\rm gs} = -0.4$ V and $V_{\rm ds} = 3$ V.



(a)



(b)

Fig. 7. Measured power characteristics of: (a) Q-band amplifier at 40 GHz and (b) Ka-band amplifier at 26 GHz. The circuits are biased at a drain bias of 3.6 V. Also shown in (a) are simulated output power characteristics represented by circular points. The measured power data are within 1 dBm of the simulation.

(within 1 dBm) with the simulated results, which demonstrates the high accuracy of our device models.

Ka-band amplifiers showed the saturated output power ($P_{\rm sat}$) of 30.2 dBm with 22-dB associated gain, and $P_{1\ \rm dB}$ of 30 dBm with 24.5-dB gain. A peak PAE of 32.5% was achieved at an output power level of 29.8 dBm. Both power gain plots showed overshoot in the medium input power range, which is attributed to the class—A/B design and the optimum large-signal output load design.

In order to explore the ultimate low-power operation capability, the drain-bias voltage was further reduced to 3.4 V, and the drain current was reduced to 0.6 A by pinching the device more. In this way, dc power consumption was limited to 2 W. For Q-band amplifiers, the peak PAE was improved to 36% with a reduced output power of 29 dBm. For Ka-band designs, a PAE higher than 37% was achieved with a similar output power. This measurement shows that decent power performance is still possible with very low dc power consumption.

VI. Summary

In this work, MMIC PA's that deliver over 1 W at a low drain bias of 3.6 V have been developed at 26 and 40 GHz. The low-voltage millimeter-wave PA's have been achieved by developing a sophisticated nonlinear device model, and combining it with optimum circuit design. Design limits for low-voltage operation have been carefully considered and the matching circuit has been designed accordingly. A modified table-based device model that combines the advantages of both analytical and table-based methods has been developed to speed up the simulation, as well as to yield accurate results under low-voltage operation.

TABLE II
COMPARISON OF Q-BAND MMIC PA PERFORMANCE: FREQUENCY OF OPERATION (FREQ.), NUMBER OF STAGES, DRAIN BIAS VOLTAGE, SATURATION POWER ($P_{\rm sat}$), 1-dB COMPRESSION POWER ($P_{1\ \rm dB}$), POWER–ADDED EFFICIENCY (PAE), ASSOCIATED POWER GAIN ($G_{\rm ass}$), POWER DENSITY (PD), AND CHIP SIZE ARE COMPARED FOR VARIOUS Q-BAND MMIC AMPLIFIERS (INCLUDING THIS PAPER)

Ref.	[13]	[14]	[15]	[3]	[4]	This Work
Freq. (GHz)	45	44.5	40	44	43	40
Stage	3	2	2	2	3	2
Bias (V)	5	5	4	5	5	3.6
P_{sat} (dBm)	28.5	30	30	30.2	31.4	30.2
P_{1dB} (dBm)	28	27	27	29.5	-	29.7
PAE (%)	14	15	29.4	30.6	21.5	28.5
G_{ass} (dB)	9.5	7	10	9.2	12.6	15.5
PD (W/mm)	368	347	390	467	410	390
Size (mm^2)	10.14	15	13	11.7	13.76	9.5

Performance of the Q-band amplifier is compared with the published data in Table II. To our knowledge, this is the first demonstration of 1-W MMIC PA's under 3.6-V bias. PAE and $P_{1\,\mathrm{dB}}$ data are also comparable to higher bias design. Thanks to the low-voltage operation, the associated power gain is among the highest ever achieved at 40 GHz. The chip size is also among the smallest for Q-band MMIC designs. This work demonstrates that power pHEMT technology can be successfully extended to produce low-voltage PA's required for millimeter-wave mobile communication systems, provided that careful circuit design methodology and suitable device models are developed.

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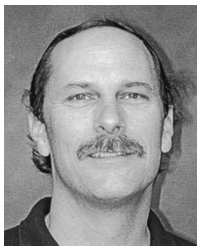

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