Design Optimization and Characterization of High-Gain GaInP/GaAs HBT Distributed Amplifiers for High-Bit-Rate Telecommunication

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***Abstract*—The design methodology, processing technology, and characterization of high-gain GaInP/GaAs heterojunctoin-bipolar-transistor-based distributed amplifiers are described in this paper. Distributed amplifiers with different active cells and number of stages have been compared for high-gain (>12 dB) and high-bandwidth (>25 GHz) performance. Based on the results, a three-stage attenuation-compensated distributed amplifier with a flat gain (S_{21}) of 12.7 dB over a bandwidth of 27.5 GHz was successfully fabricated and tested. Eye-diagram tests at 10 Gb/s show very open eye characteristics with no signal skewing. The amplifier achieves a minimum noise figure of 4 dB at 3 GHz and a sensitivity of −25 dBm for 10-Gb/s nonreturn-to-zero $2^{15}-1$ pseudorandom bit sequence with a bit error rate of 10^{-9}.**

***Index Terms*—Attenuation compensation, bit error rate, distributed amplifiers, HBT.**

I. Introduction

HIGH-SPEED optical communication (≥40 Gb/s) requires ultrawide-bandwidth optical detection, which is usually achieved by means of transimpedance amplifiers in conjunction with a photodiode. The resulting optical receiver should also meet the low-phase jitter requirement of optical systems to support the monolithic integration of clock and data recovery modules that follow the optical detection. Such a requirement can only be met by using heterojunction bipolar transistor (HBT)-distributed amplifiers due to HBT good threshold voltage uniformity and low-phase jitter properties [1], [2]. Traditional amplifier designs fail to meet this requirement due to their limited frequency performance, while high electron-mobility transistor (HEMT)-based or MESFET-based distributed amplifiers have, in principle, smaller threshold voltage uniformity and higher phase jitter.

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InP-based HBT distributed amplifiers have achieved flat gain of 7 dB over a bandwidth of 55 GHz [1], while record performance has been demonstrated from dc up to 100 GHz using InP-based HEMT's [3]. The use of InP-based technology offers the advantage of integration possibility with InGaAs p-i-n diodes and, thus, operation at 1.55-μm wavelength. Employment of GaAs-based technology allows realization of integrated optical receivers for short wavelength (∼0.8 μm) communication. This technology can also be used in conjunction with InGaAs diodes in hybrid form for long wavelength systems. GaAs technology offers the advantage of high throughput, high yield, and process maturity over its InP-based counterpart. Moreover, the lack of integration capability with 1.55-μm photodiodes can be compensated by the significant progress made recently in flip-chip mounting technology [4]. An additional advantage of the hybrid approach is the possibility of the selection of optimum p-i-n photodiode characteristics so that small input power levels and good overall quantum efficiency can be achieved.

First results on the use of GaInP/GaAs HBT technology [5] for the realization of transimpedance [6] and distributed [7] amplifiers were recently presented by the authors. In this paper, we present a methodology to design high-gain HBT distributed amplifiers and demonstrate its validity through experimental results. GaInP/GaAs HBT technology offers several advantages over AlGaAs/GaAs, such as high injection efficiency and very good etching selectivity between GaInP and GaAs. Moreover, the reduced toxicity tertiarybuthyl arsine (TBA), tertiarybuthyl phosphine (TBP) precursors employed in this paper were proven to result in excellent discrete device and integrated-circuit (IC) chip performance as previously reported by the authors [5], [6]. The design of distributed amplifiers with different active cells and various number of stages is presented in Section II. Their performance is also compared on the basis of high-gain (>12 dB) and high-bandwidth (25 GHz) requirements. Based on the results, a three-stage large bandwidth 50-MHz–27-GHz distributed amplifier with a S_{21} gain of 12.7 dB was fabricated. Fabrication and characterization details are presented in Sections III and IV, respectively.

The fabricated circuit has a common-collector cascode active cell designed using attenuation compensation technique [8]. Although, the design does not employ an active load at the input and output transmission lines [2], [9], its low-frequency

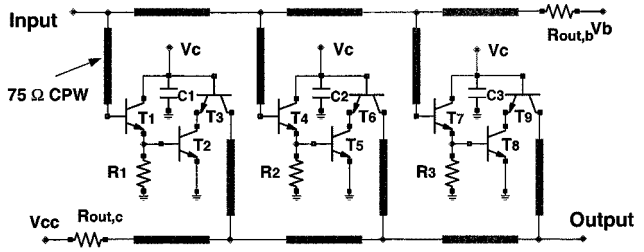

Fig. 1. Circuit schematic of the three-stage GaInP/GaAs HBT distributed amplifier using common-collector cascode scheme (Circuit A).

performance proved to extend to 50 MHz since no capacitor is used for matching the input and output.

II. Design of the GaInP/GaAs Distributed Amplifier

On-wafer probe measurement of discrete $2 \times 30\ \mu\text{m}^2$ HBT's was used to model the device inside the HP-EESOF LIBRA environment. A physical small-signal model was extracted from cold and hot S-parameter measurements [10]. The developed small-signal model was used to design distributed amplifiers with different active cell designs and various number of stages.

Distributed amplifiers using traditional approaches such as common-emitter and cascode active cells were examined first. These designs were found to provide limited values of gain due to the relatively high access resistance of the HBT base and collector terminals. A maximum gain S_{21} of 10 dB with input- and output-matched conditions was achieved with a three-stage cascode-based distributed amplifier. Increasing the number of stages only increased the gain of the amplifiers at low frequencies. The high losses introduced by the HBT input and output series resistances resulted in an overall gain reduction at high frequency (>20 GHz) as the number of stages exceeded four. Therefore, we concluded that such designs are not suitable for high-gain distributed amplifiers and pursued alternative design approaches, as explained in this paper. Reduction of the base and collector access resistances could, however, help to improve the gain-bandwidth characteristics of distributed amplifiers using common-emitter or cascode active cell designs.

The alternative design approach explained in this paper is based on the attenuation compensation technique [8], namely, a common collector stage followed by a cascode transistor pair. Fig. 1 shows a three-stage distributed amplifier based on the "common-collector cascode" active cell approach (Circuit A). This scheme provided high gain and high bandwidth, as described later. No active load was employed at the input and output transmission lines, as reported in [2] and [9]. The common-collector stage (T_1, T_4 or T_7 in Fig. 1) provides at the base and, thus, input coplanar waveguide (CPW) line, a transformation of the capacitive loads C_{BE} seen at the emitter of HBT T_1, T_4, T_7 into a negative resistance for the frequencies of interest. The effective negative resistance compensates the losses due to the loading effect of the CPW line and the other transistors. Resistors R_1 R_2, and R_3 serve as biasing resistors. Our simulation showed that the required gain and bandwidth specifications of $S_{21} > 12$ dB, BW > 25 GHz can be achieved using only three stages of amplification of this design scheme.

Addition of two feedback resistors (R_2 and R_3 and R_5 and R_6 in Fig. 2) to the common-collector cascode active cells improved

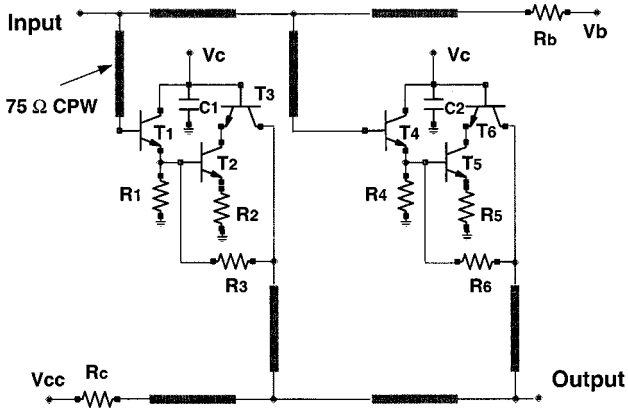

Fig. 2. Circuit schematic of two-stage HBT distributed amplifier using common-collector cascode scheme with additional feedback resistors (Circuit B).

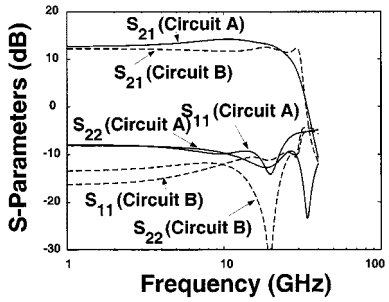

Fig. 3. S-parameter simulation of distributed amplifiers with: (a) three-stage common-collector cascode (Circuit A) and (b) two-stage common-collector cascode with additional feedback resistors (Circuit B).

the overall performance of the circuit in terms of bandwidth (Circuit B, Fig. 2). These resistors were inserted from the collector of output transistors (T_3 and T_6) to the emitter of input transistors (T_1 and T_4) and also in the emitter of T_2 and T_5. Using this approach, it was found that only two stages of amplification are adequate for achieving high-gain and high-bandwidth performance ($S_{21} > 12$ dB, BW > 25 GHz); equivalent performance using Design A necessitates three stages of amplification. The feedback resistors helped to stabilize the gain of individual stages and led to suppression of ripples in the gain-frequency characteristics despite the use of only two stages of amplification.

Fig. 3 shows the simulated S-parameters of the circuits of Fig. 1 (Circuit A) and Fig. 2 (Circuit B) using the HBT small-signal model inside the HP-EESOF LIBRA environment. As the figure indicates, both circuits provide high-gain and high-bandwidth characteristics. The input and output matching of both circuits are better than -8 dB over the operation bandwidth under 50-Ω input and output termination.

Circuit analysis was performed to understand the mechanisms responsible for the features observed in Circuits A and B of Figs. 1 and 2. The input impedance of the transistors of other distributed cells (T_4 and T_7) dominates the losses seen at the input CPW transmission line. The circuit permits compensation of this loss by means of a negative resistance induced at the base terminal of transistor T_1 (Fig. 1). Transistor T_1, being a common-collector stage, transforms the capacitive

load provided by transistor T_2 into a negative resistance, which cancels out the losses seen at the input CPW line. Compensation of losses present in the circuit allows one to obtain higher gain (>12 dB), which cannot be realized using traditional distributed amplifiers employing common-emitter or cascode cells. A distributed amplifier with a cascode active cell could only provide a gain S_{21} of 10 dB over a bandwidth of 25 GHz, while common-emitter-based designs were limited in gain as well as bandwidth ($S_{21} < 8$ dB, BW < 20 GHz). The stability of operation is assured by carefully selecting the length of transmission lines such that the overall stability factor K is always greater than one. The physical mechanisms responsible for this is the transformation of negative resistance through the CPW lines and cancellation of the losses induced by other distributed cells, leading to an overall stable operation.

The gain stage consists of the T_2–T_3 cascode pair. The use of cascode rather than common-emitter gain stage allows a higher bandwidth for each individual stage due to the suppressed Miller capacitance effect in the cascode pair. As a result, a smaller number of stages is required to produce the same overall bandwidth. Another advantage of the cascode configuration is the reduced output transmission-line losses due to the higher output impedance of common-base stage [11]. 75-Ω CPW lines were used to achieve the required phase delay among the active cells and to achieve the necessary inter-stage matching. Use of 75-Ω rather than 50-Ω impedances allowed design of the amplifier with shorter CPW transmission lines, thus reducing the overall size of the circuit. Air-bridge interconnects reduced line moding to ensure pure CPW mode operation.

An analysis of the type-A distributed amplifiers of Fig. 1 showed that the design requirement of minimum gain of 12 dB over a bandwidth of DC-27 could be satisfied with three stages of distributed amplification. The use of a two-stage rather than three-stage distributed amplifier schemes provides smaller gain (10 dB) over a narrower bandwidth of 25 GHz. A larger number of stages (≥4) tends to increase the gain only at lower frequencies. For example, four stages of distributed amplification provide a gain of 15 dB up to 15 GHz, while for frequencies between 15 to 27 GHz, the gain is not affected by the additional stage and remained at about 12 dB. Therefore, the three-stage distributed amplifier design (Circuit A, Fig. 1) was considered an optimum choice and was chosen for implementation. All HBT's were biased at or close to their optimum bias point ($V_{\rm CE} = 3$ V, $I_C = 13$–22 mA). A typical bias condition for the circuit was $V_b = 2.9$ V, $V_c = 4.5$ V, and $V_{\rm cc} = 9$ V, and the dc power consumption was 650 mW.

The input and output lines were matched to $R_{{\rm out},b} = 25\ \Omega$ and $R_{{\rm out},c} = 75\ \Omega$ resistors, respectively. This choice of resistors allowed flat gain characteristics to extend to very low frequencies, as well as suppressed noise components stemming from the resistors due to their small values. The reasonably low values of these resistors did not significantly impact the power consumption of the circuit; base and collector biases were provided through these resistors. Resistors R_1, R_2, and R_3 were used to bias the cascode cells. Bias tuning of independent stages was possible through the terminals denoted by V_c.

Previous demonstrations of HBT distributed amplifiers employed capacitors at the input and output transmission lines to provide the required matching and flat gain conditions. The use of small value resistors enabled circuit design without any capacitor at the input or output transmission lines. Capacitors were only used for high-frequency grounding purposes at the base of common-base transistors T_3, T_6, and T_9 in Fig. 1. Since no capacitors in the signal path were employed in the design, an improved low-frequency performance of the amplifier with a flat gain down to a low frequency of at least 50 MHz was achieved.

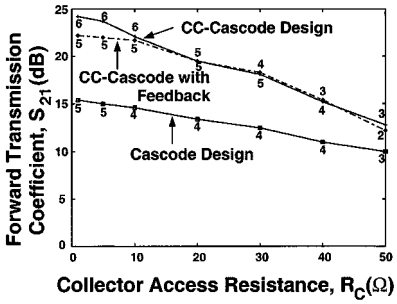

Fig. 4. Effect of collector resistance R_C in the small-signal model on the maximum achievable gain (S_{21}) of distributed amplifiers. Three different distributed-amplifier topologies have been compared. CC-Cascode design denotes that the active cell of each distributed amplifier stage is composed of a common-collector stage followed by a cascode pair (such as Circuit A). CC-Cascode with feedback denotes that two feedback resistors are added to the active cell (such as Circuit B). The number of distributed stages is shown next to each simulation point on the curve.

An analysis of the circuit sensitivity on the magnitude of the collector series resistance (R_C) and base series resistance (R_B) was performed. The overall gain of various distributed amplifiers was simulated for this purpose using LIBRA. Three different distributed amplifier topologies were examined, namely, cascode, common collector followed by cascode (i.e., Circuit A), and common collector followed by cascode with additional feedback resistors (i.e., Circuit B). Each of these topologies can, of course, be used with a different number of stages. Fig. 4 shows the effect of collector termination resistance on the maximum achievable gain (S_{21}) of distributed amplifiers using a variable number of stages of amplification and different topologies. As the collector resistance decreases, the gain of the amplifiers increases monotonically. The gain increase is partly due to the additional number of stages that can be used when the output losses induced by the collector resistance are decreased. Another contributing factor is the resulting improvement in transistor overall gain as the collector resistance is decreased. The common-collector stage followed by a cascode active cell (attenuation compensation stage, CC-Cascode) achieves the highest gain performance. CC-Cascode circuits with two feedback resistors in each active cell (see, e.g., Circuit B in Fig. 2) achieve marginally smaller gain characteristics, while their bandwidth is by at least 20% higher. The improved bandwidth characteristics are due to bandwidth enhancement of individual active stages as feedback is introduced. The gain of a cascode-based distributed amplifier is significantly lower than the other two topologies, especially if the collector resistance value is small.

Fig. 5 shows a comparison of the maximum achievable gain (S_{21}) of the above three topologies as the base series resistance (R_B) is varied. The collector resistance assumed for this study

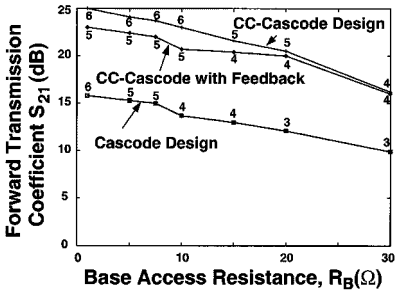

Fig. 5. Effect of base resistance R_B in the small-signal model on the maximum achievable gain (S_{21}) of distributed amplifiers. Three different distributed-amplifier topologies have been compared. CC-Cascode design denotes that the active cell of each distributed amplifier stage is composed of a common-collector stage followed by a cascode pair (such as Circuit A). CC-Cascode with feedback denotes that two feedback resistors are added to the active cell (such as Circuit B). The number of distributed stages is shown close to each simulation point on the curve.

was 10 Ω so that the effect of base resistance on the gain is best seen. A decrease in the base resistance increases the S_{21} gain of all the amplifiers monotonically. Gain increase is achieved by using a larger number of active stages, as well as transistors with higher gain as a result of reduced base resistance.

III. GaInP/GaAs HBT Monolithic-Microwave Integrated-Circuit Technology

The distributed amplifier of Fig. 1 (Circuit A) was fabricated using the GaInP/GaAs HBT technology developed at The University of Michigan at Ann Arbor. GaAs Technology offers the advantage of high throughput, high yield, and process maturity over its InP counterpart. This technology takes advantage of several advanced techniques that have been proven to permit realization of high-performance discrete and integrated HBT circuits of high reliability and yield [5], [6].

The HBT layers were grown using a specially developed hydride and hydrogen-free chemical beam epitaxy (CBE) process with very low defect density ($<$10 def·cm^2). Details of the process have been previously reported by the authors [5]. Self-aligned GaInP/GaAs single HBT's were fabricated on these layers using simple all wet chemical etching, which minimizes layer damage and allows excellent selectivity. Nonalloyed metals were deposited for emitter, base, and collector contacts. A laterally etched undercut (LEU) technology was developed and applied in the base–collector region to reduce the base–collector capacitance by 25% $(C_{\rm BC})$ while avoiding base resistance degradation. The overall maximum oscillation frequency was improved by 20% due to employment of a lateral etch undercut. The associated gain improvement and extension of operation frequency range led to improved gain and bandwidth performance of the amplifier. By way of an example, the gain of the distributed amplifier improved from 11.5 to 12.7 dB and its operation bandwidth increased from 24 to 27.5 GHz when LEU technology was employed. Silicon dioxide was used for passivation. Fig. 6 shows the cross section of a 2-μm emitter HBT fabricated with this technique.

Fabricated 2 $\times$ 30μm^2 HBT's showed a dc gain of 35 and cutoff frequency (f_T) and maximum oscillation frequency $(f_{\rm max})$ of 55 and 65 GHz, respectively. First, reliability tests

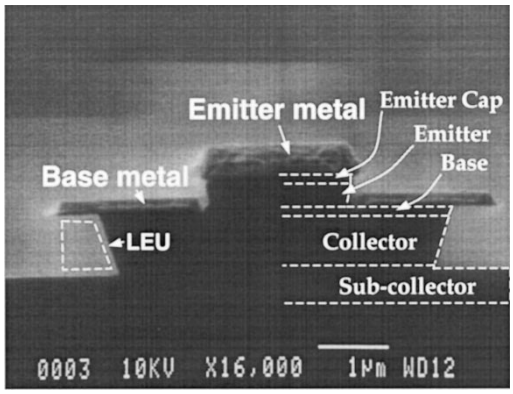

Fig. 6. Cross section of the fabricated self-aligned GaInP/GaAs HBT.

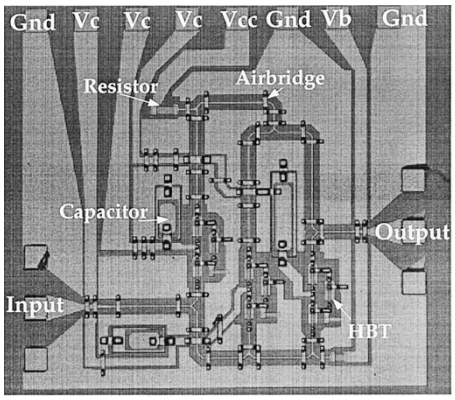

Fig. 7. Photomicrograph of fabricated distributed amplifier of Design A (Fig. 1). The chip size is 1125 $\times$ 1200 μm^2.

performed on the devices revealed only 3% degradation in the current gain over 1000 h of bias and temperature stress ($J_C = 40$ kA/cm^2 and $T_j = 150$°C).

Integrated resistors were realized using 700-Å Ni/Cr thin metal film deposition. Metal–insulator–metal (MIM) monolithic capacitors for high-frequency grounding were fabricated using Al_2O_3. The amplifier chip was connected to the high-frequency test ports via 50-Ω CPW lines. Air-bridge interconnects along the transmission lines reduced line moding, thus supporting pure CPW-mode operation. Fig. 7 shows a photomicrograph of the fabricated distributed amplifier in GaInP/GaAs HBT technology. The chip size was 1125 $\times$ 1200 μm^2.

IV. Distributed Amplifier Characterization

On-wafer testing was used for circuit characterization. The S-parameters of the distributed amplifier were measured from 50 MHz to 40 GHz using an HP8722D network analyzer. Fig. 8 shows the measured S-parameters of the amplifier measured at $V_b = 2.9$ V, $V_c = 4.5$ V, and $V_{\rm cc} = 9$ V. A S_{21} gain of 12.7 dB over a bandwidth of 27.5 GHz was achieved. This corresponds to a 118-GHz gain-bandwidth product, which is among the highest reported values for HBT-based distributed amplifiers, i.e., 107 GHz for an InP-based HBT distributed amplifier [1] and 173 GHz for InP-based transferred-substrate HBT distributed amplifier [12]. Amplifier isolation (S_{12}) ranged from -50 to -12 dB in the operation bandwidth, while input and output matching (S_{11}, S_{22}) ranged from -13 to -3 dB. The

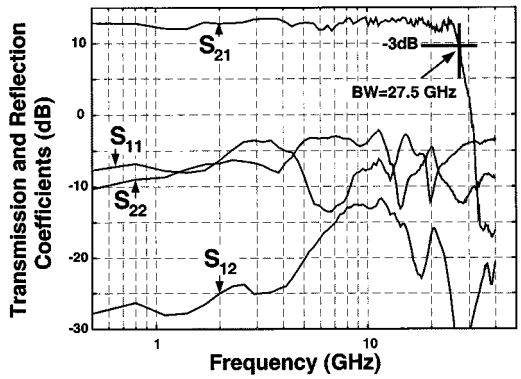

Fig. 8. Measured S-parameters of distributed amplifier (Circuit A, Fig. 1).

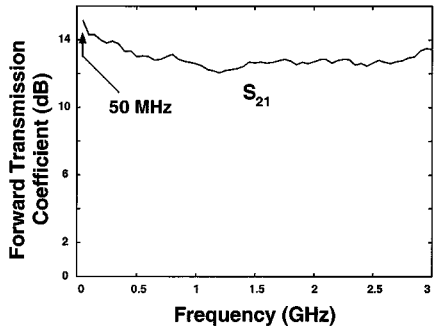

Fig. 9. Forward transmission coefficient S_{21} of distributed amplifier (Circuit A of Fig. 1) measured at low frequencies.

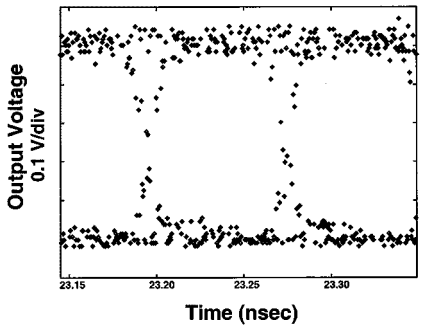

Fig. 10. Measured eye diagram of the distributed amplifier at 10 Gb/s $2^{15}-1$ NRZ PRBS.

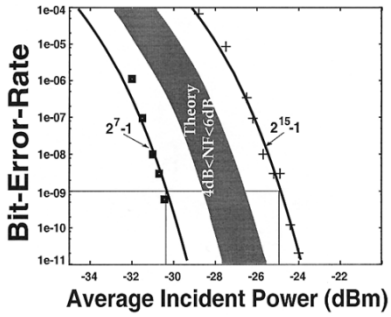

Fig. 11. BER of the amplifier as a function of average incident power measured at 10-Gb/s NRZ PRBS. Different word lengths are used. The theoretical values are calculated based on a constant NF of 6 dB over the measured bandwidth of 10 GHz.

measured input and output reflection coefficients were higher than the simulated parameters ($S_{11}, S_{22} \leq -8$ dB).

Distributed amplifier designs benefit from the presence of an active load at the input and output transmission lines to extend the bandwidth to low frequencies [2], [9] and improve noise performance [13]. The amplifier reported here does not use such active loads, but demonstrates operation capability at low frequency. This is due to the fact that the attenuation compensation scheme employed in these amplifiers allows one to use low termination resistor values $R_{\text{out},b}$ and $R_{\text{out},c}$, while achieving high gain by means of the negative resistance provided by the common-collector transistors. The noise performance of the amplifier also benefits from the use of low input and output matching resistors. Fig. 9 shows details of the forward transmission coefficient (S_{21}) of the amplifier measured in the 50-MHz to 3-GHz range. As can be seen from the figure, the gain does not change significantly at low frequencies.

Eye-diagram tests were performed for the amplifier at 10 Gb/s with a $2^{15}-1$ nonreturn to zero (NRZ) pseudorandom bit sequence (PRBS) using an Anritsu MP1701B pattern generator and a sampling oscilloscope. Fig. 10 shows the measured results, indicating very open-eye characteristics with no signal skewing and very small inter-symbol interference (ISI) and no jitter. Reduced signal skewing and ISI in the eye diagram are attributed to the circuit high bandwidth of operation. It is expected that this circuit perform well up to 40-Gb/s bit rates.

The electrical sensitivity of the amplifier was measured using an Anritsu MP1702A bit error rate (BER) detector. Fig. 11 shows the BER measured at 10-Gb/s NRZ PRBS with two different word lengths. The 2^7-1 word length showed a sensitivity of -33 dBm at 10^{-9} BER while the $2^{15}-1$ word length had a lower sensitivity of -25 dBm. Also shown in the same figure are the calculated BER's of the amplifier as a function of incident power for the two cases. In one case, we assumed that the noise figure (NF) of the amplifier corresponds to a constant value of 4 dB, which is the minimum value of measured high-frequency NF for the amplifier as described below. The other plot shows the BER with a constant NF of 6 dB, which corresponds to the maximum measured NF value in the operating range of the amplifier. In this calculation, the error probability (BER) is found from a complementary error function of signal-to-noise amplitude [14]. As can be seen, the theoretical prediction falls close to measured BER results with a sensitivity of -28.6 and -26.6 dBm at 10^{-9} BER being predicted for NF's of 4 and 6 dB, respectively. The small difference in measured and calculated BER indicates that the amplifier sensitivity is primary dictated by noise and phase jitter plays a minor role on amplifier performance at the high operation speed of 10 Gb/s used for testing.

The sensitivity of the distributed amplifier reported in this paper is among the highest reported figures [15]. The high sensitivity of the amplifier can be attributed to two factors. One is the high bandwidth of operation of the amplifier, which results in very small ISI and, therefore, provides a higher noise margin. The other factor is its low-noise performance.

Fig. 12 shows the results from high-frequency noise tests of the amplifier carried out from 250 MHz to 18 GHz with input

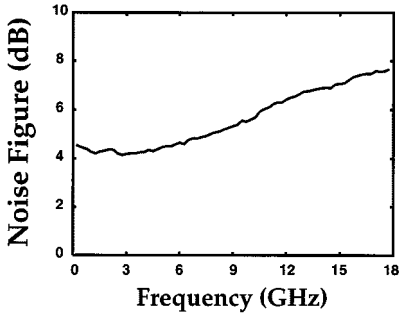

Fig. 12. NF of the distributed amplifier measured between 250 MHz to 18 GHz under source matched to 50-Ω condition.

terminated to 50 Ω. The characteristics measured in these experiments were used to obtain the simulated sensitivity performance reported earlier. An HP8970B/8971B NF test set was used for these tests. Although the termination impedances are not optimized for noise matching, the results reveal a minimum NF of 4 dB at 3 GHz and an NF of about 6 dB at 10 GHz. These values are among the lowest NF's reported for distributed amplifiers [13], [15]. The overall good noise performance of the distributed amplifier employed in this paper is related to the use of low matching resistor values at the input and output transmission lines ($R_{\text{out},b}$ and $R_{\text{out},c}$), which turn out to be close to the impedance conditions necessary for optimum noise performance. Another important parameter influencing the noise performance is the small noise contribution of the transistors themselves due to their low base resistance ($R_B = 2.5\ \Omega$), as indicated by small-signal modeling. The latter was possible due to the high carrier concentration ($\geq 4 \times 10^{19}\text{cm}^{-3}$) obtained in the thin (60 nm) C-doped GaAs base.

V. Conclusion

The design methodology for high-gain high-bandwidth HBT distributed amplifiers has been discussed in this paper. The study suggests that common-emitter or cascode active cell designs are not suitable for high-gain distributed amplifier applications. Design based on a common-collector stage followed by a cascode pair with or without additional feedback resistors (Circuit A, Fig. 1 and Circuit B, Fig. 2) can provide high-gain high-bandwidth performance of $S_{21} > 12$ dB and BW > 25 GHz. The introduction of feedback resistors in Circuit B allows one to reduce the number of stages and improve the bandwidth of the distributed amplifier by at least 20%. The effect of base and collector resistance on the overall gain of the amplifier was also considered.

Based on the performed analysis, a three-stage GaInP/GaAs-based HBT distributed amplifier with a common-collector cascode active cell was designed, fabricated, and successfully tested. A gain of 12.7 dB over a bandwidth of 50 MHz–27.5 GHz was achieved. The amplifier showed very open eye-diagram characteristics and had -25-dBm sensitivity for 10-Gb/s NRZ $2^{15} - 1$ PRBS at a BER of 10^{-9}. High-frequency noise characterization of the amplifier revealed a minimum NF of 4 dB at 3 GHz. These noise tests permitted analysis and confirmation of the sensitivity characteristics of the amplifier.

Acknowledgment

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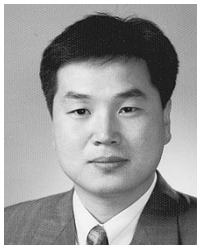

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