High-Isolation CPW MEMS Shunt Switches—Part 1: Modeling

Jeremy B. Muldavin, *Student Member, IEEE,* and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—This paper, the first of two parts, presents an electromagnetic model for membrane microelectromechanical systems (MEMS) shunt switches for microwave/millimeter-wave applications. The up-state capacitance can be accurately modeled using three-dimensional static solvers, and full-wave solvers are used to predict the current distribution and inductance of the switch. The loss in the up-state position is equivalent to the coplanar waveguide line loss and is 0.01–0.02 dB at 10–30 GHz for a 2-μm-thick Au MEMS shunt switch. It is seen that the capacitance, inductance, and series resistance can be accurately extracted from dc-40 GHz S-parameter measurements. It is also shown that dramatic increase in the down-state isolation (20^+ dB) can be achieved with the choice of the correct *LC* series resonant frequency of the switch. In part 2 of this paper, the equivalent capacitor–inductor–resistor model is used in the design of tuned high isolation switches at 10 and 30 GHz.**

***Index Terms*—Low loss, MEMS, micromachining, microwave, millimeter-wave, switches.**

I. Introduction

MICROELECTROMECHANICAL systems (MEMS) electrostatically actuated reflective switches for low-loss microwave and millimeter-wave applications have recently been demonstrated [1]–[4]. MEMS switches are composed of a thin metal membrane (or beam), which can be electrostatically actuated to the RF line using a dc-bias voltage. Two major types of MEMS switches have come to the forefront: the series metal-to-metal contact switches [3] and the shunt-capacitive switches [2]. A shunt-capacitive MEMS switch consists of a thin metal membrane "bridge" suspended over the center conductor of a coplanar waveguide (CPW) or microstrip line and fixed at both ends to the ground conductors of the CPW line [see Fig. 1(a)]. A 1000–2000-Å dielectric layer is used to dc isolate the switch from the CPW center conductor. When the switch (membrane) is up, the switch presents a small shunt capacitance to ground. When the switch is pulled down to the center conductor, the shunt capacitance increases by a factor of 20–100, presenting an RF short.

MEMS shunt switches have several advantages over their p-i-n diode counterpart. The MEMS switch has very little dc power consumption (microjoule during the switching process), allows for large down- to up-state capacitance ratios ($C_d/C_u =$ 20–100), has very low intermodulation products, and can be fabricated on almost any substrate. Several disadvantages include slow switching speeds (2–10 μs), high actuation voltages (15–80 V), and hot switching in high RF power applications (>2 W). These disadvantages may be tolerated in many applications, such as low-loss high-isolation telecommunications switches and radars with relatively low scanning rates.

This paper focuses on the modeling of CPW shunt-capacitive switches. The single switch is first accurately modeled using numerical and experimental techniques, and its equivalent capacitor–inductor–resistor (CLR) model is derived. The CLR model is also extracted from dc–40-GHz measurements and is compared to full-wave simulations.

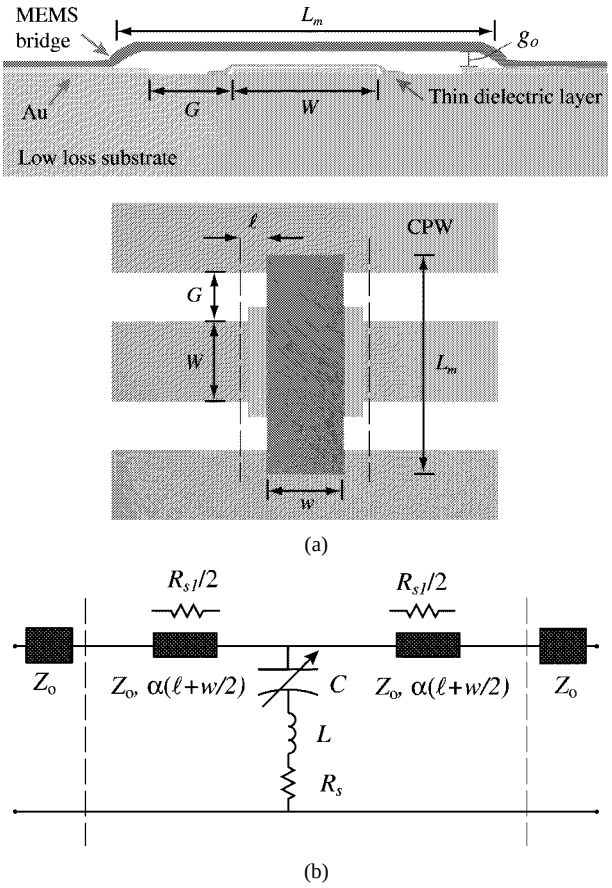

Fig. 1. (a) Typical shunt capacitive switch over a CPW shown in cross section in up position and top view. (b) Equivalent-circuit model.

II. MEMS Shunt-Switch Description

The single MEMS switch is fabricated on a CPW line with dimensions of $G/W/G = 60/100/60$ μm (50 Ω) for

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The authors are with the Radiation Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109-2122 USA (e-mail: muldavin@engin.umich.edu; rebeiz@umich.edu).

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dc–40-GHz measurements on a high-resistivity silicon substrate (3000 Ωcm). The switch length L_m is 300 μm and the anchors are 40 μm from the CPW ground plane edge. Various membrane widths are used in this work, from 20 to 140 μm so as to achieve different switch capacitance and inductance values. The membrane height is $g_o = 1.5$–2 μm, and the membrane thickness t is 2 μm.

A. Actuation Mechanics

In order to actuate the switch, the center conductor of the CPW line is dc biased with respect to the ground. The resulting electrostatic forces pull the membrane toward the center conductor, with a pull-down voltage of

$$V_p = \sqrt{\frac{8k}{27\epsilon_o W w} g_o^3} \tag{1}$$

where k is the effective spring constant of the membrane, W is the CPW center conductor width, w is the membrane width, ϵ_o is the permittivity of free space, and g_o is the nominal gap height. Notice that the pull-down voltage is independent of the switch width. The effective spring constant k of the membrane can be approximated by [5]

$$k = \frac{32Et^3w}{L_m^3} + \frac{8\sigma(1-\nu)tw}{L_m} \tag{2}$$

where E is Young's modulus of the membrane material, t is the membrane thickness, L_m is the membrane length, σ is the residual tensile stress in the membrane, and ν is Poison's ratio for the membrane material. For a 2-μm-thick electroplated Au switch ($E = 80$ GPa, $\nu = 0.42$) with $L_m = 300$ μm, $g_o = 1.5$ μm, and $\sigma = 0$ and 20 MPa, the pull-down voltage is 26 and 35 V, respectively. Once the bias voltage is released, the mechanical stresses in the membrane overcome the stiction forces and pull the membrane away from the dielectric layer, returning it to the original position. The switching time is dominated by squeeze film damping when the switch is being pulled down [5]–[7], and by the time it takes for the membrane to pull itself up from the dielectric layer. Switching times of 5–20 μs have been reported [2], [3].

B. Fabrication

The MEMS switch was implemented on a 400-μm-thick high-resistivity silicon substrate ($\epsilon_r = 11.9$) covered with 4000-Å SiO_2 using a finite-ground CPW [8]. The CPW lines are defined using a liftoff process by evaporating a 300/8000-Å layer of Ti/Au. Next, a 1000–2000-Å plasma-enhanced chemical vapor deposition (PECVD) Si_xN_y layer is deposited and patterned. A 1.5–2-μm-thick sacrificial layer of photoresist is then deposited and patterned. The thickness of this layer determines the nominal gap height g_o of the membrane. A 300/1000/1000-Å Cr/Au/Ti seed layer is evaporated, and then patterned to remove the top Ti layer so that the membranes and circuit metal, excluding the area underneath and near the membrane, can be electroplated with Au at the same time. The Au is electroplated in a 55° cyanide-based solution with a current density of 2–4 mA/cm^2. The electroplating thickness is approximately 2–2.5 μm. The sacrificial layers are removed using Ti, Cr, and Au etchants to remove the seed layers and Acetone to remove the resist layer. To avoid collapsing the membrane during drying, the structure can be released using a critical point drying system [9].

The Au membrane switches have a low compressive residual stress under the process parameters described above. However, the compressive stress only slightly decreases the pull-down voltage of the switch since the mechanical stress due to the spring constant is much larger than the residual stress. A material with a slightly tensile residual stress is preferred. The choice of Au as the membrane material was determined by process availability. Typical pull-down voltages for these switches are 12–25 V, depending on the plating rate, membrane thickness, resist profile, and vertical stress gradients.

III. Circuit Model of the MEMS Shunt Switch

The MEMS switch is modeled by two short sections of transmission line and a lumped CLR model of the bridge with the capacitance having the up-state/down-state values. The transmission-line sections are of length $(w/2) + \ell$ where $\ell = 40$ μm is the distance from the reference plane to the edge of the MEMS bridge. Typical values of the capacitance for millimeter-wave switches are 35 fF/2.8 pF, an inductance of 7–8 pH and a series resistance of 0.2–0.3 Ω. For X-band switches, the capacitance is 100 fF/8 pF with an inductance of 4–5 pH and a series resistance of 0.15 Ω (the modeling of the bridge CLR values will be presented in the following section).

The switch shunt impedance is given by

$$Z_s = R_s + j\omega L + \frac{1}{j\omega C} \tag{3}$$

with $C = C_u$ or C_d depending on the position of the switch. The *LC* series resonant frequency of the shunt switch is

$$f_o = \frac{1}{2\pi\sqrt{\mathrm{LC}}} \tag{4}$$

and the impedance of the shunt switch can be approximated by

$$Z_s = \begin{cases} \dfrac{1}{j\omega C}, & \text{for } f \ll f_o, \\ R_s, & \text{for } f = f_o, \\ j\omega L, & \text{for } f \gg f_o. \end{cases} \tag{5}$$

The CLR model behaves as a capacitor below the *LC* series resonant frequency and as an inductor above this frequency. At resonance, the CLR model reduces to the series resistance of the MEMS bridge. For $C_u/C_d = 35$ fF/2.8 pF with $L = 7$ pH, the resonance occurs at $f_0 = 322$ and 36 GHz when the switch is in the up-state/down-state position, respectively. It is for this reason ($f_0 = 322$ GHz) that the inductance of the bridge plays absolutely no role in the up state for $f < 100$ GHz. As will be seen later, the inductance plays an important role in the down state.

The cutoff frequency of the switch is sometimes stated as $f_c = 1/2\pi C_u R_s$, and $f_c = 30$ THz for a switch with $C_u = 35$ fF and $R_s = 0.15$ Ω. While this figure-of-merit has been used extensively with Schottky and p-i-n diodes, it is not applicable to MEMS switches. The reason is that the switch inductance limits the down-state performance at a much lower

TABLE I
SIMULATED STATIC CAPACITANCE OF A MEMS BRIDGE ($L_m = 300$ μm, $t = 2$ μm, $t_d = 1500$ Å, $\epsilon_r = 7.6$)

w	IE3D	HFSS	Measured
20 μm	20.5 pH	15.8 pH	15 pH
30 μm	15.5 pH	13.5 pH	12.5 pH
50 μm	13.5 pH	10.5 pH	9.5 pH
80 μm	9.5 pH	8 pH	7 pH
110 μm	6.5 pH	5.8 pH	5.1 pH
140 μm	5.5 pH	4.4 pH	–

frequency than f_c. A better value to use is the down-state resonant frequency (f_o or $2f_o$) since the MEMS shunt switch results in acceptable isolation up to twice the resonant frequency in the down-state position.

IV. MODELING OF THE MEMS SHUNT SWITCH

A. Up-State Capacitance

The parallel-plate capacitance of the MEMS shunt switch is

$$C_{\rm pp} = \frac{\epsilon_o w W}{g_o + \dfrac{t_d}{\epsilon_r}}. \tag{6}$$

The second term in the denominator is due to the finite thickness of the dielectric and, if neglected, the paralle-plate capacitance is equal to the standard formula of $C = (\epsilon_o A)/(g+t_d)$. For a dielectric thickness of 1500 Å, a dielectric constant of 7.6 (Si_xN_y) and a bridge height of 4 μm, neglecting the second term results in an underestimation of the parallel-plate capacitance by 3%, and for a height of 1.5 μm, the error increases to 10%.

The fringing field capacitance of MEMS switches, i.e., C_f, is a substantial portion of the total capacitance, as indicated in Table I (20%–50%). The calculation is done by solving for the total capacitance using a three-dimensional (3-D) electrostatic program called Maxwell 3D and subtracting the parallel-plate capacitance derived above.

Some MEMS switches are fabricated with a set of closely spaced holes in the bridge membrane. This is done to allow the removal of the sacrificial layer using dry-etching techniques, and to allow a faster operation of the switch by reducing the air damping underneath the bridge. The holes are typically 4 μm in diameter spaced at a period of 5–6 μm in a triangular or hexagonal lattice. The height of the bridge is typically 3–4 μm. The capacitance of this structure is simulated using the Ansoft Static Simulator and results in the same capacitance as a bridge fabricated using a continuous sheet of metal. This is due to the fringing fields, which completely cover the holes. The rule of thumb is that the hole diameter should be less than $2g_o$ to not affect the capacitance.

B. Down-State Capacitance and Capacitance Ratio

The MEMS switch capacitance in the down-state position can be easily calculated using $C_d = \epsilon_0 \epsilon_r A/d_1$. In this case, the thickness of the dielectric is so small that the fringing capacitance can be neglected. The down-state/up-state capacitance ratio is

$$\frac{C_d}{C_u} = \frac{\dfrac{\epsilon_o \epsilon_r A}{t_d}}{\left(\dfrac{\epsilon_o A}{g_o + t_d/\epsilon_r}\right) + C_f}. \tag{7}$$

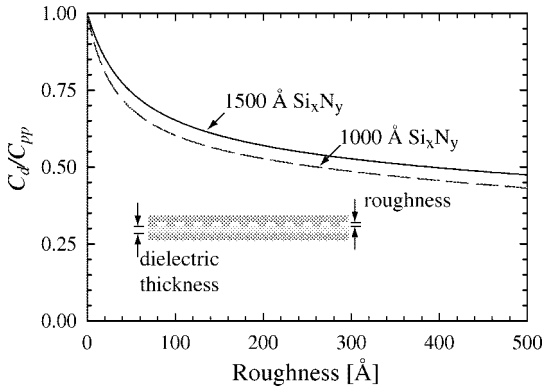

Fig. 2. Simulated down-state capacitance versus roughness in the overlying bridge layer.

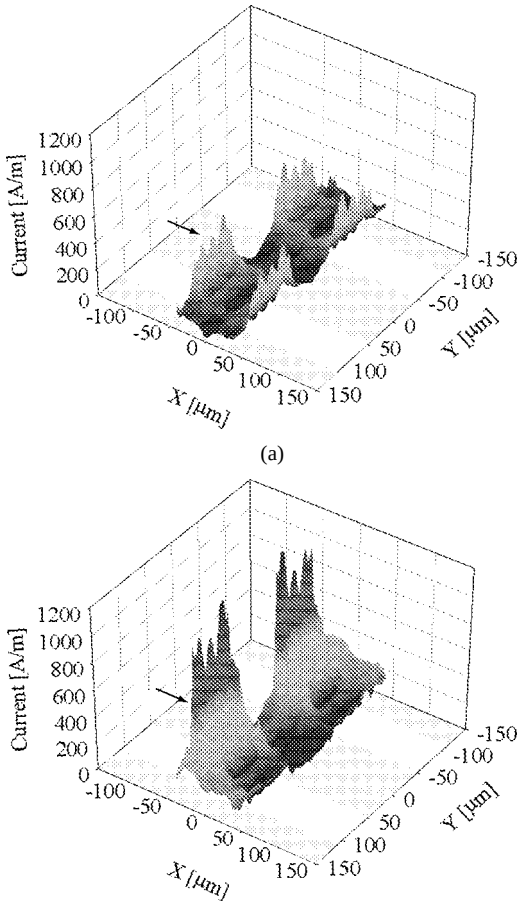

Fig. 3. Simulated current distribution on the MEMS bridge in: (a) the up state and (b) the down state for an 80-μm-wide MEMS bridge 0.1 μm over a 60/100/60-μm CPW line. A 1-W wave is incident from the left-hand side and travels in the x-direction.

For a dielectric thickness of 1000 Å and $\epsilon_r = 7.6$, the capacitance ratio is 60 : 1 and 120 : 1 for a capacitance area of 80 × 100 μm, and a height of 1.5 and 4 μm, respectively.

It is tempting to make the dielectric layer as thin as possible to increase the capacitance ratio. However, it is impractical to deposit a Si_xN_y layer, which is thinner than 1000 Å due to pin-hole problems in thin dielectric layers. Also, this dielectric layer must be able to withstand the actuation voltage (20–50 V) without dielectric breakdown. It is for this reason that this layer is typically 1000–1500-Å thick in all switches built today.

The down-state capacitance can be degraded if the MEMS bridge layer or dielectric layer are rough. This can be due to the deposition parameters of the nitride or the fabrication process of the MEMS bridge. Fig. 2 shows the reduction in the down-state capacitance assuming a perfectly flat dielectric layer, and a roughness 0–500 Å. The contact area is assumed to be 50% of the total bridge area. The dielectric layer is 1000-Å (1500- Å) thick with a dielectric constant of 7.6. It is seen that a capacitance degradation of 65% (60%) occurs for a roughness of 100 Å. Therefore, for optimal capacitance ratio, it is essential that the roughness of the MEMS bridge and that of the dielectric layer be kept at less than 40 Å.

C. Current Distribution

The current distribution at 30 GHz of a MEMS bridge in the up-state position, with a width of 80 μm, and suspended 3 μm above the transmission line is shown in Fig. 3(a). The capacitance of the MEMS switch is around 32 fF. The switch is placed in a CPW configuration, but the results are the same for a microstrip design. The normalized current distribution is obtained using IE3D[1] or Sonnet. It is seen that there is no RF current on the bridge portion, which is above the transmission line. Also, the current is concentrated on the edge of the bridge over the CPW gap. If the bridge width is changed to 40 μm, the current distribution remains unchanged, always hugging the edges of the MEMS bridge.

The current distribution in the down state with $w = 80$ μm and $C_d = 0.5$ pF is shown in Fig. 3(b). It is seen that the current is concentrated on one edge of the MEMS bridge since this edge presents a short circuit to the incoming wave. From Fig. 3(a) and (b), it is expected that the up-state inductance and resistance of the MEMS switch are different from the down-state values. However, as discussed before, the down-state inductance is of importance since it affects the operation of the switch at millimeter-wave frequencies.

D. Series Resistance

There are two components to the series resistance of the MEMS switch. The first component (R_{s1}) is approximated by

$$\alpha = \frac{R_{s1}/\ell}{2Z_o} \tag{8}$$

and is due to the transmission-line loss (both ohmic and dielectric) and depends on the definition of the reference plane. The second component is R_s, which is due to the MEMS bridge only [see Fig. 1(b)].

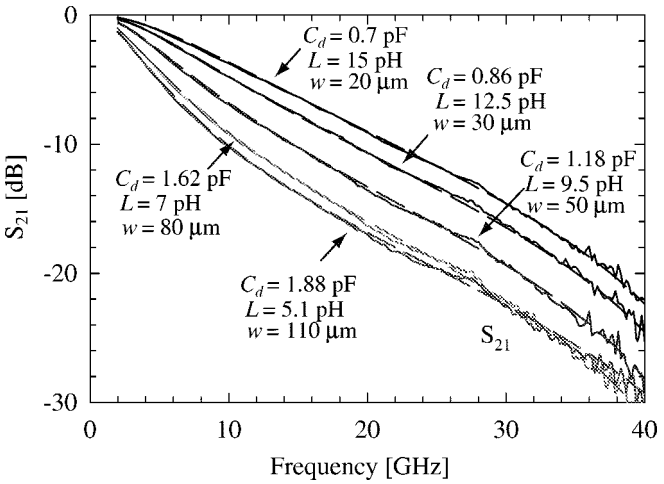

Fig. 4. Down-state measured and fitted S-parameters for MEMS switches of various widths.

The measured attenuation of the CPW line can be used to derive R_{s1}. For the switch in the up state and $|S_{11}| < -10$ dB, we assume that the current on the center conductor is unaffected by the bridge. For a CPW line on high-resistivity silicon with an 8000-Å-thick Au center conductor and 2-μm-thick Au ground planes, the measured attenuation is $\alpha = 1.7$ dB/cm (0.20 Np/cm) at 30 GHz. A switch length (the distance between the reference planes) of 160 μm results in a line loss of 0.027 dB (0.0031 Np) and an equivalent R_{s1} of 0.32 Ω. For an 8000-Å-thick Au CPW line with $G/W/G = 100/100/100$ μm on quartz, the measured attenuation is $\alpha = 0.4$ dB/cm (0.046 Np/cm) at 30 GHz, which results in a line loss of 0.005 dB (0.0006 Np) and an equivalent R_{s1} of 0.06 Ω.

The resistance of the MEMS bridge (R_s) is much harder to calculate due to the current distributions in the up and down states [see Fig. 3(b)]. Simple equivalent models based on simulated current distributions and the assumption of uniform current penetration to a skin depth in the metal can be derived and applied to the calculation of the bridge resistance R_s. For reasons of simplicity, we omit the presentation of these models. As shown in Section V-C, the bridge resistance in the down state can be accurately extracted from the measured S-parameters.

The skin depth is $\delta = 1/\sqrt{f\pi\mu\sigma}$ and for an Au (and Al) bridge, the skin depth is 0.73 μm (0.84 μm) at 10 GHz and 0.42 μm (0.48 μm) at 30 GHz. If the bridge thickness is smaller than two skin depths, the switch resistance is constant with frequency. For thick Au MEMS bridges ($t > 1.5$ μm), the switch resistance changes with frequency as $\sqrt{f}$ above 30 GHz due to the skin depth effect, and is constant at lower frequencies. For thin Al bridges (0.5–1 μm), the bridge resistance is constant at all frequencies of interest.

E. Inductance

A simple and accurate way to model the switch inductance in the down state is to assume that the capacitance of the switch is large enough so that it is a short circuit, and to model this short circuit using numerical electromagnetic techniques (IE3D,

[1]IE3D, Release 5, Zeland, Fremont, CA, 1998.

TABLE II
MEMS BRIDGE INDUCTANCE FOR SEVERAL BRIDGES WITH VARIOUS WIDTHS
($L_m = 300\ \mu$m, $t = 2\ \mu$m)

$w \times W$ [μm^2]	g [μm]	C_t [fF]	C_{pp} [fF]	C_f [fF]	C_f/C_{pp}
40×100	4	13.8	8.8	5	57%
80×100	4	23.4	17.6	5.8	33%
140×160	4	59.2	49.3	9.9	20%
40×100	1.5	29.8	23.2	6.5	28%
80×100	1.5	55.6	46.6	9	19%

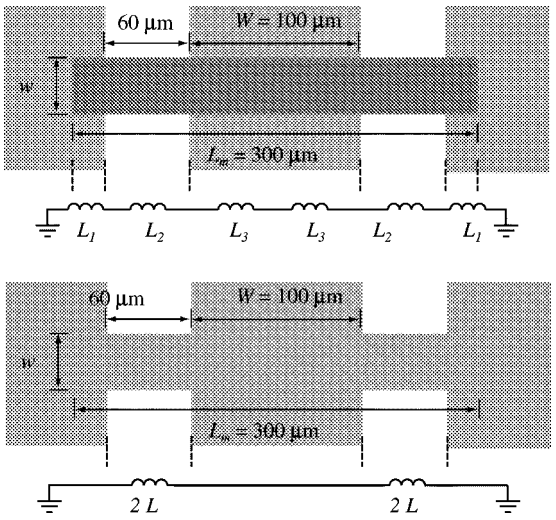

Fig. 5. Equivalent-circuit model for the inductance of the MEMS switch in the down state.

Sonnet, HFSS[2]). This results in an efficient computation since the dielectric layer is completely ignored. The modeled S-parameters from 1 to –60 GHz are fitted to an *RL* model, and the series resistance and inductance are extracted. The numerical software does not give an accurate value for the series resistance (since it is very small), but results in excellent modeling of the inductance.

The down-state isolation for rectangular switches of increasing widths (length is held constant at $L_m = 300\ \mu$m) is shown in Fig. 4. The switch inductance and capacitance can be *uniquely* determined to within ±3% from a fit of the equivalent circuit to the measured 2–40-GHz S-parameters (see Section V-B for details). The down-state capacitance is 0.5–0.8 times the parallel plate estimate due to the surface roughness of the underlying metal and dielectric layers. Table II shows the modeled values and the comparison with fitted values obtained from S-parameter measurements shown in Fig. 4. Notice that for a bridge width change from 20 to 140 μm, the inductance changes by a factor of 3.0 and not 7.0, indicating that the RF current is concentrated on the first edge of the bridge, and is weakly dependent on the width of the bridge.

The bridge inductance can be modeled as a set of inductances in series, as shown in Fig. 5. However, the values of L_1 and L_3 are very small (less than 1 pH). This is due to two factors: the current is carried predominantly on the edge of the CPW center conductor and ground planes and, therefore, the portions

[2]HFSS, Release 6, Ansoft Maxwell HFSS, Pittsburgh, PA, 1998.

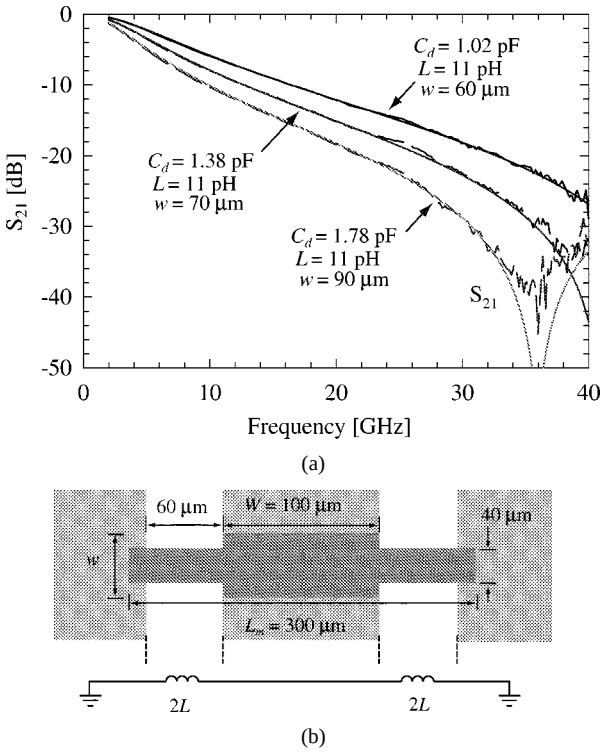

Fig. 6. (a) Down-state measured and fitted S-parameters for MEMS switches where the width of the section over the center conductor is varied and the portion over the CPW gap is held constant. (b) Schematic and equivalent circuit for the inductance.

of the bridge over the CPW center conductor and ground planes (L_1, L_3) contribute insignificantly to the bridge inductance, and there is a canceling (image) effect due to the backing metal conductor ($g = 0.2$–$1.5\ \mu$m) for these portions of the bridge. Therefore, the bridge inductance is dominated by L_2, which is associated with the portion of the bridge over the CPW gaps.

An experiment was performed to further prove that the bridge inductance is due to the portion of the bridge over the CPW gaps. In this case, the width of the portion of the bridge over the apertures of the CPW is held constant (40 μm) and the width of the bridge over the center conductor of the CPW is varied (see Fig. 6). The measured S-parameters were again fit to a CLR model. It is seen that the fitted capacitance (accurate to ±3%) varies from 1 to 1.78 pF as w increases, but the switch inductance is constant at 11 pH for the three cases.

F. Loss

The loss of a MEMS shunt switch is sometimes taken to be $|S_{21}|^2$. The decrease in S_{21} does not necessarily indicate power loss in the switch, but can simply be due to an increase in the reflected power from the switch ($|S_{11}|^2$). The loss of a MEMS switch is better derived from the S-parameters as

$$\text{Loss} = 1 - |S_{11}|^2 - |S_{21}|^2 \tag{9}$$

and this can be easily calculated using a microwave circuit simulator (Libra,[3] etc.) or using measured values.

The MEMS shunt switch loss is composed of two parts: the transmission-line loss underneath the bridge, and the MEMS

[3]Libra, Series IV 6.6, Hewlett-Packard Company, Santa Rosa, CA, 1997.

bridge loss. The power loss in the bridge is $P_{\text{loss}} = I_s^2 R_s$, where I_s is the current in the bridge. The MEMS bridge loss is

$$\text{Loss} = \frac{\text{Power loss in MEMS bridge}}{\text{Power incident on the switch}} = \frac{I_s^2 R_s}{|V^+|^2/Z_o} \tag{10}$$

$$\text{Loss} = \left| \frac{2Z_s \,||\, Z_o}{Z_s \,||\, Z_o + Z_o} \right|^2 \frac{1}{|Z_s|^2} R_s Z_o. \tag{11}$$

In the up-state position and for $S_{11} < -13$ dB, we have $Z_s \gg Z_o$ and the loss becomes

$$\text{Loss} = \omega^2 C_u^2 R_s Z_o. \tag{12}$$

In the down-state position and for $S_{21} > -10$ dB, we have $Z_s \ll Z_o$ and the loss is

$$\text{Loss} = \frac{4R_s}{Z_o}. \tag{13}$$

The loss of a MEMS switch with $C_u = 35$ fF, $C_d = 2.8$ pF, $L = 7$ pH, and $R_s = 0.1\ \Omega$ and $0.25\ \Omega$ (constant with frequency) is shown in Fig. 7. The switch loss is also plotted for $R_s = 0.25\ \Omega$, taking into account two 40-μm sections of transmission line at both sides of the switch. The line loss is assumed to be 0.1, 0.25, and 1.5 dB/cm at 30 GHz and varying as $\sqrt{f}$ with frequency, which is typical of microstrip and CPW transmission lines on quartz and silicon substrates.

From the above calculations, it seen that the switch loss is dominated by the transmission-line loss in the up-state position, especially for high-resistivity silicon substrates. Therefore, the measured loss of a MEMS switch is directly dependent on the definition of the reference planes. In the up state, it is very hard to measure a switch loss of 0.005–0.015 dB at 1–30 GHz. One way of obtaining an accurate loss value is to measure 6–8 closely spaced switches and divide the insertion loss by the number of switches. In the down state, the switch loss is 0.07–0.1 dB for $R_s = 0.25\ \Omega$ above 10 GHz, and less than 0.06 dB for $R_s = 0.1\ \Omega$.

V. Fitting CLR Parameters to S-Parameter Measurements

The CLR values can be extracted accurately from S-parameter measurements. In this case, the MEMS switch is fabricated and measured from 1 to 40 GHz using on-wafer calibration techniques. At The University of Michigan at Ann Arbor, we have used the thru-reflection-line (TRL) calibration technique, and defined the reference planes to be 40 μm from the MEMS bridge.

A. Up-State Capacitance

The S-parameters are first measured in the up-state position and the measured data (S_{11}) is fitted to get the up-state capacitance of the switch. The inductance and resistance are not fitted using this measurement since their effect is negligible in the up-state position.

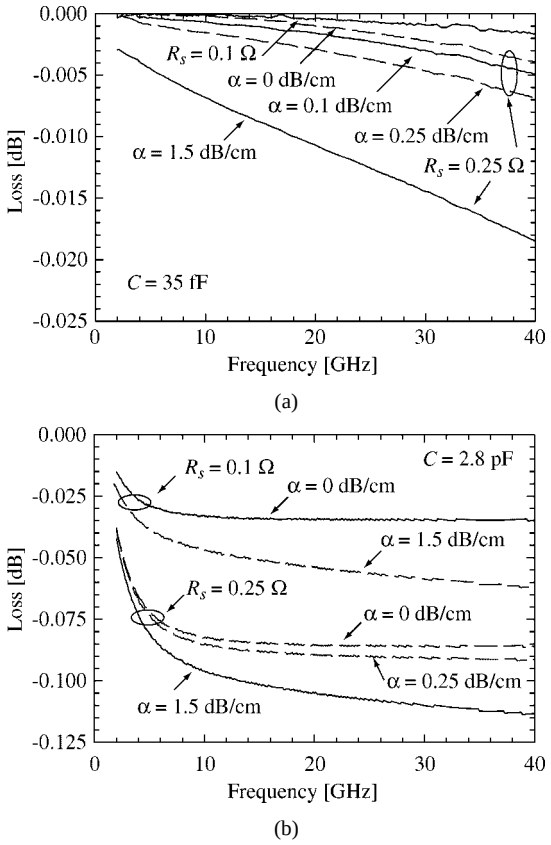

Fig. 7. (a) Up-state and (b) down-state simulated loss ($|S_{11}|^2 + |S_{21}|^2$) for various values of R_s and α. The reference planes are 40 μm from the edge of the MEMS switch.

In the up-state position, the reflection coefficient is (neglecting LR_s)

$$S_{11} = \frac{-j\omega C_u Z_o}{2 + j\omega C_u Z_o} \tag{14}$$

and for $|S11| < -10$ dB or $\omega C_u Z_o \ll 2$

$$S_{11}^2 = \frac{\omega^2 C_u^2 Z_o^2}{4}. \tag{15}$$

The above equations result in a straightforward determination of the up-state capacitance of the MEMS shunt switch from the measured data. Fig. 8 shows the measured and fitted up-state S-parameters of a MEMS switch, 80-μm wide and with dimensions shown in Fig. 1. It is seen that the fitted up-state capacitance (70 fF) agrees well with the electrostatic value derived above (68 fF).

B. Down-State Capacitance and Inductance

The S-parameters are measured with the switch in the down-state position, and a CLR model is fitted to the measured data (S_{21}) using Libra. Fig. 9 shows a typical switch in the down-state position and the fitted capacitance and inductance (CL) values. Notice that the capacitance solely controls the response from 1 to 20 GHz (up to $\sim f_o/2$). Once the capacitance is determined, the inductance value controls the resonant frequency location. Even if the resonant frequency of the MEMS switch is beyond the measurement bandwidth, the inductance has a strong

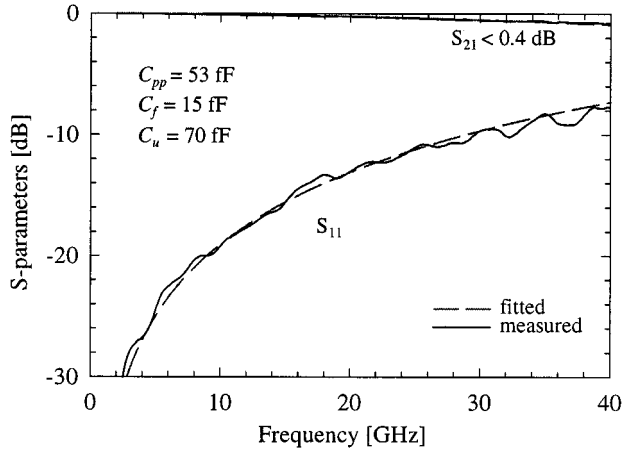

Fig. 8. Up-state measured and fitted S-parameters for an 80-μ-wide bridge with a nominal gap height g_o of 1.5 μm.

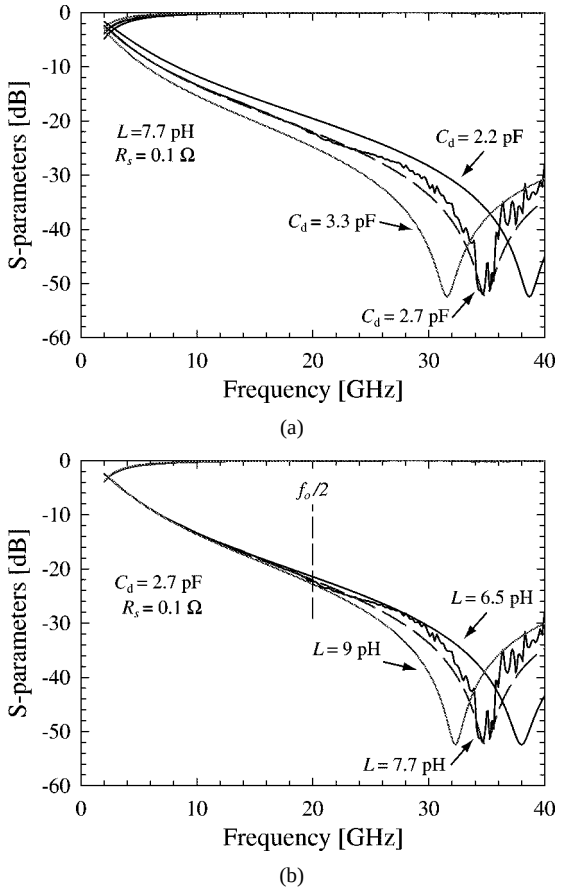

Fig. 9. Down-state measured and fitted S-parameters for an 80-μm-wide bridge.

effect on the slope of S_{21} after $f_o/2$, and this fact can be used to fit an accurate model of the switch inductance.

The switch inductance and capacitance are *uniquely* determined to within $\pm 3\%$ from a fit of the equivalent circuit to the measured 2–40-GHz S-parameters. As indicated above, the down-state capacitance is dependent on the surface roughness and cannot be easily modeled. The inductance agrees quite well with full-wave modeling (see Section IV-E).

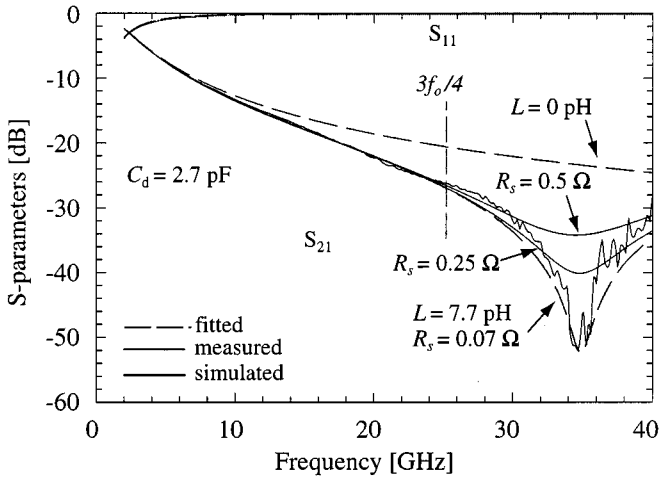

Fig. 10. Down-state measured and fitted S-parameters for an 80-μm-wide bridge, showing the effect of the inductance and resistance (R_s) on the fit.

C. Series Resistance of the MEMS Bridge

The series resistance of the MEMS bridge is best fitted around the resonant frequency. In this case, the switch impedance is $Z_s = R_s$ and S_{21} is

$$S_{21}|_{\omega_o} = \frac{2R_s \,||\, Z_o}{R_s \,||\, Z_o + Z_o} \simeq \frac{2R_s}{Z_o + R_s}. \tag{16}$$

Fig. 10 shows the fitted S-parameter for an Au switch fabricated at The University of Michigan at Ann Arbor ($w = 80\,\mu$m, same dimensions as above) with $C_d = 2.7$ pF, $L = 7.7$ pH, and $R_s = 0.07\ \Omega$. The response for $R_s = 0.07\ \Omega$, $0.25\ \Omega$, and $0.5\ \Omega$ are included for comparison. It is seen that as the series resistance gets smaller, the resonance in S_{21} gets sharper and deeper (-48, -40, -34, dB, respectively). In fact, an excellent calibration (to -50 dB) is needed to be able to measure a series resistance of $0.1\ \Omega$. Also, the series resistance has virtually no effect at $f < 3f_o/4$, thus, it is important to measure the S-parameters of the switch around the resonant frequency.

Fig. 10 also shows the calculated S-parameters for $L = 0$ pH. It is clear from Fig. 10 that the inductance and resistance cannot be ignored in the down state. The *LC* resonant frequency for most shunt switch designs is 20–50 GHz, depending on the dimensions of the switch. Therefore, the isolation in the down-state position can be dramatically increased (20^+ dB) by designing for the required resonant frequency. This is done in part 2 of this paper [10].

VI. Conclusion

This paper presented an electromagnetic model of the MEMS shunt switch, which is derived using standard numerical simulators. A step-by-step approach for extracting the CLR parameters of the MEMS shunt switch from the measured S-parameters was shown. It is seen that the loss of the MEMS shunt switch in the up state is limited by the transmission line and, therefore, is directly dependant on the definition of the reference planes. Also, the inductance of the switch in the down state has a large effect on the isolation, and can actually improve the performance of the switch by 10–20 dB at resonance.

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Jeremy B. Muldavin (S'86) received the B.S.E. degree in engineering physics from The University of Michigan at Ann Arbor, in 1996, and is currently working toward the Ph.D. degree in electrical engineering at The University of Michigan at Ann Arbor.

He spent four years as a Student Researcher in the High Energy Spin Physics Group, The University of Michigan at Ann Arbor. His research interests are development and characterization of novel MEMS structures and interconnects for components and subsystems in wireless communication systems.

Gabriel M. Rebeiz (S'86–M'88–SM'93–F'97) received the Ph.D. in electrical engineering from the California Institute of Technology, Pasadena, in 1988.

In September 1998, he joined the faculty of The University of Michigan at Ann Arbor, and became a Full Professor in May 1998. He has held short Visiting Professorships at Chalmers University of Technology, Göteborg, Sweden, Ecole Normale Superieur, Paris, France, and Tohoku University, Sendai, Japan. His research interests are in applying micromachining techniques and MEMS for the development of novel components and subsystems for wireless communication systems. He is also interested in Si/GaAs radio-frequency integrated-circuit (RFIC) design for receiver applications, and in the development of planar antennas and microwave/millimeter-wave front-end electronics for applications in millimeter-wave communication systems, automotive collision-avoidance sensors, monopulse tracking systems, and phased arrays.

Prof. Rebeiz received the 1991 National Science Foundation Presidential Young Investigator Award and the 1993 URSI International Isaac Koga Gold Medal Award for Outstanding International Research. He received the 1995 Research Excellence Award presented by The University of Michigan at Ann Arbor. Together with his students, he has received Best Student Paper Awards presented by the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) (1992, 1994–1999), and the IEEE Antennas and Propagation Society (IEEE AP-S) (1992, 1995) and the 1990 *Journees Int. Nice Antennes* (JINA) Best Paper Award. He received the 1997 Electrical Engineering and Computer Science Department Teaching Award, the 1998 College of Engineering Teaching Award, and was selected by the students as the 1997–1998 Eta–Kappa–Nu Electrical Engineering and Computer Science Professor of the Year. In 1998, he received the Amoco Foundation Teaching Award, given yearly to one (or two) faculty at The University of Michigan at Ann Arbor, for excellence in undergraduate teaching. He is also the corecipient of the IEEE 2000 Microwave Prize for his work on MEMS switches and phase shifters.