A Phase-Interpolation Direct Digital Synthesizer with an Adaptive Integrator

Akihiro Yamagishi, Hideyuki Nosaka, *Member, IEEE*, Masahiro Muraguchi, *Member, IEEE*, and Tsuneo Tsukahara, *Member, IEEE*

***Abstract*—A phase-interpolation direct digital synthesizer (DDS) with an adaptive integrator is described in this paper. Unlike a conventional DDS, it does not use ROM or a D/A converter. Therefore, less power is dissipated and the maximum speed is increased. The delay time for phase interpolation is generated by the adaptive integrator, which is composed of a capacitance switch array and current switch array, and by a comparator with constant threshold voltage. The DDS was fabricated on 0.5-μm CMOS process technology. The spurious level is lower than −50 dBc and the power dissipation is 60 mW at a clock frequency of 40 MHz and output frequency of about 19 MHz.**

***Index Terms*—CDMA, CMOS, DDS, frequency hopping, synthesizer.**

I. Introduction

CONVENTIONAL designs for wireless systems employ a phase-locked loop (PLL) for the synthesizer because a PLL has a low power dissipation, low spurious-frequency level, and high accuracy in the frequency. However, the frequency switching of a PLL is very slow, which limits the channel-switching flexibility. On the other hand, wireless systems employing a direct digital synthesizer (DDS) do not suffer from this limitation; the frequency switching is much faster and, thus, the channel-switching flexibility is improved. For example, a DDS can switch channels during the guard time for TDMA slots. DDS's are also useful for 64-kb data communication services in personal handy phone systems and for frequency-hopping CDMA systems like Bluetooth. We, therefore, believe they will be a key components in for future advanced wireless systems. However, DDS's are generally thought to be more power hungry and to have a higher spurious-frequency output than PLL's [1], [2]. Consequently, they have not been widely used in portable wireless communications equipment.

We have developed a phase-interpolation DDS that, unlike a conventional DDS, does not use ROM and a D/A converter. The maximum speed of a conventional DDS depends on the ROM access time, and the ROM or D/A converter account for most of the power dissipation. Therefore, with the phase-interpolation DDS, less power is dissipated and the maximum speed is increased. The conventional DDS also has high-level alias frequencies reflected at the Nyquist frequency. As a result, the usable output frequency is only 1/3 or 1/4 of the clock frequency. However, the interpolation DDS does not have such alias frequencies, which means the usable output frequency reaches 1/2 of the clock frequency. We have already proposed a phase-interpolation DDS with a digitally controlled delay generator, in which the delay time is generated by a ramp wave generator and adaptive threshold voltage generator [3]. In this paper, we describe a new DDS fabricated on 0.5-μm CMOS process technology. In this DDS, delay time is generated by an adaptive integrator composed of a capacitance switch array and current switch array, and by a comparator with constant threshold voltage.

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A. Yamagishi and T. Tsukahara are with NTT Telecommunications Energy Laboratories, Kanagawa 243-0198, Japan (e-mail: aki@aecl.ntt.co.jp).

H. Nosaka is with the NTT Photonics Laboratories, Kanagawa 239, Japan.

M. Muraguchi is with the NTT Electronics Corporation, Kanagawa 239, Japan.

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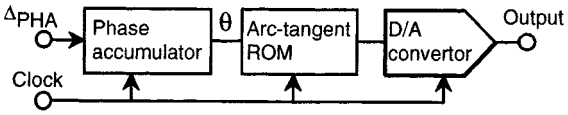

Fig. 1. Block diagram of a conventional DDS.

II. Phase Interpolation DDS Architecture

A conventional DDS consists of a phase accumulator, an arc-tangent ROM, and a D/A converter (Fig. 1). The phase accumulator generates the phase data θ needed in order to accumulate input data, namely, the frequency control word $\Delta_{\rm PHA}$, at a clock frequency. The arc-tangent ROM converts the phase data to digital sine wave data, and the D/A converter converts that to an analog signal. The output frequency f_o is given by

$$f_0 = \frac{\Delta_{\rm PHA}}{2^N} f_{\rm CLK} \tag{1}$$

where $f_{\rm CLK}$ is the clock frequency. The main problems of the conventional DDS are a high spurious-frequency level and high power dissipation, which have a tradeoff relationship. The spurious-frequency level of the DDS arises from quantized error in the phase and sine wave data. Increasing the bit length of the phase data and sine wave data decreases the spurious-frequency level. Doing so, however, means the ROM capacity and D/A converter bit length have to be increased, which results in increased power dissipation and a lower maximum speed. Therefore, many techniques for compressing of the ROM capacity have been proposed [4].

The phase-interpolation DDS has nether a ROM nor a D/A converter (Fig. 2). Therefore, the problems of the conventional DDS are eliminated, and a low spurious-frequency level, low-power, and a high-output frequency are possible. The

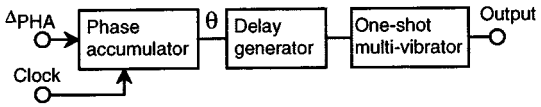

Fig. 2. Block diagram of the phase-interpolation DDS.

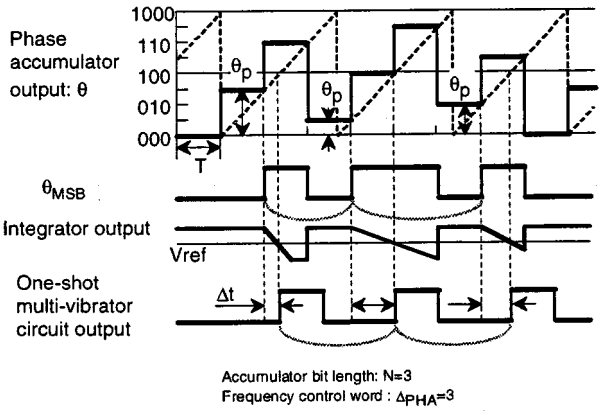

Fig. 3. Waveforms of the phase-interpolation DDS.

phase-interpolation DDS consists of a phase accumulator, a delay generator, and a one-shot multivibrator circuit. Fig. 3 shows the wave forms of the interpolation DDS for a phase accumulator bit length of three and a frequency control word of three. The accumulator is the same as that used in a conventional DDS. The phase accumulator output, i.e., the phase data, looks like ramp data. The MSB of the phase data, i.e., $\theta_{\rm MSB}$, has the same average frequency as the conventional DDS output frequency. However, it contains undesired spurious-frequency components because neither the pulse width nor the time interval are constant. The delay generator generates the desired delay adaptively in order to line up the rising edge of $\theta_{\rm MSB}$ on a constant time interval. The required delay time Δt is given by

$$\Delta t = \frac{2^{N-1} - \theta_p}{\Delta_{\rm PHA}} T \tag{2}$$

where θ_p is one datum of θ from the previous clock cycle. The multivibrator circuit produces the pulsewidth constant. Thus, the interpolation DDS generates a pulse wave that has constant time interval and pulse width, and its output frequency is given by (1).

III. Circuit Design

The delay generator is composed of an adaptive integrator and comparator. The integrator starts working at the rising edge of $\theta_{\rm MSB}$ and its time constant changes adaptively. The delay is generated by comparing the integrator output and the reference voltage. This means the delay generator causes the DDS to produce pulses whose rising edge lines up on a constant time interval. Consequently, there is a constant time interval between the rising edge of the pulses generated. The fundamental delay generation circuit is shown in Fig. 4. The integrator is composed of an array of current switching cells and an array of capacitance switching cells. The input voltage of the comparator decreases

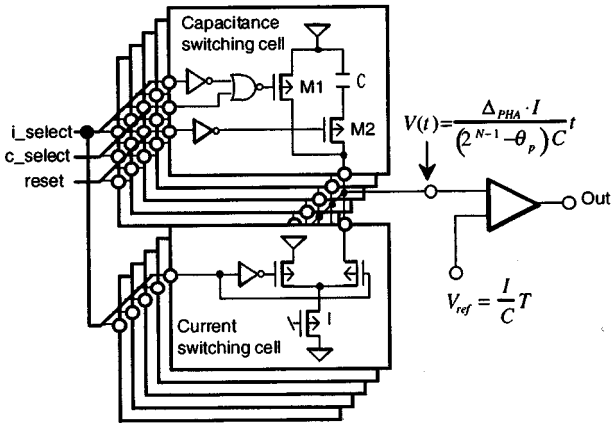

Fig. 4. Block diagram of the delay generation circuit.

linearly after integration starts, and the slope depends on the capacitance and current. Therefore, the delay time

$$\Delta t = \frac{c}{i} V_{\rm ref}. \tag{3}$$

The current switching array is controlled by $\Delta_{\rm PHA}$ and the capacitance switching array is controlled by the inverse of θ_p. Therefore, the output voltage of the integrator, i.e., the input voltage of the comparator, is given by

$$V(t) = \frac{\Delta_{\rm PHA} \cdot I}{(2^{N-1} - \theta_p)C} t \tag{4}$$

where C is unit capacity, I is the unit current value, and t is the time of integration. When

$$V_{\rm ref} = \frac{I}{C} T \tag{5}$$

the delay generator generates the required delay given by (2).

The circuit for each current switching cell consists of a current source and differential switch, while the circuit of each capacitance switching cell consists of a unit capacitor, two transistor switches, and a few logic gates. Transistor M2 is the selection switch for the integration capacitor, and M1 is the reset switch. M1 is controlled by a reset signal and a control signal to the current switching array in such a way that the starting voltage of the integrator is kept constant.

IV. Spectrum of the Phase-Interpolation DDS

Fig. 5 shows output spectrums of a conventional DDS and the phase-interpolation DDS. The conventional DDS exhibits high-level alias frequencies. As the output frequency increases, the alias frequency decreases. This limits the usable output frequency to 1/3 or 1/4 of the clock frequency. At that limit, the distance between the output and nearest alias frequency is short, which produces a high-level spurious frequency. On the other hand, the interpolation DDS has no alias frequencies because it does not have a D/A converter. It has high-level harmonics because the output consists of pulse waves. However, the frequency of the harmonics increases as the output frequency increases. As a result, the usable fundamental output frequency reaches half the clock frequency. Furthermore, the harmonics

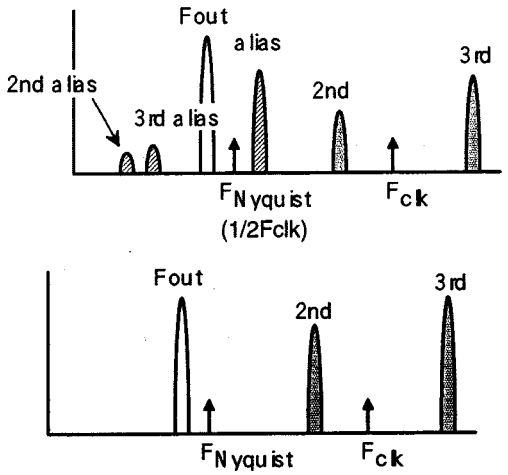

Fig. 5. Output spectra of a conventional DDS and a phase-interpolation DDS.

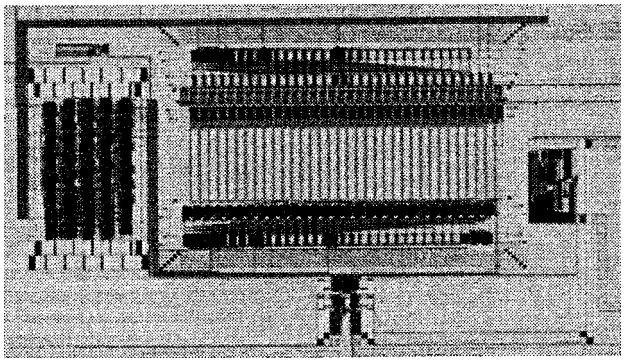

Fig. 6. Photograph of the prototype DDS IC.

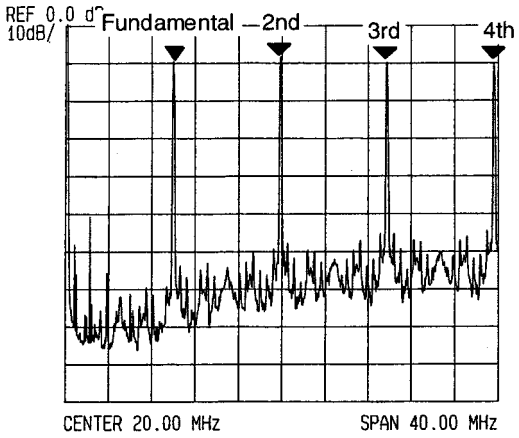

Fig. 7. The output spectrum of the prototype DDS IC ($f_{\mathrm{CLK}} = 40$ MHz, $\Delta_{\mathrm{PHA}} = 111111$).

can be used for output, which enables the output frequency to be greater than the clock frequency.

V. Experimental Results

We fabricated the prototype phase-interpolation DDS integrated circuit (IC) on 0.5-μm CMOS process technology. A photograph of the prototype is shown in Fig. 6. The chip size is 4 $\times$ 3 mm. In this prototype, the accumulator bit length is eight, and the unit capacitance is 0.5 pF. Since the unit current

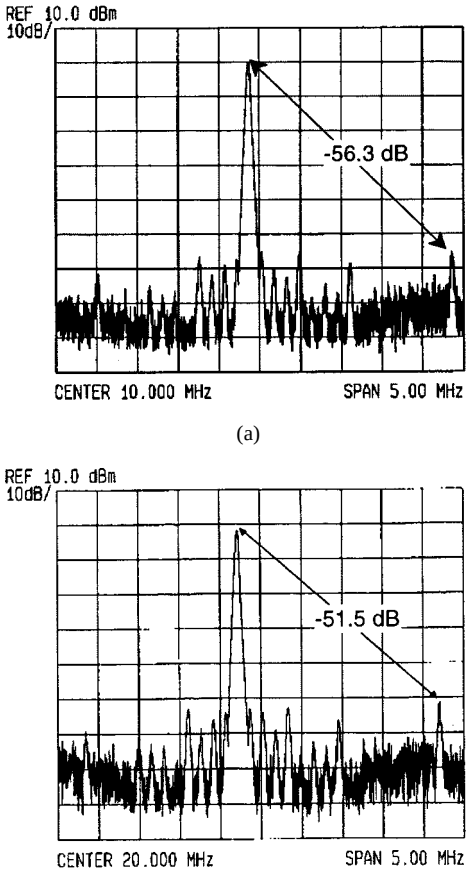

Fig. 8. The output spectrum of the prototype DDS IC. (a) Fundamental output spectrum. (b) Second harmonic input spectrum.

depends on the clock frequency, it is controlled by a bias voltage. Fig. 7 shows the output spectrum of the DDS IC. The output has harmonics, but does not have any alias frequencies. The clock frequency is 40 MHz, the output frequency control word is "111111," and the fundamental output frequency is 9.84375.4 MHz. At a 3-V power supply, the current dissipations are 3 mA for the analog parts, 0.5 mA for the digital parts, and 16 mA for the output parts. Fig. 8 shows the output spectrum of the fundamental and second harmonic for a frequency span of 5 MHz. The clock frequency and control word are the same as in Fig. 7. The fundamental output frequency is 9.84375 MHz, and the frequency step is 156.25 kHz. The spurious level is less than -55 dBc. The second harmonic output frequency is 19.6875 MHz, and the frequency step is 312.5 kHz. The spurious-frequency level is less than -50 dBc. The causes of the spurious frequencies in Fig. 8 is considered to be delay time error in the delay generator. Fig. 9 shows the simulated delay time error dependence of the spurious level. In this simulation, the spurious level was calculated by adding the ideal delay time to delay time error. To obtain a spurious level below -55 dB, the delay time error should be lower than 0.8%. One reason for the increasing spurious level is the parasitic capacitance of the transistors and lines connecting them. It is added into the denominator of (4) and makes delay time error. Therefore, the spurious level of this DDS could be decreased by using finer process technology. Fig. 10 shows the spurious-frequency

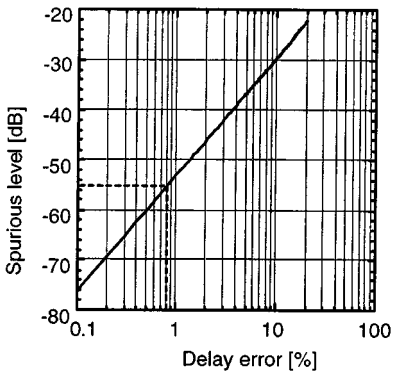

Fig. 9. Spurious level versus delay error of the phase-interpolation DDS (simulation).

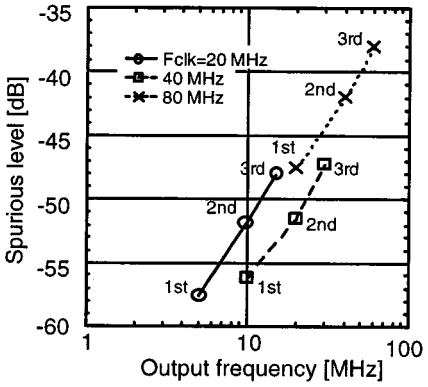

Fig. 10. Spurious level versus output frequency (the output frequency was changed by setting the clock frequency to the harmonics).

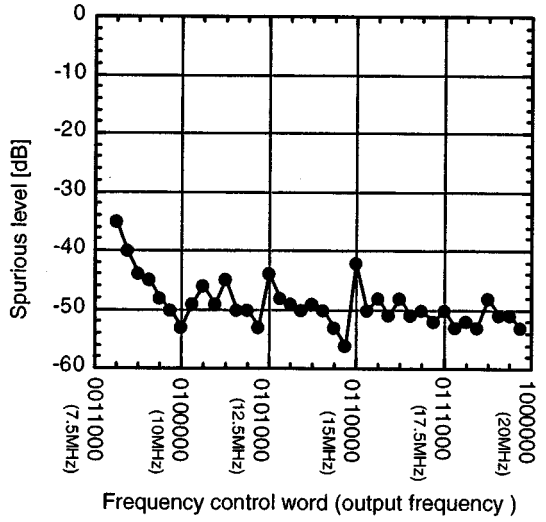

Fig. 11. Spurious level versus frequency control word ($f_{\mathrm{CLK}} = 40$ MHz, second harmonic output).

level within plus-or-minus 5 MHz of the desired frequency. To obtain these data, the output frequency control word was set to "111111." The output frequency was changed by setting the clock frequency to the frequency of the fundamental, second, and third harmonic, which are 20, 40, and 80 MHz. This graph shows that the DDS can generate frequencies higher than the Nyquist frequency. Fig. 11 shows the frequency control word dependence of the spurious-frequency level. For these data, the clock frequency was 40 MHz and the output frequency was set to that of the second harmonic. This DDS exhibits a spurious-frequency level of -40 dBc at a bandwidth of over 10 MHz.

VI. Conclusion

A phase-interpolation DDS with an adaptive integrator has been proposed in this paper. This DDS, unlike a conventional one, does not use ROM or a D/A converter. Therefore, less power is dissipated and the maximum speed is increased. We fabricated the DDS on 0.5-μm CMOS process technology. The spurious level is lower than -50 dBc and the power dissipation is 60 mW at a clock frequency of 40 MHz and output frequency of about 19 MHz. We have shown that the spurious-frequency level of the DDS depends on the delay error of the delay generator. One of the fundamental causes of the delay error is the parasitic capacitance of the transistors and connecting lines. Therefore, the spurious-frequency level and power dissipation of the DDS will be further decreased by using finer and silicon-on-insulator process technologies, which have smaller parasitic element. The phase-interpolation DDS will be useful for wireless systems that need a very fast frequency-switching synthesizer.

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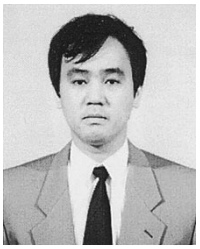
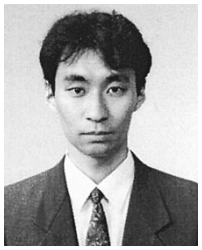


Akihiro Yamagishi was born in Toyama, Japan, in 1964. He received the B.E. and M.E. degree in electrical engineering from Toyama University, Toyama, Japan, in 1986 and 1988, respectively.

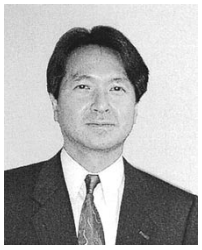
In 1988, he joined NTT LSI Laboratories, Kanagawa, Japan, where he was engaged in the research and development of frequency synthesizers IC's. He is currently a Research Engineer at NTT Telecommunications Energy Laboratories, Kanagawa, Japan, where he is engaged in the research and development of large-scale integrations (LSI's) for communication systems.



Hideyuki Nosaka (M'97) was born in Kanagawa, Japan, on March 4, 1971. He received the B.S. and M.S. degrees in physics from Keio University, Kanagawa, Japan, in 1993 and 1995, respectively.

In 1995, he joined NTT Wireless Systems Laboratories, Yokosuka, Japan, where he was engaged in the research and development of monolithic microwave integrated circuits (MMIC's) and frequency synthesizers. Since 1999, he has been engaged in research and development of InP-based IC's and module design for optical communication at NTT Photonics Laboratories, Kanagawa, Japan.

Mr. Nosaka is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.



Masahiro Muraguchi (S'81–M'81) was born in Kanazawa, Japan, in 1955. He received the B.S. degree in electrical engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1978, and the M.S. and Ph.D. degrees in physical electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1980 and 1983, respectively.

In 1983, he joined the NTT Atsugi Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, where he was involved in the design and fabrication of GaAs MMIC's. From 1987 to 1999, he was with NTT Wireless Systems Laboratories, Yokosuka, Japan, where he was engaged in research and development work on MMIC's for wireless communication systems. In 1999, he temporarily transferred to the NTT Electronics Corporation, where he is currently the Sales Department Director of the Ultra-High-Speed Electronics Group. His current research interests include high-speed electronics and optoelectronic devices for optical fiber communications.

Dr. Muraguchi is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He received the 1994 Ichimura Award for outstanding contribution to MMIC technology.

Tsuneo Tsukahara (M'92) was born in Fukushima, Japan, in 1956. He received the B.S. and M.S. degrees in applied physics from Tohoku University, Sendai, Japan, in 1979 and 1981, respectively.

In 1981 he joined the Electrical Communications Laboratories, Nippon Telegraph and Telephone Public Corporation (NTT), Tokyo, Japan, where he has been involved with device noise analysis and analog IC's design, especially, for high-performance A/D and D/A converters. He is currently a Leader of the RF Circuit Applications Research Group at the NTT Telecommunications Energy Laboratories, Kanagawa, Japan. His current interests are in low-power and high-performance wireless communications LSI's and low-voltage circuit techniques.

Mr. Tsukahara is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan, and the Institute of Electrical Engineer of Japan (IEEJ).