# System Demonstration of a Multigigabit Network Switch

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***Abstract*—A 4 × 4 single-flux-quantum (SFQ) network switch has been packaged and successfully demonstrated in a hybrid closed-cycle refrigerator (CCR) system at multigigabit data rates. Full operation of the packaged switch, with self-routing of 4-Gb/s data packets, was demonstrated using a 1-GHz address header decode. The switch is packaged on a superconducting multichip module (MCM) mounted on the 4.5-K stage of the CCR. On-chip asynchronous Josephson drivers and cooled GaAs preamplifers are used to amplify the SFQ outputs of the switch. The maximum operation bandwidth of the switch is currently limited by the asynchronous Josephson driver. New designs of the Josephson drivers, which have demonstrated operation at 10 Gb/s, are expected to enable switch operation at 10 Gb/s. The system is equipped with fiber-optical inputs and high-speed cryogenic photodetectors. The fiber-optic interfaces, RF packaging, and MCM packaging in the CCR system have demonstrated error-free operation at 10 Gb/s.**

***Index Terms*—Hybrid technology switch, multigigahertz switch, network switch, single-flux-quantum circuits, superconducting switch.**

## I. Introduction

THE communication bandwidth in fiber-optical network backbones continues to increase due to increasing user demand, processor speed, and integration of broad-band services. Ultrahigh bit-rate electronics is needed to route digital information in the high-speed optical layers of future communication networks. Currently, the optical layers are only used for point-to-point transmission, and the switching is done in the slower electrical layers of the network. Ultrahigh-speed optical packet-switched networks have been proposed [1], but are limited by the primitive state of optical processing and the bandwidth limitation of advanced semiconductor technologies.

Superconductive single-flux-quantum (SFQ) technology can offer data rates unattainable by advanced semiconductor technologies [2] and complex functionality—such as synchronization, serial memory, contention resolution, and address decoding—which is beyond the reach of optical processing in the foreseeable future. In addition to high-speed and ultra-low power dissipation, SFQ electronics offers the unique advantage of instantaneous clock recovery [3] at high data rate, which is unattainable by advanced semiconductor or optical technologies. SFQ packet switches with optical interfaces can dramatically increase the functionality and capacity of the optical layers in future ultrahigh-speed networks.

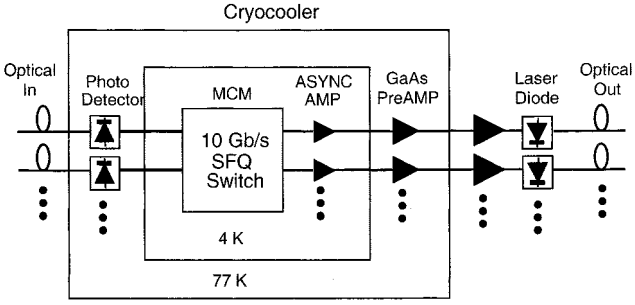


Fig. 1. Block diagram of switch demonstration system.

The network switch presented here was developed for a U.S. Department of Commerce Advanced Technology Program (ATP) joint venture formed by Conductus Inc., Sunnyvale, CA, TRW, Redondo Beach, CA, University of California at Berkeley, and Stanford University, Stanford, CA, and was administered by the U.S. National Institute of Standards and Technology (NIST), Boulder, CO, and benefited from technical input from NIST. This project focused on development of a hybrid digital communications system using the complementary advanced technologies of superconductor SFQ electronics, cryogenic semiconductor amplifiers and optoelectronic components, and fiber optics. The goal of final demonstration system for this project was a 10-Gb/s multichannel switch, packaged in a closed-cycle refrigeration system. A block diagram of the system is shown in Fig. 1. The data enter the system on optical fibers and are converted to electrical signals by cryogenic photodetectors at 80 K. They are transmitted to the switch via the multichip module (MCM) at 5 K and are routed by the switch to the appropriate output channel. The SFQ output of the switch (a few hundred microvolts) is then amplified to a voltage level of 2–5 mV by the on-chip Josephson junction (JJ) drivers, and is further amplified by the cooled low-noise GaAs amplifiers at 80 K. Further amplification can be used at room temperature to drive the laser diodes or to provide input to an error detector or sampling oscilloscope.

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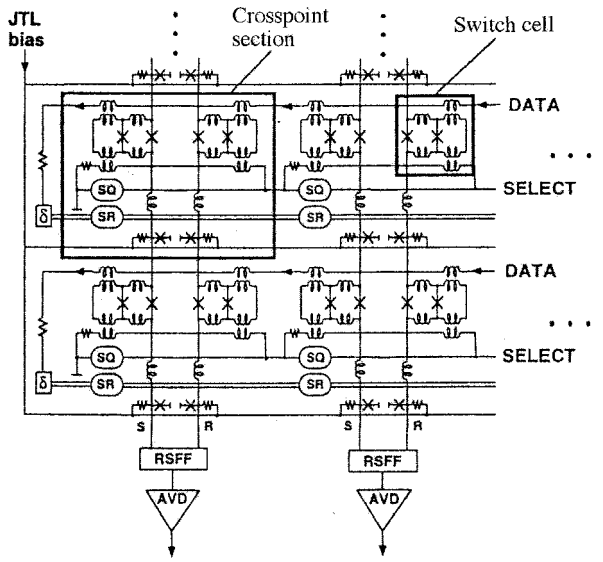


Fig. 2. Representative $2 \times 2$ corner of the switch. The $SR$ block represents 1 bit of the shift register, $SQ$ is a two-junction readout SQUID inductively coupled to $SR$, and $\delta$ is a clocked comparator used for the shift register input.

## II. Josephson Circuits

### A. SFQ Switch

The $4 \times 4$ SFQ switch was implemented in the standard HYPRES niobium foundry process with junction critical current density of 1 kA/cm$^2$.[1] The $2 \times 2$ corner section of the SFQ switch shown in Fig. 2 has a hybrid crossbar architecture with microstrip transmission-line input rows, Josephson transmission-line (JTL) output columns, and RF-superconducting quantum interference device (SQUID)-based switch cells located at each crosspoint. The address is decoded by means of SFQ shift registers integrated into each row of the switch matrix. For an $n \times n$ switch, the data format consists of an $n$-bit address header followed by a variable-length data packet. The address and data timings are defined by an external select signal and are shown in Fig. 3. The address header is clocked into the shift register to select the appropriate channel for data transmission. Once the output channel is selected, the input data entering the rows are inductively coupled to the switch cells and are transmitted down the selected columns as SFQ pulses. Data transmission though the switch is asynchronous, which allows nonreturn to zero (NRZ) or return to zero (RZ) data format, and different data and address clock rates. Furthermore, different input channels can support different clock rates for asynchronous applications. A detailed description of the switch design and operation is provided in [4]. (In subsequent unpublished work at TRW, a path through a $16 \times 16$ version of the switch fabricated with a junction critical current density of 2 kA/cm$^2$ was demonstrated at 8 Gb/s on a test probe in a Dewar.)

[1]Foundry service is available from HYPRES Inc., Elmsford, NY. Design rules available via HYPRES home page. [Online]. Available: http://www.hypres.com

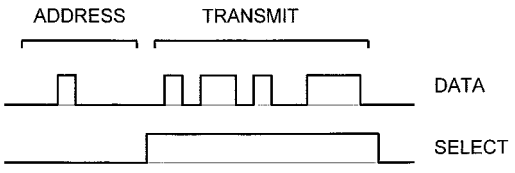


Fig. 3. Input select, address, and data signals for the switch.

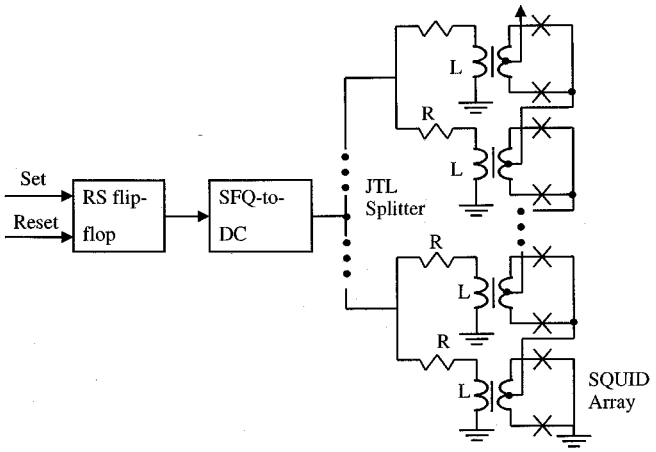


Fig. 4. Asynchronous output driver with 24 series resistively shunted SQUID's providing the output voltage of a few millivolts.

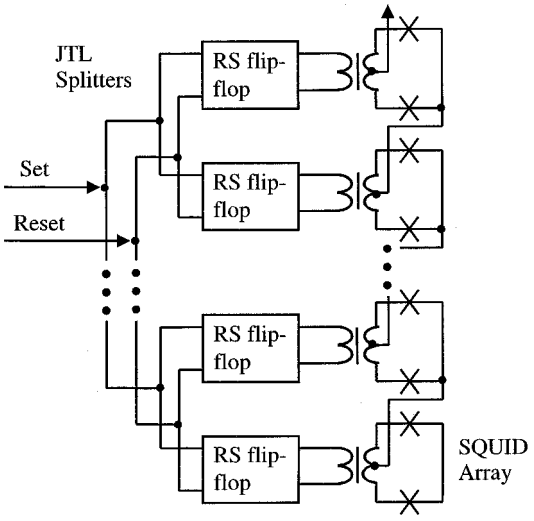


Fig. 5. Modified version of the asynchronous output driver.

### B. Asynchronous Josephson Driver

Asynchronous Josephson drivers, designed by HYPRES, are integrated with the $4 \times 4$ switch chip. These drivers are dc powered, and consist of a set/reset (RS) flip-flop, SFQ/dc converter, and JTL splitter coupled to an output array of SQUID's, as shown in the diagram in Fig. 4 [5]. There is a total of 24 SQUID's in series for the output. The SFQ/dc converter produces multiple-fluxon voltage pulses with average amplitude of 250 $\mu$V, and duration much longer than that of the individual SFQ pulse. This signal is distributed via the JTL splitter to the output SQUID array, which produces a 2–5 mV (chip-to-chip)

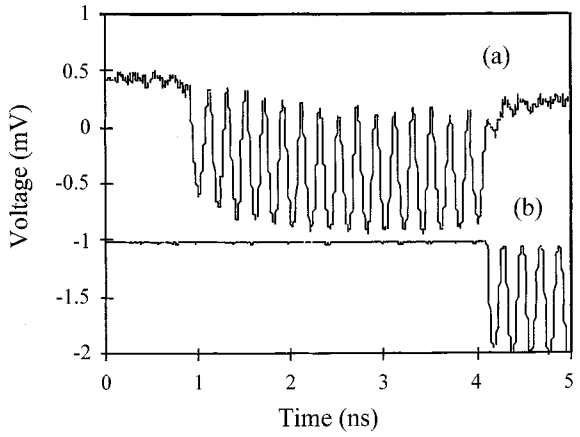


Fig. 6. Measurement of modified Josephson driver at 10 Gb/s. (a) Driver output for a 0 001 010, $\cdots$, 101 000 input pattern at 10-Gb/s data rate. (b) Input pattern with time offset.

signal. The bandwidth of these driver circuits, implemented in 1 kA/cm$^2$ niobium technology, is limited to about 4 Gb/s of NRZ data, which limits the maximum bandwidth of the test results presented in Section IV. When implemented in 2.5-kA/cm$^2$ technology, the bandwidth of this driver increased to 8 Gb/s with the same output voltage of 2–5 mV.

The primary factors limiting the speed of these drivers were found to be: 1) the L/R delay produced by the superconducting transformers between the JTL splitter and the SQUID's and 2) fluxon repulsion within the JTL splitter, which causes broadening and lowering of the average voltage pulses. To solve these problems, we designed a new driver using a dual SFQ splitter for the set and reset quanta, which are distributed to an array of RS flip-flops (see Fig. 5). Each RS flip-flop is inductively coupled to a SQUID in the output array. The set and reset splitters are designed to provide equal SFQ propagation delay from the input to each RS flip-flop. This driver was successfully tested in a dipping probe for NRZ data rate up to 10 Gb/s with 1.2-mV output, as shown in Fig. 6. The new driver was implemented in the standard 1-kA/cm$^2$ HYPRES process. The measured rise and fall times were about 35 ps, which is also the limit of our pattern generator and test probe. Additional development, such as fabrication with high-$J_c$ junctions, is needed for this application because the voltage level is inadequate for low bit-error-rate amplification by the cryogenic semiconductor amplifiers (several-millivolt signals are needed).

## III. System Packaging

The superconductor and semiconductor cryoelectronic components are packaged in a hybrid vacuum system utilizing the 4.5- and 80-K temperature stages of a Boreas B100 closed-cycle refrigerator.[2] The packaging is shown schematically in Fig. 7. The system includes 24 high-speed coaxial I/O lines, each with 18-GHz bandwidth, and two fiber-optical inputs to the 80-K stage. Multilevel magnetic shielding is used to shield the Josephson circuits from the earth's ambient field and the magnetic field generated by the cryocooler. The magnetic field at the location of the SFQ switch is about 1 mG.

[2]Boreas was a division of HYPRES Inc., Emsford, NY.

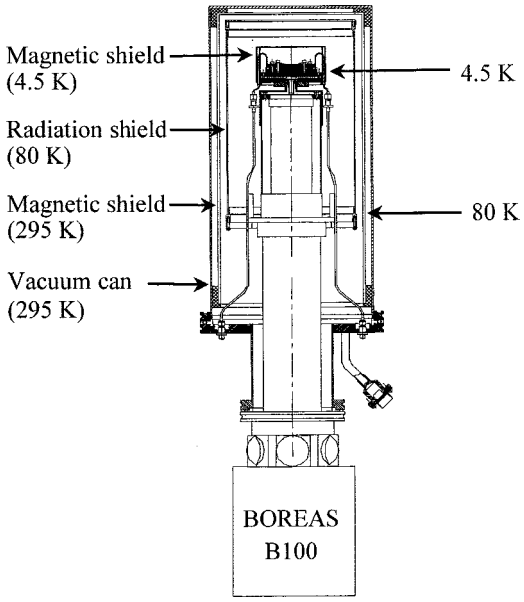


Fig. 7. Switch mounting, cooling, and shielding on the cold head of a Boreas B100 refrigerator.

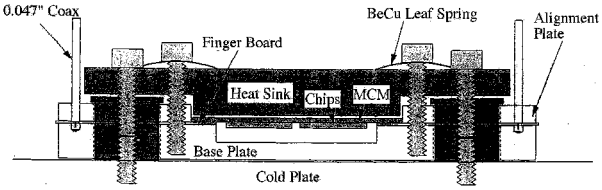


Fig. 8. Mounting structure for the sample holder.

### A. Cryogenic and MCM Packaging at 5 K

The Josephson circuits are packaged on a high-bandwidth superconducting MCM. The 5 mm $\times$ 5 mm circuit chips are flip-chip bonded onto the 1.25 in $\times$ 1.25 in MCM using a low-temperature solder-bump technique, which enables low-inductance and high-bandwidth contacts [6]. The 100-$\mu$m round pads in the Nb wiring on the MCM and on the chip each comprise 35 nm of Ti as an adhesion/barrier layer, 400 nm of Pd as the solder-contact layer, and 50 nm of Au to prevent oxidation of the Pd. The solder is InSn, which reflows at 118 °C. After reflow, the solder bumps collapse to a height of 5–7 $\mu$m. The shortness of the connection plays an important role in minimizing the parasitic inductance of the connection [7]. Simple electromagnetic modeling predicts the connection inductance is less than 10 pH, a value suitable for 10-Gb/s pulse propagation with good matching.

The MCM is mounted in a high-speed 72-pin sample holder using beryllium copper spring-contact fingers.[3] The mounting structure for the sample holder, which is contained within the magnetic shield at the top of refrigerator in Fig. 7, is shown in Fig. 8. Careful thermal design and several incremental improvements were necessary to provide sufficient thermal conductivity between the 4.5-K stage and the mounted circuit chips, to compensate for the heat carried to the sample holder and MCM by

[3]High Precision Devices Inc., Boulder, CO.

TABLE I
CRYOGENIC OPTICAL AND ELECTRONIC COMPONENTS

| Device | Parameter | Room temperature Performance | 77 K performance |
|---|---|---|---|
| Photodetector (fiber packaged) | Dark current | 1 mA | 0.4 mA |
| | Bandwidth | 12 GHz | 14 GHz |
| Laser diode (fiber packaged) | Bandwidth | 12 GHz | 14 GHz |
| | Threshold | | $> 2 \times$ lower than at 300 K |
| GaAs amplifier (packaged) | Noise figure | 6.4 dB | 3.9 dB |
| | Bandwidth | 12 GHz | 15 GHz |

the high-speed lines. Silver paste was used to attach the back of the MCM to a copper heat sink, which is in good thermal contact with the 4.5-K stage. An additional cooling path was provided directly to the mounted chips via a copper link to the 4.5-K temperature stage. The temperature difference between the circuit chip and the 4.5-K stage is about 0.5 K, which is low enough to enable full operation of the niobium Josephson circuits with good margins.

### *B. RF Performance*

Error-free operation ($\mathrm{BER} < 10^{-12}$ confirmed using two different BER test systems: Hewlett-Packard and Anritsu) at 10 Gb/s was demonstrated for a passive two-way path through the I/O coaxial lines, the high-speed sample holder, microstrip lines on the MCM with solder-bump contacts, and a coplanar transmission line on a mounted chip. Fig. 9 shows the clean 10-Gb/s pseudorandom bit sequence (PRBS) eye diagram obtained, with greater than 30% eye openings. A time-domain reflection (TDR) measurement verified than the impedance at all points in the transmission path was within 4 $\Omega$ of the designed 50-$\Omega$ characteristic impedance. The insertion loss at 10 Gb/s is 5 dB for the two-way path, or 2.5 dB from the coaxial input at room temperature to the mounted niobium chip at 5 K.

### *C. Optical Interfaces*

The optical interfaces use commercial 10-Gb/s laser diodes and photodetectors packaged with single-mode optical fiber.[4] The laser diode and photodetector packages have been successfully tested in vacuum at 10 Gb/s for cryogenic temperatures down to 77 K. The photodetectors are mounted on the

[4]Lasertron, Burlington, MA 01803 (laser diode model #QLM3S900-002 and photodetector model #QDMH-1).

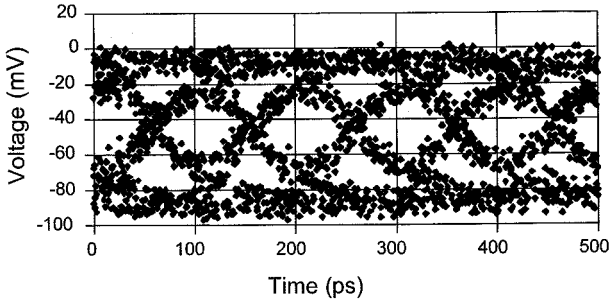


Fig. 9. Eye diagram of 10-Gb/s PRBS pattern transmission through a niobium chip mounted on an MCM in the CCR.

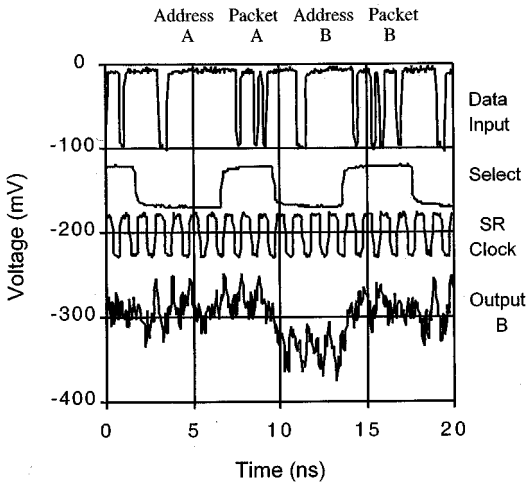


Fig. 10. Measurement of $4 \times 4$ switch for 4-Gb/s data rate and 1-GHz address clock packaged on an MCM in the CCR system.

80 K stage of the closed-cycle refrigerator (CCR), and have lower dark current and higher sensitivity when cooled. Cooled 10-Gb/s GaAs preamplifiers[5] are used on the 80-K stage of the CCR to amplify the output signals. Table I shows the room temperature and 77-K performance of the optoelectronic devices and the amplifier. It is seen there, for example, that the noise figure of these amplifiers improves from 6.4 dB at room temperature to 3.9 dB at 77 K. Additional amplification is provided using low-noise 10-Gb/s room-temperature amplifiers.[6] Although the laser diodes demonstrate a 20% improvement in bandwidth when cooled, the additional amplification required to drive the laser dissipates too much power to justify operation of the laser diodes on an 80-K stage. The optical interfaces in the CCR have been operated up to 8 Gb/s.

## IV. Demonstration of Switch in CCR at 4 Gb/s

The $4 \times 4$ switch, mounted on an MCM, was successfully measured in the CCR system for data rate up to 4 Gb/s with a 1-GHz address clock. The chip temperature is estimated at 5 K. The measurement results are shown in Fig. 10. The input consists of 4-Gb/s data packets preceded by address headers. The output shows data packet $B$ being successfully routed to output channel $B$. A cooled preamplifier, with 11-dB gain is used at the 80-K stage. The low signal-to-noise ratio in the output signal is due to the lower than expected output of the on-chip Josephson driver, which also limits the bandwidth of this measurement to 4 Gb/s. As pointed out in Section II-B, a redesign of the output driver increased its output.

## V. Conclusions

Almost all passive and active electronic devices exhibit improved performance at low temperature. The goal of this ATP joint-venture program was to demonstrate the unique capabilities of superconductor electronics when integrated with cooled conventional electronics in a high-speed cryoelectronic communication system. In the process of this development, various electronic devices and components were optimized for operation at low temperature, and tested at high data rate, some of which represent record performance as follows:

| | |
|---|---|
| superconducting switch | 8 Gb/s; |
| superconducting amplifier | 10 Gb/s; |
| MCM | 10 Gb/s (test equipment limited); |
| laser diode (80 K) | 30 Gb/s; |
| photodetector (80 K) | 20 Gb/s; |
| gallium–arsenide amplifier (80 K) | 12 Gb/s; |
| RF packaging (refrigerator I/O) | 10 Gb/s (test equipment limited). |

Note that not all of these components were integrated into the final system, due to scheduling and packaging limitations.

The superconducting switch demonstrated successful data transmission at 8 Gb/s, which we believe was limited by the 2.5-kA/cm$^2$ driver circuit. However, due to integration and testing limitations, the full functionality of the switch could only be demonstrated up to a data rate of 4 Gb/s. An improved driver design in 1-kA/cm$^2$ technology, using an array of RS flip-flops, demonstrated operation at 10 Gb/s. With an input signal of only 200 $\mu$V, and input referred noise of about 10 $\mu$V, this may represent the most sensitive 10-Gb/s amplifier demonstrated.

The MCM test at 10 Gb/s included transmission of the data through two solder-bumps (I/Os) attaching a flipped chip. The cooled laser measurement gave the highest bandwidth reported at that time, and the cooled detector demonstrated a dark current orders of magnitude better than at room temperature.

Two system tests were performed. The first was an electrical test that included the SFQ switch on the MCM with an amplifier output. The complete demonstration system included MCM packaging, cryogenic semiconductor amplifiers and optoelectronic components, fiber-optical interfaces, and RF packaging, all mounted in the CCR. Packet-switching operation for data rate up to 4 Gb/s was demonstrated with a 1-GHz address clock.

Further improvement and integration are required to transform this demonstration vehicle to a useful network switch. Contention resolution and other network protocol functions should be added. The size and speed of the switch can also be increased. The new Josephson driver circuit, demonstrated at 10 Gb/s, is expected to enable operation of the switch at this data rate if fabricated in a higher current density fabrication process. TRW successfully demonstrated operation of both $8 \times 8$ and $16 \times 16$ switches with architecture identical to that of the $4 \times 4$ switch, which would enable a data throughput of up to 160 Gb/s with 10-Gb/s per channel.

## Acknowledgment

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[5]Picosecond Pulse Laboratories, Boulder, CO (model #5830).

[6]Anritsu America, Rochelle Park, NJ. (model #A3HB3102).

## References

[1] D. Cotter, J. K. Lucek, and D. D. Marcenac, "Ultra-high-bit-rate networking: From the transcontinental backbone to the desktop," *IEEE Commun. Mag.*, vol. 35, pp. 90–95, Apr. 1997.

[2] K. K. Likharev, "Ultra-fast superconductor digital electronics: RSFQ technology roadmap," in *Proc. 21st Int. Low-Temperature Phys. Conf.*, vol. 6, Aug. 1996, p. 3331.

[3] V. Kaplunenko, V. V. Borzenets, N. B. Dubash, and T. Van Duzer, "Superconducting single flux quantum 20 Gb/s clock recovery circuit," *Appl. Phys. Lett.*, vol. 71, pp. 128–130, July 1997.

[4] N. B. Dubash, P. F. Yuh, V. V. Borzenets, T. Van Duzer, and S. R. Whiteley, "SFQ data communication switch," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 2681–2684, June 1997.

[5] O. A. Mukhanov, S. V. Rylov, D. V. Gaidarenko, N. B. Dubash, and V. V. Borzenets, "Josephson output interfaces for RSFQ circuits," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 28–26, June 1997.

[6] K. E. Yokoyama, G. Akerling, A. D. Smith, and M. Wire, "Robust superconducting die attach process," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 2631–2634, June 1997.
[7] J. J. Licari, *Multichip Module Design, Fabrication, & Testing*. New York: McGraw-Hill, 1955.

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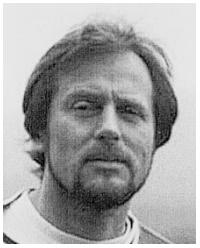
In 1994, he joined Conductus Inc., Sunnyvale, VA, where he is involved in cyroelectronic circuits and systems for high-speed digital communications. His technical work at Conductus Inc. has included rapid-single-flux-quantum (RSFQ) integrated-circuit (IC) design, crossbar switches, cryo-CMOS, fiber-optical interfaces, high bit-rate testing, network switching, clock recovery, and high-temperature superconductor (HTS) wireless filter design. As Manager of digital circuit development, he lead Conductus's effort in the development and commercialization of high-speed superconducting systems for ultrafast data switching and digital communications. In the fall of 1998, he joined SiRF Technology Inc., where he is involved with radio-frequency integrated-circuit (RFIC) design for low-power global positioning system (GPS) receivers in high-bandwidth biplolar, BiCMOS and RF CMOS technologies.

Dr. Dubash is a member of the IEEE Solid-State Circuits Society and the IEEE Microwave Theory and Techniques Society.



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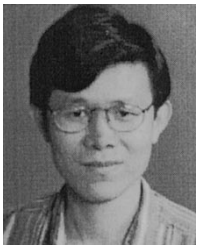

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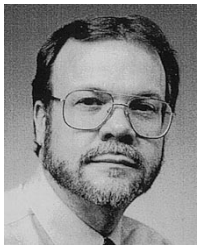
Since joining Conductus Inc., Sunnyvale, CA, in 1995, he has been involved with the development of cryogenic fiber-optic components/links for high-speed data communications, and on the development of HTS and low-temperature superconductor (LTS) devices and application-specific integrated circuits (ASIC's). Collaborating with the Optoelectronics Group at the University of California at Santa Barbara, he has been leading the effort on the development of cryogenic InP/GaAsIn high-speed photodetectors and long-wavelength vertical cavity lasers. In collaboration with the University of California at Berkeley, Stanford University, Hypres Inc., and the Electronics and Technology Division, TWR, he has designed and tested advanced LTS and HTS digital circuits for high-speed communication and instrumentation applications, based on both the RSFQ logic family and long junction logic family. He has invented several novel circuits by combining long JJ's with RSFQ circuits. He has also been involved in the design of microwave low-noise amplifiers, modeling of advanced microwave filter systems, and mobile communication system. Recently, he has been involved in the development of ferroelectric microwave material and devices. Before joining Conductus Inc., he was with the Chalmers University of Technology, where he was involved in high-frequency properties and applications of LTS and HTS devices and circuits, especially the flux-flow three-terminal devices. He designed, fabricated, and measured the first integrated superconducting receiver for the linewidth measurement of flux-flow Josephson oscillators in the band of 280–330 GHz. He demonstrated the first HTS flux-flow long junction transistor with current gain larger than one. He also observed Fiske and Eck resonances in HTS bicrystal junctions, which contributed to the understanding of the tunneling nature for HTS junctions.

Dr. Zhang was the recipient of the 1994 SAAB-Scania Award for the best Ph.D. dissertation in electronics. He has also been the recipient of several U.S. Government Small Business Initiative Research (SBIR) grants.

**Vsevolod Kaplunenko** received the Ph.D. degree from the Institute of Solid State Physics, Russian Academy of Science, Chernogolovka, Moscow district, Russian, in 1986, and the M.S. in physics of metals at the Moscow Institute of Steel and Alloys, Moscow, Russia, in 1980.

He is currently a Member of the Technical Staff at Conductus Inc., Sunnyvale, CA. Since 1988, he has designed and tested superconducting digital circuits based on the RSFQ logic family. During this time, he has enhanced the circuit design and simulation capabilities (see http://home.pacbell.net/kapl). At Conductus Inc., he has developed novel RSFQ circuits for communication applications. Before joining Conductus Inc., he was a Guest Researcher at the Chalmers University of Technology, Göteborg, Sweden, and the Technical University of Denmark, Lyngby, Denmark, from 1993 to 1996. He was a Senior Researcher at the Institute of Radio Engineering and Electronics, Russian Academy, from 1986 to 1993. He possesses over 12 years experience in the physics and technology of superconducting electronics and has authored or co-authored over 35 papers in this field.

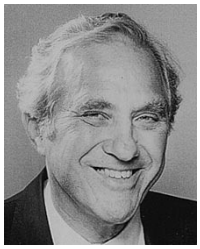


**John W. Spargo** (S'76–M'98) received the B.A. degree in physics and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley, in 1974, 1981, and 1983, respectively.

From 1983 to 1990, he led project activity in superconducting JJ microelectronics research at Hughes Technology Center, within Hughes Aircraft. While there, he was involved in NbN-based Josephson circuit process development , NbN-based A/D circuits, dc SQUID circuits, and SQUID arrays, as well as laser-deposited YBCO granular weak-link devices, and the use of buffer layers to improve the superconducting properties of YBCO films. In 1990, he joined TRW Space and Electronics, Redondo Beach, CA. He is currently Manager of the Superconductor Electronics Organization, Electronics and Technology Division, where he manages research and development in the area of HTS and LTS integrated circuit processing and superconductive electronics for space- and ground-based applications. His research activities include HTS and LTS integrated circuits for analog and digital applications for space- and ground-based systems, telecommunications, and high-performance digital computing. The accomplishments of the TRW effort include the only multilayer HTS IC process on full 2-in wafers, the only 10-K operating temperature superconductor IC foundry capability, demonstration of a 2.5-Gb/s 16 $\times$ 16 switch and demonstration of MCM and flip-chip packaging for high-bandwidth applications of superconductor electronics.

Dr. Spargo is a member of the Board of Directors of the Applied Superconductivity Conference and a past chair and current member of the Organizing Committee of the Workshop on Josephson Devices, Circuits, and Systems. He is serves on the IEEE Applied Superconductivity Council and is an Associate Editor for electronic applications for the IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY. He was the 1997 recipient of the TRW Independent Research and Development Award.

**A. D. Smith**, photograph and biography not available at time of publication.



**Theodore Van Duzer** (S'52–A'54–M'60–SM'75–F'77–LF'93) received the Ph.D. degree from the University of California at Berkeley, in 1960.

Since 1961, he has been on the University of California at Berkeley faculty as a member of the Department of Electrical Engineering and Computer Sciences. He is currently a Professor in the Graduate School. He has co-authored two textbooks *Principles of Superconductive Devices and Circuits and Fields, 2nd Edition* (Upper Saddle River, NJ: Prentice-Hall, 1999) and *Waves in Communication Electronics, 3rd Edition* (New York: Wiley, 1994), and has authored and co-authored numerous research literature on superconductor electronics. His current research interests focus on Josephson devices and on multigigahertz digital superconductor circuits, including hybrids with cryogenic semiconductor components.

Dr. Van Duzer is a member of the U.S. National Academy of Engineering. He is founding Editor-in-Chief of the IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY.