Generic-Device Frequency-Multiplier Analysis—A Unified Approach

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***Abstract*—In this paper, a unified generic FET frequency multiplier theory is developed. The predictions of this approach are consistent with previously published results, but this theory is valid for an extended set of bias/drive regimes of operation. The model can be applied in the cases of both single- and double-sided current clipping. The model predictions are presented as contour plots. These provide a general summary of the harmonic generation characteristics of a generic device, and the optimum bias and drive conditions. For a frequency doubler, 15% more second harmonic power than that indicated by a conventional analysis is predicted for the optimum configuration. For a frequency tripler, an alternative biasing condition is proposed, which yields interesting advantages over previously published approaches. The predictions of the unified generic approach are shown to be consistent with the corresponding contour plots for a specific device, as determined from a numerical Fourier analysis of its current waveform as given by a nonlinear device model. The trend in measured conversion efficiency versus input power for a fabricated GaAs monolithic-microwave integrated-circuit C frequency tripler, with an output at 56 GHz, is compared with the predictions of the generic and device-specific models, with acceptable agreement being achieved.**

***Index Terms*—Frequency conversion, harmonic analysis, MMIC, MIMIC, MESFET, HEMT.**

I. Introduction

A LARGE volume of work has been published on the topic of MESFET-type frequency multipliers. Both theoretical [1], [2] and experimental [3]–[6] studies have been presented. The general inference from theoretical work (that MESFET/high electron-mobility transistor (HEMT) devices are primarily suited to doubler and (to a lesser extent) tripler applications), has been largely borne out by experimental findings. The complexity of the expressions used to model the drain current dependence in the theoretical analyses has varied significantly. Gopinath *et al.* [1] utilized a detailed $I_{\rm ds}$ model, which facilitated a study of the influence of various aspects of the nonlinear device on its multiplying behavior, Maas [2], on the other hand, applied a generic piecewise linear transconductance (PLT) (g_m) model, where $I_{\rm ds}$ clipping effects only are considered, to develop generalized multiplier biasing and drive criteria. Maas' approach is consistent with the findings of [1], in which the $I_{\rm ds}$ clipping contribution is the most significant factor affecting harmonic generation.

However, recent developments [7] have demonstrated an alternative tripler-bias arrangement, which has the potential to perform significantly better than would be predicted by the earlier theoretical models. This improvement has been explained analytically (using the PLT model), but it has not been shown conclusively whether it is the true optimum or whether further improvements are yet possible. Moreover, it also casts some doubt on the conclusions drawn regarding frequency doublers in the conventional analysis.

In this paper, we endeavor to combine the best of the Gopinath *et al.* and Maas techniques. The goal has been to study and, if necessary, refine the multiplier design criteria of Maas by applying the PLT model in a more generalized and more extensive harmonic analysis. The criteria for third harmonic optimization will be compared with the findings of Fudem *et al.* [7]. The application of the PLT model facilitates a good fundamental understanding of the key parameters influencing the harmonic conversion capability of an FET device. In order to take real device characteristics into account, the Angelov device model [8] will be used to assess the validity of the design criteria derived using the PLT model.

Finally, despite the fact that the primary value of this paper is the intuitive insight it provides, and not quantitative results, model validation is carried out for a fabricated GaAs monolithic-microwave integrated-circuit (MMIC) frequency tripler with an output at 56 GHz. The measured conversion efficiency versus input power characteristic for this circuit is compared with the predictions of both the PLT and device-specific (Angelov) models, with acceptable agreement being achieved.

II. Review of Published Analyses

A. Gopinath et al.

Gopinath *et al.* [1] concentrated on frequency doublers in particular, and derived a number of conversion efficiency values based on a specific $I_{\rm ds}$ model. The strategy used was to study the contribution to second harmonic generation of the main nonlinear factors involved, including $C_{\rm gs}$ nonlinearity, $I_{\rm ds}$ clipping, and the $V_{\rm gs}$–$I_{\rm ds}$ transfer characteristic. A key finding was that $I_{\rm ds}$ clipping is the primary contributor to second harmonic generation.

Gopinath *et al.* also conclude that the optimum bias point for doubler operation is either near pinchoff or else near gate forward conduction. In both cases, the resultant waveform clipping leads to significant harmonic generation.

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B. Maas

Mass [2] approached this subject in a more fundamental manner by making the assumption that g_m is piecewise linear. The only nonlinear effect considered is $I_{\rm ds}$ clipping. This PLT model is not strictly valid for a MESFET (and even less so for an HEMT due to the g_m peaking caused by a neutral region developing in the doped wide-bandgap material as the gate bias is increased), but nevertheless is very useful in providing an insight into the principal sources of harmonic generation and in developing a first-order estimate of the optimum drive/biasing combination.

Maas also assumes that only pinchoff-based clipping occurs, and that forward conduction effects are avoided. On this basis, a Fourier analysis is carried out, from which a set of harmonic coefficient curves is derived. In the analysis, Maas assumes that the nonlinear device is biased near pinchoff, and that drain current flows when the superposition of the bias and the applied ac signal brings the instantaneous gate voltage above pinchoff. The fraction of the full ac cycle for which current flows is referred to as the *aperture*, and this is determined by the gate bias and ac drive level. This mode of operation is essentially similar to that of a Class-C-type amplifier. The net result is that the drain current flows in distinct pulses, and Maas makes the further assumption that these individual pulses are themselves sinusoidal in shape (this sinusoid having the same period as the applied signal only for an *aperture* of 0.5). In this paper (Section III-A), a more exact analysis is presented, which shows that, in most practical cases, the sinusoidal pulse assumption is justified.

Based on the results of this analysis, it appears that the FET-type device is suitable for doubling and tripling requirements. For higher harmonic numbers, the conversion efficiencies appear poor.

C. Fudem and Niehenke

Fudem and Niehenke [7] have developed balanced active triplers based on a new biasing arrangement. Instead of adopting the Maas bias scheme, which would demand an aperture in the region of 0.23 (see Section III-A), they have instead opted for a bias point midway between pinchoff and the onset of forward conduction, consistent with a Class-A amplifier. Having thus biased the device, it is then over-driven by a large-amplitude ac signal, which drives the device both into pinchoff and into forward conduction every cycle. The resulting drain current waveform is severely clipped at both ends, thereby introducing harmonics. When driven hard, the current resembles a square wave. Among the interesting properties of an ideal square wave is the fact that it contains odd harmonics only of the fundamental. The Fourier analysis of the severely clipped waveform suggests that the maximum third harmonic content of the drain current, for a given device biased in Class-A mode, exceeds that which can be achieved with the same device when biased near pinchoff according to Maas' design criterion. Fudem and Niehenke have published measurements on functional balanced triplers biased in this way, thereby demonstrating the viability of this approach.

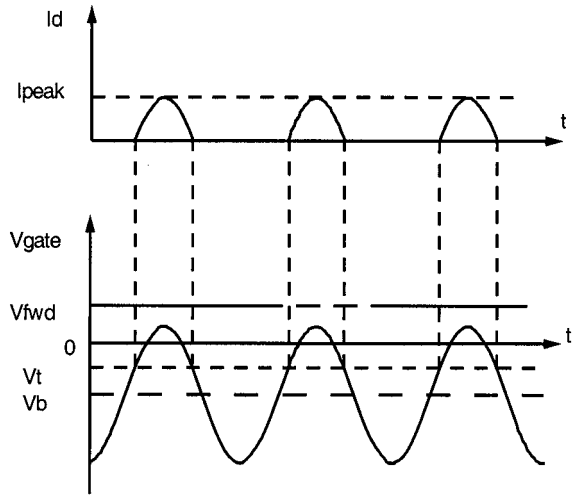


Fig. 1. Device waveforms for multiplier with pinchoff clipping.

III. New Generalized Approach

The conventional output of a theoretical FET frequency-multiplier analysis is a combination of gate bias and fundamental RF input gate levels for optimum generation of a given harmonic of the fundamental. Suitable input and output matching networks are then required to extract the available desired harmonic power, while at the same time rejecting the unwanted harmonics (including the fundamental). To a significant extent, these terminations are independent of the device, and are generally strongly dependent on the fundamental frequency involved (very often they consist of reactive shunt stubs, which present short circuits at the unwanted frequencies). These terminations do not contribute to the conversion performance as such, and the frequency conversion *capability* of the device can be assessed on the basis of ideal terminations.

A. Refinement of Maas Analysis

A simple representation of the gate voltage and drain current waveforms, associated with a device biased near pinchoff, is outlined in Fig. 1. The gate dc-bias voltage level is V_b, the threshold voltage is V_t, forward conduction commences at $V_{\rm fwd}$, and the peak value of the current pulses is $I_{\rm peak}$.

As outlined in Section II-B, the primary assumptions made by Maas are: 1) g_m is piecewise linear and 2) the drain current pulses are half-wave rectified sinusoids.

A straightforward analysis yields the following Fourier coefficients I_n for the drain current waveform in Fig. 1:

$$I_n = \frac{4I_{\rm peak}}{\pi}\,\frac{t_0}{T}\,\cos\left(\frac{n\pi t_0}{T}\right)\,\frac{1}{1-(2nt_0/T)^2} \qquad (1)$$

where t_0/T is the aperture. Using this result, Maas has developed a set of curves that trace the conversion efficiency to various harmonics as a function of the aperture value.

The above analysis is now modified, by the elimination of assumption 2) above. Instead, the current waveform is assumed to be a clipped sinusoid, proportional to that part of the gate

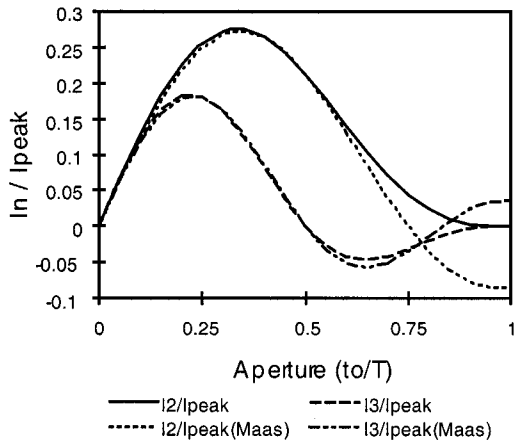


Fig. 2. Comparison between new and Maas model results.

voltage waveform that exceeds the threshold level. This is a more consistent application of the PLT characteristic. Using this approach, the refined Fourier coefficients are found to be

$$I_n = \frac{I_{\text{peak}}}{\pi}\left\{\frac{\sin\left([n-1]\pi t_0/T\right)}{n-1} + \frac{\sin\left([n+1]\pi t_0/T\right)}{n+1} - \frac{2}{n}\cos\left(\pi t_0/T\right)\sin\left(2\pi t_0/T\right)\right\} \quad (2)$$

for $n \neq 1$ and

$$I_1 = \frac{I_{\text{peak}}}{\pi}\left\{\frac{\pi t_0}{T} - \frac{\sin\left(2\pi t_0/T\right)}{2}\right\}. \quad (3)$$

A comparison between the conventional Maas analysis and the results obtained using our modified approach above is presented in Fig. 2. The results are presented as the harmonic current normalized to the peak current (I_{peak}) versus the aperture. Traces for the second and third harmonics only are presented. The results of the two analytical approaches are very similar, certainly up to an aperture value of about 0.5, which corresponds to the device being biased at V_t. For aperture values greater than 0.5, the results begin to diverge significantly. At an aperture value of 1.0, which corresponds to a drain current with a full sinusoidal waveform, the refined analysis yields zero harmonic current coefficients as expected, whereas the Maas model suggests nonzero values due to its assumption of half-sinusoidal pulses becoming increasingly invalid. In terms of multiplier efficiency and optimum aperture values for harmonic generation both analyses yield similar results.

B. Justification for a Generalized Theory

As a consequence of [7], where it has been shown that improved tripler conversion performance is possible by biasing the device differently to the "optimum" bias suggested by [2], the conclusions of Maas must be reconsidered. Maas' primary concern in opting for the pinchoff region for multiplier biasing was the avoidance of gate forward conduction, as this would introduce significant reliability concerns. Fudem and Niehenke, however, have demonstrated successful tripler operation with circuits in which the effects of forward conduction are exploited.

The analysis proposed by Fudem and Niehenke considers a device biased for Class-A-type operation. Consider a situation where the applied ac voltage becomes very large: this causes the current waveform to be severely clipped and an approximately square-waveform results. The Fourier terms associated with a perfect square wave are given by

$$I_n = \frac{2I_{\text{peak}}(-1)^n}{n\pi}, \qquad n \text{ odd}$$
$$I_n = 0, \qquad n \text{ even}. \quad (4)$$

This odd harmonic characteristic of a square wave was utilized by Fudem and Niehenke in their tripler designs. For a square wave, the amplitude of I_3 is approximately $0.212I_{\text{peak}}$. The corresponding value from the pinchoff clipping analysis (see Fig. 2) is approximately $0.183I_{\text{peak}}$.

With this in mind, a more generalized Fourier analysis needs to be carried out on the generic PLT device. This general analysis should allow for arbitrary bias and drive levels, and facilitate a study of the harmonic generation characteristics of a device operating with pinchoff clipping, forward conduction clipping, or both. Based on the results of this analysis, a contour analysis could be carried out whereby, at a glance, the optimum combinations of bias and drive could be estimated for conversion to a given harmonic.

The theoretical analysis of a multiplier with single-sided clipping has been discussed in Section III-A. In order to facilitate a generalized study, a Fourier analysis is also required for the situation in which double-sided clipping occurs.

C. Double-Sided Clipping Theory

Some of the key parameters used in the derivation of this extended model are shown in Fig. 3. In order that the results be as generic as possible, a form of normalization is applied. The gate voltage is normalized such that pinchoff effects are observed for values less than zero, and that forward conduction occurs for values greater than 1.0. In a manner similar to Maas, the Fourier current coefficients are normalized relative to the maximum drain current of the device. This differs subtly from [2], where Maas in fact normalized relative to the peak value of the given current pulse, rather than the maximum value that that peak could possibly attain when driven sufficiently hard. Both normalizations are equivalent when the forward conduction limit is just reached at the peak of the ac cycle.

Let the dc and ac gate voltages be V_b and V_{in}, and let the corresponding normalized voltages be V_{DC} and V_{AC}. The normalized values are derived from the actual values using the expressions

$$V_{\text{DC}} = \frac{V_b - V_t}{V_{\text{fwd}} - V_t} \quad (5)$$

$$V_{\text{AC}} = \frac{V_{\text{in}}}{V_{\text{fwd}} - V_t}. \quad (6)$$

Denote the actual gate bias voltage midway between V_t and V_{fwd} by V_{mid} ($= 0.5$ normalized).

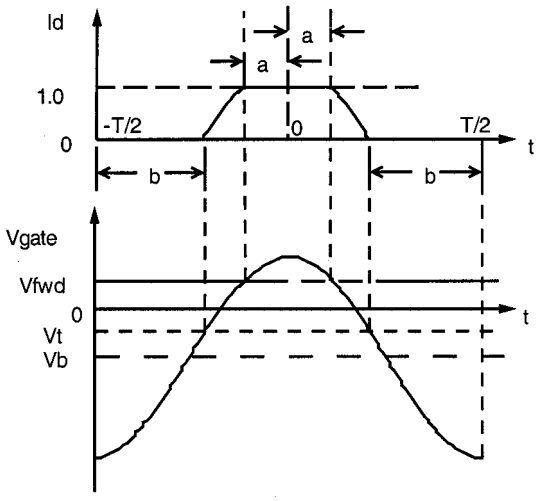


Fig. 3. Device waveforms for multiplier with double-sided clipping.

The clipping durations are given by (see Fig. 3)

$$V_{\rm AC}\cos(\omega a) = 1 - V_{\rm DC} \tag{7}$$

$$V_{\rm AC}\cos(\omega b) = V_{\rm DC}. \tag{8}$$

For a given $V_{\rm DC}$ and $V_{\rm AC}$, these equations can be solved for a and b. The normalized current waveform is then given by

$$i(t) = \begin{cases} 0, & -T/2 \le t \le -T/2 + b \\ V_{\rm DC} + V_{\rm AC}\cos(\omega t), & -T/2 + b \le t \le -a \\ 1, & -a \le t \le a \\ V_{\rm DC} + V_{\rm AC}\cos(\omega t), & a \le t \le T/2 - b \\ 0, & T/2 - b \le t \le T/2. \end{cases} \tag{9}$$

A Fourier analysis can then be carried out on the above waveform, yielding

$$\begin{aligned} I_n = {} & \frac{2V_{\rm DC}}{n\pi}\Big[(-1)^{n+1}\sin(n\omega b) - \sin(n\omega a)\Big] \\ & + \frac{V_{\rm AC}}{(n-1)\pi}\Big[(-1)^{n}\sin([n-1]\omega b) - \sin([n-1]\omega a)\Big] \\ & + \frac{V_{\rm AC}}{(n+1)\pi}\Big[(-1)^{n}\sin([n+1]\omega b) - \sin([n+1]\omega a)\Big] \\ & + \frac{2}{n\pi}\sin(n\omega a), \qquad n \ne 1. \end{aligned} \tag{10}$$

The fundamental component I_1 is given by

$$\begin{aligned} I_1 = {} & \frac{2V_{\rm DC}}{\pi}\Big[\sin(\omega b) - \sin(\omega a)\Big] + 2V_{\rm AC}\left[0.5 - \frac{a+b}{T}\right] \\ & + \frac{V_{\rm AC}}{2\pi}\Big[-\sin(\omega b) - \sin(\omega a)\Big] + \frac{2}{\pi}\sin(\omega a). \end{aligned} \tag{11}$$

D. Regimes of Bias/Drive Operation

For a given bias voltage and drive level, a number of distinct regimes of operation can now be identified; these regimes require the application of different analyses (corresponding to either Sections III-A or III-C) in the calculation of the appropriate Fourier coefficients. This situation is summarized in Fig. 4, where the symmetry of the clipping characteristic, with respect to the midpoint voltage, is exploited.

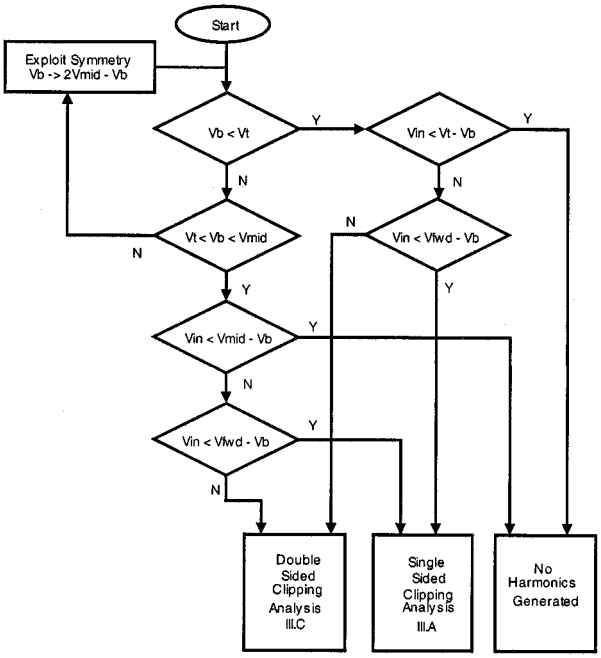


Fig. 4. Regimes of operation for multiplier analysis.

IV. Generic Unified Theory Results

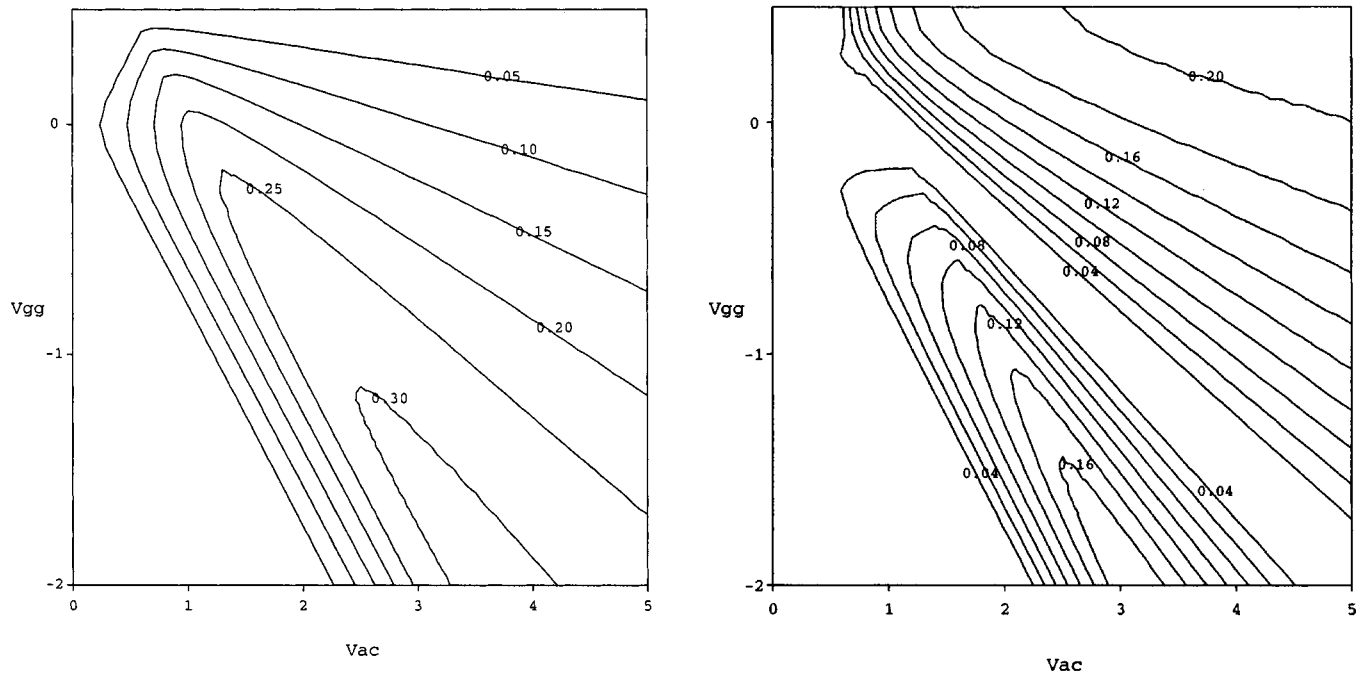
The unified theory described in Section III can be used to explore the full range of possibilities, in terms of the normalized bias and drive levels applied to an ideal PLT device, in order to assess the optimum combination for a given multiplier requirement.

The most useful analysis strategy comprises a full sweep of both variables with the calculation of normalized harmonic current coefficients over a matrix of bias and drive combinations. These results can then be studied via contour plots. These plots facilitate a rapid assessment of the trends in the multiplier characteristics as the input parameters are varied. The multiplier performance for the PLT device is symmetric about $V_{\rm mid}$ and, as a result, the contour plots developed for this generic device only depict the harmonic content for bias levels up to $V_{\rm mid}$.

Typical contour plots are presented in Figs. 5 and 6. In Fig. 5, the normalized second harmonic current coefficients are plotted; the normalized third harmonic current coefficients are plotted in Fig. 6. Some interesting observations can be made on studying these contour plots.

A. Generic Doubler

It can be shown that the optimum condition for second harmonic generation, based on the single-sided clipping analysis of Section III-A, is given in terms of the normalized voltages by $V_{\rm AC} = 2.0$, $V_{\rm DC} = -1.0$, with the corresponding value of I_2 being approximately 0.276. This results simultaneously in the optimum aperture value and the maximum peak of the drain



(a)

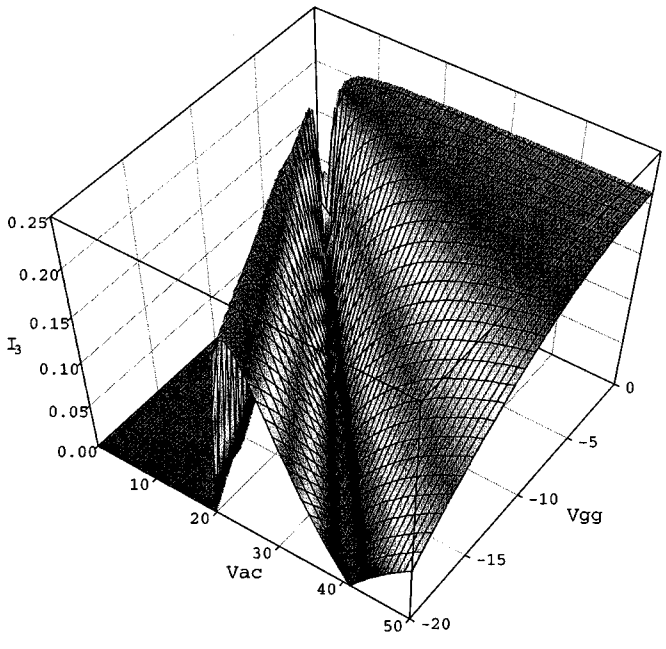
Fig. 5. Second harmonic contour plot (PLT).

current pulses, just prior to the onset of forward conduction. It is apparent from Fig. 5 that the value of I_2 continues to increase as $V_{\rm AC}$ increases beyond 2.0, with $V_{\rm DC}$ fixed at -1.0 and, in fact, peaks at a value of 0.298 at a normalized input level $V_{\rm AC}$ of 2.3. This corresponds to an increase in the second harmonic current content of about 8%. Provided the embedding networks are appropriate, this can also lead to an increase of about 8% in the second harmonic load power.

It is interesting to study how the optimum values of I_2 and $V_{\rm AC}$ vary as $V_{\rm DC}$ is made more negative. These trends are outlined in Table I. It appears that $I_2({\rm max})$ is heading toward an asymptotic limit. This is confirmed by performing the unified analysis with large $V_{\rm DC}$ and $V_{\rm AC}$ values. It is found that $I_2({\rm max})$ does not increase beyond a certain value, regardless of how large $V_{\rm DC}$ and $V_{\rm AC}$ are allowed to become. This limit can be explained by means of a simple Fourier analysis.

It has previously been mentioned that a square wave contains odd harmonics only. However, by varying the duty cycle of the waveform so that a rectangular wave results, even-order harmonic content can be introduced. It is easily shown that the second harmonic content of a rectangular wave peaks when the duty cycle is 0.25. Under these circumstances, the normalized second harmonic content is given by $I_2({\rm max}) = 1/\pi = 0.318$, which is consistent with the asymptotic limit in Table I. As $|V_{\rm DC}|$ and $V_{\rm AC}$ are allowed to increase, the relative values at the I_2 peak are such that the resulting current waveform is an increasingly close approximation to a rectangular wave with a duty cycle of 0.25.

In a practical device, it may be difficult to achieve this level of performance due to breakdown considerations. Nevertheless, it is clear that significantly improved performance (i.e., $I_2({\rm max}) > 0.276$) can be achieved by means of modest changes in the values of $V_{\rm DC}$ and $V_{\rm AC}$.



(b)

Fig. 6. Third harmonic contour plots (PLT). (a) Normal bias/drive ranges. (b) Extended bias/drive ranges.

B. Generic Tripler

In Section III-B, it was explained how overdriving a device biased at $V_{\rm mid}$ leads to a square-wave drain-current waveform, which has a significant third harmonic content. This is consistent with the third harmonic contour plot in Fig. 6(a). From the contour plot, it is immediately apparent that, by biasing the generic device at $V_{\rm mid}$, and by applying an adequate ac level, I_3 achieves a value close to the theoretical limit of 0.212, discussed in Section III-B. As outlined in [7], it is clear that this mode of

TABLE I
V_{DC}/V_{AC} TRENDS FOR MAXIMUM I_2 CURRENT

V_{DC}	V_{AC} (opt)	I_2 (max)	% Improvement
-1.0	2.0	0.276	-
-1.0	2.3	0.298	8.0
-1.1	2.4	0.300	8.7
-1.2	2.6	0.302	9.4
-1.3	2.7	0.303	9.8
-1.4	2.8	0.305	10.5
-1.5	2.9	0.306	10.9
-1.6	3.1	0.307	11.2
Theoretical Limit		0.318	15.2

operation yields superior conversion to the third harmonic than the more conventional pinchoff biasing arrangement.

The discussion in Section IV-A concerning the Fourier analysis of a rectangular wave will now be extended. Consider a rectangular wave with a duty cycle of 1/6. Unlike the square wave considered previously, this rectangular wave does contain significant even-order harmonics. It is easily shown that the normalized third harmonic coefficient of this waveform is $2/3\pi = 0.212$, which is the same as that of the square wave. In other words, by biasing the generic device such that the drain-current waveform approximates a rectangular wave with a duty cycle of 1/6, the same optimum value of I_3 can be achieved. In terms of a real device, this would require the device to be biased well below pinchoff, and a high ac drive level would be required. Before configuring a frequency tripler in this way, the breakdown characteristics of the real device in question would have to be considered. A third harmonic contour plot for the generic device, with extended ranges on both the V_{DC} and V_{AC} sweeps, is presented in Fig. 6(b).

The previously identified operating point, with V_{mid} biasing, is again apparent. However, another possible operating region, associated with a similar level of third harmonic generation, is evident. This initially manifests itself for a V_{DC} of about -5.0, and a V_{AC} of about 7.0, and it then extends down the plot, diagonally to the right-hand side. It is clear that for a given V_{DC}, this high third harmonic conversion is only maintained over a narrow window of V_{AC} levels. Within this window, the relationship between V_{DC} and V_{AC} is such that the resulting approximately rectangular waveform has a duty cycle of about 1/6. When V_{AC} moves outside this window, the duty cycle deviates significantly from the optimum value and the third harmonic conversion efficiency degrades.

The possibility of a 1/6 duty-cycle tripler design point is potentially interesting for a number of reasons. Firstly, the dc current content is significantly reduced, and this reduces the dissipated power. The fundamental content of the rectangular wave is less than that of the square wave and, thus, the fundamental rejection characteristics are improved. On the other hand, even-order harmonics (in particular, second harmonic) are introduced; this leads to the need to reject the second harmonic at the output, a problem that does not exist in the square-wave case. Finally, the operating point with the 1/6 duty cycle requires a large drive power to achieve the necessary V_{AC} levels. The square-wave approach is not as demanding in this regard. However, this is not necessarily a major concern, as low-frequency power is relatively cheap and easy to produce. The greatest concern in operating a multiplier in this way is likely to be breakdown related.

V. MULTIPLIER ANALYSIS USING ANGELOV HEMT MODEL

Thus far, the contour plot method has been used as a tool to assess the harmonic generation characteristics of a generic FET device as a function of both bias and applied voltage levels. On the basis of the results obtained, some generalized comments have been made concerning the suggested optimum circuit design criteria for a doubler and tripler.

In this section, a published and commonly used nonlinear HEMT model [8] is considered. In order that the analysis be as consistent as possible with that outlined in Section IV, a harmonic-balance simulator has not been used in this assessment. Moreover, a harmonic-balance simulation could introduce source and load mismatch effects which, though vitally important to actual multiplier performance, would make it difficult to extract specific information on the frequency conversion *capability* of a device as a function of bias and drive conditions. Such capability information is readily available from a Fourier analysis of the device I–V characteristic. Due to the complex nature of the I–V features of this model, a closed-form Fourier analysis is not possible, and a numerical discrete Fourier analysis was instead carried out to calculate the harmonic content of the drain current. Other aspects of the Angelov model, such as the capacitance elements, were not considered; these, of course, have an influence on the harmonic generation capability of a given device, but their effects are secondary to the effects of the I–V nonlinearities, as shown in [1], and further justified for low-frequency considerations in [9]. As in Section IV, this Fourier analysis has been performed across a matrix of bias and drive levels. The difference in this case of course is that the various voltage and current values are not normalized, as a specific device is under consideration; the actual device considered is a Westinghouse 0.5 mm $\times$ 0.25 μm power HEMT, with the parameters outlined in [10, Table V, App. 3]. The applied frequency has been arbitrarily set to 10 GHz in the analysis; the actual frequency is not significant, as the capacitance effects have been neglected. Having carried out the analysis, the results are again presented in the form of contour plots.

The resulting contour plots for the second and third harmonic coefficients of the output drain current are shown in Figs. 7 and 8. These "real-device" contour plots are similar in form to those derived in Section IV for the PLT generic FET device. For both the frequency doubler and tripler, the same regions of optimum performance are apparent. This demonstrates the validity of the generic unified theory approach.

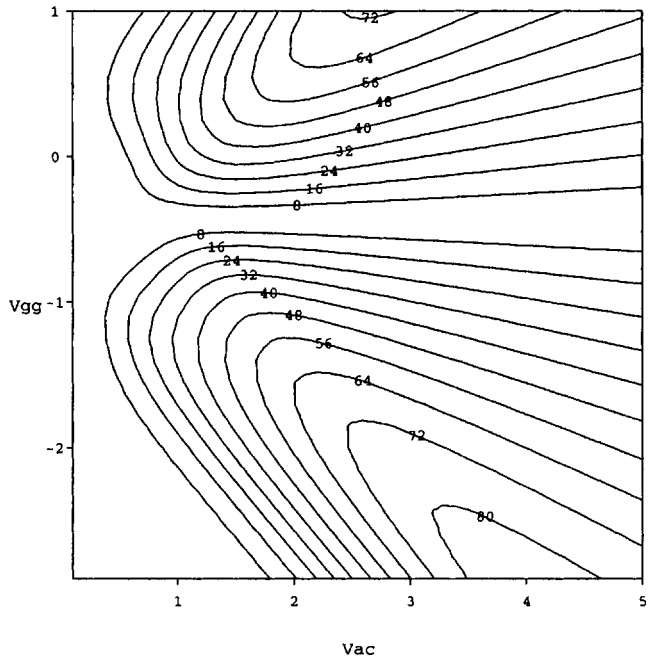


Fig. 7. Second harmonic contour-plot Angelov device model.

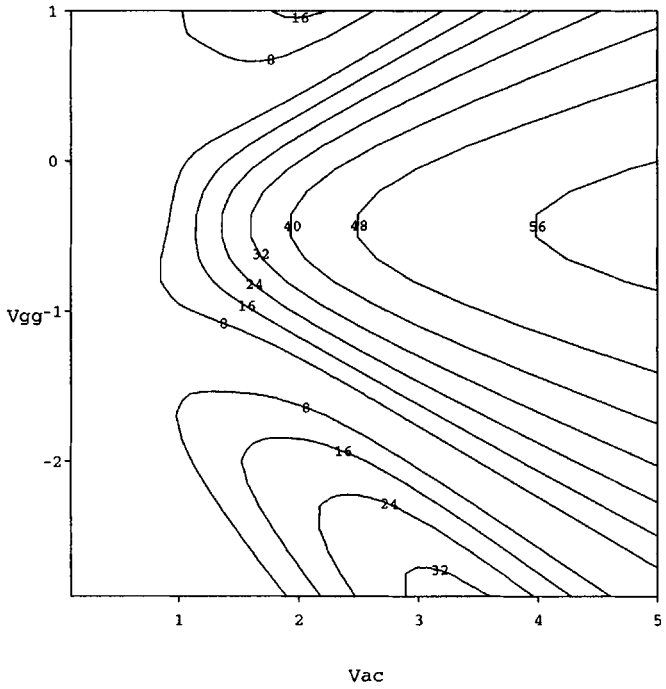


Fig. 8. Third harmonic contour-plot Angelov device model.

VI. Experimental Verification

A MMIC frequency tripler has been designed to generate power at 56.2 GHz [11]. The tripler consisted of a 4×40 μm pseudomorphic high electron-mobility transistor (pHEMT) device, biased near pinchoff, embedded between reactive stub networks. These networks were designed to provide good input and output matches, and unwanted harmonic rejection, and to facilitate bias injection. The design has been fabricated at a commercial 0.25-μm GaAs foundry, and has been assembled in a customized package with coaxial connectors. A minimum conversion loss of 14.1 dB has been measured (13 dB predicted) under optimum bias/drive conditions for this circuit. The conversion loss has been characterized as a function of the input power, and these results have been compared with the corresponding predictions using the Angelov model (the foundry device's threshold voltage, i.e., -1.4 V, is similar to that assumed for the Westinghouse device for which the Angelov parameters are available [10]). In order to eliminate all other factors so that the input power dependence of the conversion loss can be compared in isolation, the measured conversion loss values have all been offset by a set amount so that the resulting optimum conversion loss is consistent with the minimum conversion loss predicted by the Angelov model analysis described in Section V. The input power values have also been modified to account for input losses due to the packaging arrangement, and an imperfect input match. Using the threshold voltage value, the results of the generic unified theory analysis can be *de-normalized* and these also have been compared with the measurements. The resulting comparison is presented in Fig. 9.

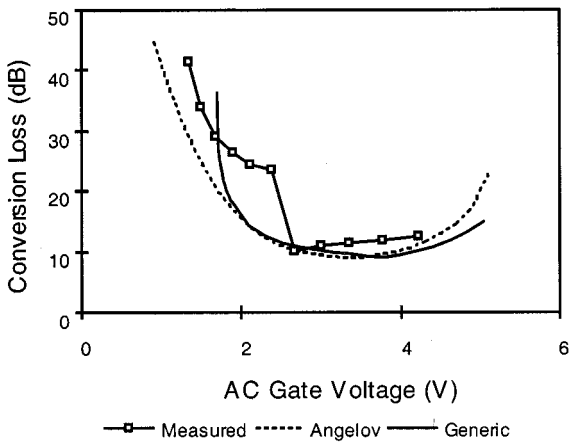


Fig. 9. Comparison between measured and predicted tripler conversion loss versus input level.

The agreement obtained is reasonable, especially considering that only the waveform clipping nonlinear effects have been considered. Note that the conversion loss associated with the generic model becomes infinite when the ac gate voltage becomes so small that the peak gate voltage is below the threshold. The Angelov model, with its more complex current formulation, yields a softer turn on in this regard.

VII. Conclusions

The analyses described in Sections IV and V validate the unified generic theory and demonstrate its value as a simple and effective means of intuitively assessing the harmonic generation capability of an FET. As a closed-form analytical tool, the unified generic theory can be used to perform rapid contour plot calculations at a large number of matrix points with a fine resolution. Being generic, the analysis it generally applicable to all FET-type devices provided the appropriate normalizations are carried out. The "real-device" approach, on the other

hand, requires a numerical solution, including a complex discrete Fourier analysis. The greater complexity of this approach makes it more expensive to implement; moreover, its results are device specific and are not directly "scalable" to other devices with different characteristics. Of course, for a given device, the "real-device" approach is likely to yield more accurate results; however, for the design of multipliers using modern sophisticated harmonic-balance simulation tools, the approximate optimum design suggested by the generic unified analysis is an ideal starting point which the harmonic-balance optimizer can refine as necessary to achieve the true optimum design solution. Similarly, the harmonic-balance-derived optimum design can be checked for consistency with the generic analysis, a useful way of improving the level of confidence in the harmonic-balance result.

The measured conversion loss dependence on the applied ac level for a fabricated and packaged MMIC frequency tripler has been compared with the corresponding predictions of the unified generic and device-specific (Angelov-based) analyses. The level of agreement achieved is reasonable, in particular, since only the current clipping effects have been considered, and the comparison certainly suggests that both approaches constitute valid frequency multiplier design and assessment tools.

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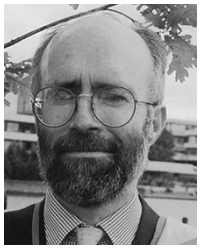

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