A Low-Power GaAs Front-End IC with Current-Reuse Configuration Using 0.15-μm-Gate MODFET's

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***Abstract*—We have developed a novel current-reuse configuration of a front-end integrated circuit (IC), where the current can be reused in the whole circuit blocks that are a low-noise amplifier, local amplifier, and mixer. The power dissipation of the front-end IC is reduced by the factor of three as compared to conventional front-end IC's. Excellent RF performance such as conversion gain of 30 dB and noise figure of 1.6 dB at 1.5 GHz is attained under the conditions of the supply voltage and current of 3.6 V and 3 mA, respectively.**

***Index Terms*—Current reuse, FET, front-end, GaAs, low power, phase-shift lithography.**

I. Introduction

GaAs FRONT-END integrated circuits (IC's) have come to be widely used for mobile communication sets due to their excellent RF performance. The essential characteristics of those front-end IC's are low noise, high gain, and low consumption power [1]–[3], which have been attained by shortening the gate length of GaAs FET's. Although this shortening of the gate length improves RF performance, supply voltage to FET's must be reduced due to the low breakdown voltage. It is noted that the typical operation voltage of a GaAs FET with 0.15-μm gate length is less than 2.0 V. Therefore, the FET's cannot be used for the application sets like personal handy phone sets where the voltages of 3 or 3.6 V from one Li battery cell or three NiMH battery cells are commonly used.

Based on these inherent characteristics of the deep submicrometer GaAs FET, we proposed a novel current-reuse configuration of a front-end IC, where a low-noise amplifier (LNA), local amplifier, and mixer can reuse the same dc current. This circuit configuration is expected to reduce the consumption power by the factor of three.

Several studies on the current-reuse configuration have been reported for the digital application field. However, few studies for analog application have been reported [1]. In particular, a three-stage current-reuse configuration of front-end IC's have not been reported thus far.

In this paper, we have demonstrated a low-power GaAs front-end IC with a three-stage current-reuse configuration using 0.15-μm-gate MODFET's, which can be used at a low operation voltage. At first the design concept of the current-reuse configuration is described. After the device structure of the IC is explained briefly, the RF performance of each component is explained. Finally, the total RF performance of the fabricated front-end IC with a current-reuse configuration is described. The performance of the fabricated IC showed conversion gain of 30 dB, a noise figure (NF) of 1.6 dB, and an output third-order intercept point (IP3) of 9 dBm at the frequency of 1.5 GHz with a supply voltage and current of 3.6 V and 3 mA, respectively. This power dissipation of 11 mW is the lowest value among those ever reported.

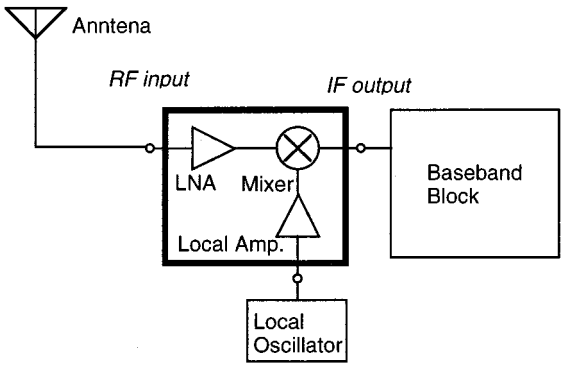

Fig. 1. Block diagram of the front-end IC in mobile communication sets.

II. Circuit Design

Fig. 1 shows the block diagram of the front-end IC, which consists of an LNA, local amplifier, and mixer. The LNA and local amplifier are designed by using a single-gate FET, while the mixer is designed by using a dual-gate FET. A design goal is to minimize the power dissipation of the front-end IC.

Fig. 2 shows the concept of the current-reuse configuration. In a conventional configuration, the voltage ($V_{\rm dd}$) from batteries is applied to each component independently. When all components consume the same current (I_d), the power dissipation is $3 \cdot V_{\rm dd} \cdot I_d$. On the contrary, the dc current is reused by three components in the current-reuse configuration. The power dissipation of the front-end IC with the current-reuse configuration is reduced to $V_{\rm dd} \cdot I_d$. However, the supply voltage to each component is reduced by the factor of three. Therefore, this configuration requires low voltage operation of less than 1.2 V to FET's because the battery used in mobile communication sets is usually 3.6 V. The 0.15 –μm-gate MODFET's was chosen due to their low voltage operation. It is noted that the 0.15-μm-gate MODFET's cannot be used in the conventional configuration because the operation voltage ($V_{\rm dd}$) is as high as 3.0 or 3.6 V in which the FET's cannot be operated due to their low breakdown voltage.

Manuscript received October 8, 1997.

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Publisher Item Identifier S 0018-9480(00)06528-5.

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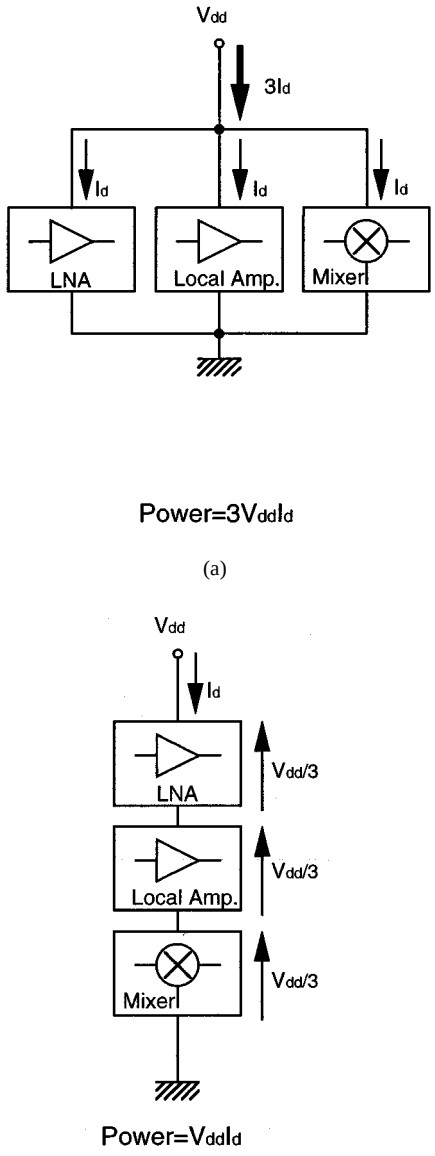

Fig. 2. Concept of the current-reuse configuration. (a) Conventional configuration. (b) Current-reuse configuration.

Fig. 3 shows the schematic circuit of the present IC using the current-reuse configuration. The function of each block is also described. The LNA, local amplifier, and mixer blocks are stacked. Basically the same dc current (I_d) flows through each FET via external choke coils. However, a bias circuit is required for the desirable operation current. Gate bias resistors (R_{g1}, R_{g2}, R_{g3}) are designed to be the same value of 10 kΩ because the same V_{ds} to each FET is available. Specifically, the voltages at source terminals are determined so that the same dc current I_d flows through each FET. The total consumption current of the IC is determined by the source bias resistor (R_s) of the mixer block. We design R_s to be 100 Ω for the operation current of 3 mA.

Large on-chip bypass capacitors and coupling capacitors are required in the circuit. The bypass capacitor is designed to be 200 pF to reduce the impedance of the bypass capacitors sufficiently.

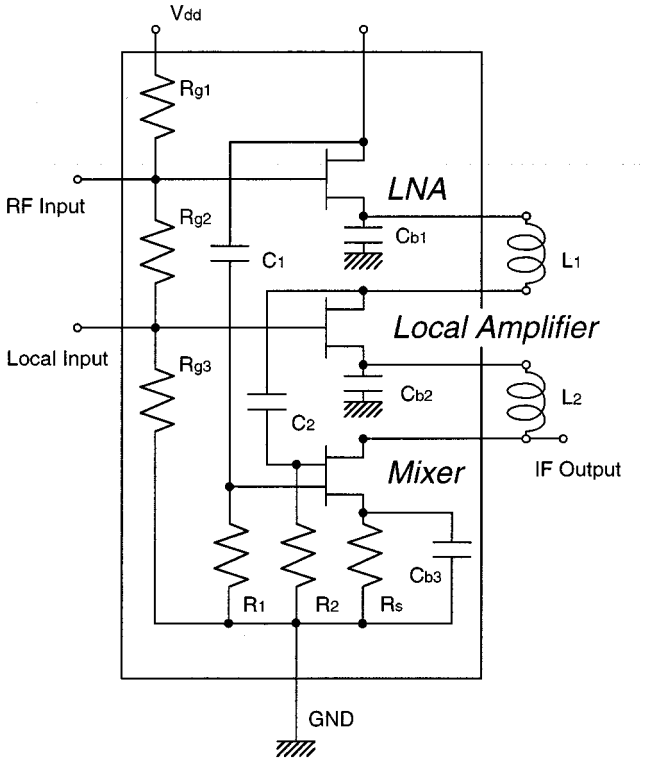

Fig. 3. Schematic circuit of the present IC with the current-reuse configuration.

The RF signal is amplified by the LNA and introduced to the dual gate mixer through coupling capacitors. RF signals are isolated to LO and mixer blocks by coke coils and a bypass capacitor. The LO signal is also introduced to the dual gate mixer as the same manner. The input RF signal with high frequency is converted to IF in the mixer block.

III. Device Structure and Fabrication Process

The schematic cross-sectional view of the present IC is shown in Fig. 4. The FET's are 0.15-μm-gate FET's, which are fabricated by using the phase-shifter–edge–line (PEL) method, which is one of the phase-shift lithography [4], [5]. This technique can fabricate deep-submicrometer FET's by utilizing interference of an i-line light of a conventional stepper. The gate and ohmic metal are Ti/Al and AuGeNi, respectively. The details of the fabrication process is described elsewhere [5].

The present IC employs $SrTiO_3$ (STO) capacitor technology [6] because the STO capacitor saves the area consumption owing to its high permittivity. The STO film is fabricated by using a low-temperature sputtering process in order to avoid the deterioration of impurity profile in the epitaxial structure [6]. Thus, the obtained STO capacitor has a dielectric constant of 100, which is over 15 times higher than that of a conventional SiN one. The STO film keeps a high dielectric constant from dc to over 10 GHz.

Fig. 5 depicts a chip photograph of the present IC. The top block is an LNA, the middle block is a local amplifier, and the

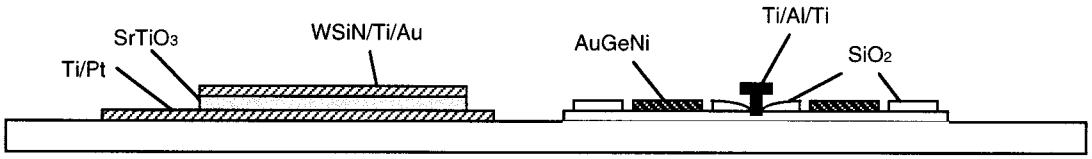

Fig. 4. Schematic cross section of the present IC with a 0.15-μm-gate MODFET and STO capacitor.

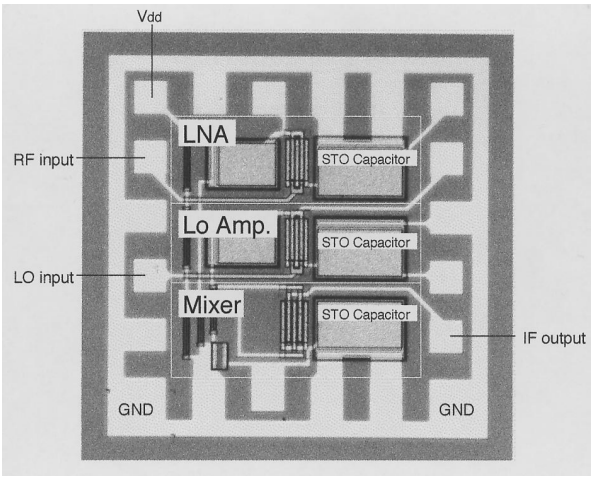

Fig. 5. Chip photograph of the fabricated IC with the current-reuse configuration.

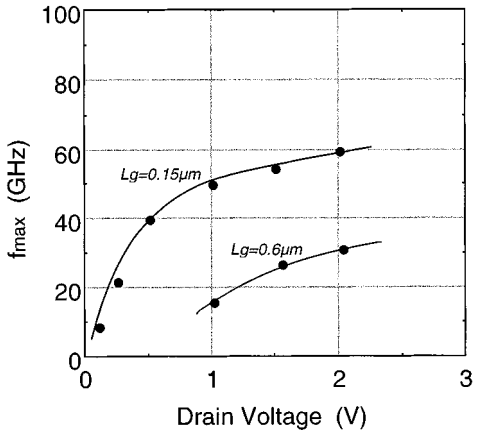

Fig. 6. $f_{\max}$ of the 0.15-μm-gate MODFET as a function of drain voltage.

bottom block is a mixer. The ground of the IC is arranged peripherally along the chip to reduce ground impedance. Pads for connecting to the external component are also arranged peripherally along the chip. The chip size is 1 mm $\times$ 1 mm. Owing to the STO capacitor technology, bypass capacitors and coupling capacitors are integrated in such a small area.

IV. Results and Discussion

A. MODFET

Fig. 6 shows the measured gate-length dependence of $f_{\max}$ (maximum oscillation frequency) as a function of the drain voltage. The $f_{\max}$ was calculated from the s-parameter measured by an on-wafer technique. The measured condition is not for the bias point, which gives a maximum $f_{\max}$ of the device, but for the bias point at the operation condition. The 0.15-μm gate MODFET shows higher $f_{\max}$ compared to the 0.6 μm one. The 0.15-μm-gate MODFET has sufficiently high $f_{\max}$ even for the drain voltage of 1 V.

The measured drain breakdown voltage of the 0.15-μm-gate MODFET was lower than 2.5 V. The drain conductance is drastically increased for the drain voltage over 2.5 V due to the punch through. This fact indicates that MODFET's with 0.15-μ m gate length are suitable to the current-reuse configuration, in which the supply voltage to FET's is reduced down to 1.2 V.

B. LNA

Fig. 7 shows the measured gain and NF of the fabricated LNA as a function of the supply voltage. These are measured by using an NF meter (HP8970A). The supply voltage was varied

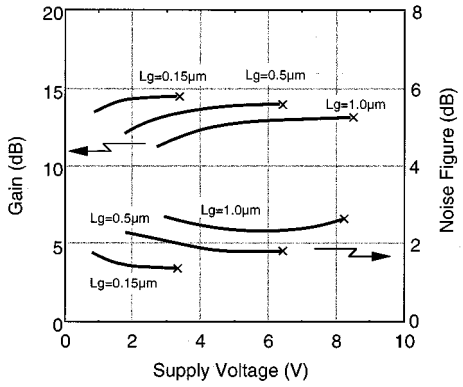

Fig. 7. Gain and NF of the fabricated LNA as a function of the supply voltage at 1.5 GHz.

at an operation current of 3 mA. The input and output ports were matched to the chip externally by stab tuners. The drain voltage was applied up to the condition where punch through of the FET's was occurred. Namely, the maximum supply voltages in Fig. 7 indicate the breakdown voltages of FET's with various gate lengths. The FET with a gate length of 0.15 μm shows lower breakdown voltage as compared to the FET's with a gate length of 1.0 μm. The LNA with an 0.15-μm-gate FET exhibits higher gain and lower NF than those LNA's with 0.6- or 1.0-μm gate length at a supply voltage of 1 V. More specifically, the 0.15-μm-gate MODFET is needed to operate the LNA at a supply voltage of less than 1 V. This is because the 0.15-μm FET has smaller $C_{\rm gs}$ and larger transconductance.

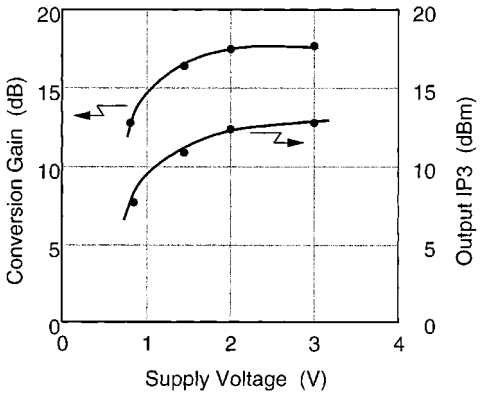

Fig. 8. Conversion gain and output IP3 of the fabricated dual-gate mixer as a function of the supply voltage at 1.5 GHz.

TABLE I
COMPARISON BETWEEN THE DEVELOPED AND CONVENTIONAL IC'S

Performance		Present IC	Conventional IC
Power dissipation	(mW)	11	30
Conversion Gain	(dB)	30	27
Output IP3	(dBm)	9	10
Noise Figure	(dB)	1.6	2.2

C. Dual-Gate Mixer

We evaluated the fabricated dual-gate mixer with 0.15-μm gate length. Fig. 8 shows the measured conversion gain and output IP3 as a function of the supply voltage. The frequency of input RF, local signal, and IF are 1.5, 1.35 GHz, and 150 MHz, respectively. This characteristic was measured by using two signal generators and a spectrum analyzer. The matching was tuned by the same manner as the section of the LNA. Although the RF performance is degraded by reducing the operation voltage, the conversion gain of 15 dB and the output IP3 of 9 dBm are obtained at operation voltage of 1 V for the 0.15-μm-gate MODFET. This characteristic is sufficient for the application to front-end IC's.

D. Front-End IC's

We evaluated the fabricated front-end IC with and without the current-reuse configuration, which consisted of the LNA, local amplifier, and dual-gate mixer at 1.5 GHz. All the RF ports were matched to the chip externally. The isolation between the LNA and local amplifier was as high as 20 dB. This is because the inductance for RF cut was sufficiently large to isolate each component.

The comparison of the RF performance between the present IC and conventional IC is summarized in Table I. The present IC has a current-reuse configuration with the 0.15-μm-gate FET's. On the other hand, the conventional IC has no current-reuse configuration where the gate length of the FET's is 1.0 μm. Table I also shows that the power dissipation is reduced from 30 to 11 mW, keeping excellent RF performance. This performance is realized by the current-reuse configuration with 0.15-μm-gate MODFET technology.

V. CONCLUSION

We have developed a low-power GaAs front-end IC with a current-reuse configuration using 0.15-μm-gate MODFET's fabricated by using phase-shift lithography. The current-reuse configuration using 0.15-μm-gate MODFET's reduced the power consumption of a front-end IC by the factor of three. Sufficient RF performance such as conversion gain of 30 dB, NF of 1.6 dB, and output IP3 of 9 dBm at 1.5 GHz was obtained at a supply voltage of 3.6 V and operation current of 3 mA. The present GaAs front-end IC is suited to recent mobile communication systems, which require low dissipation power.

ACKNOWLEDGMENT

The authors would like to thank Dr. K. Itoh and Dr. G. Kano for their encouragement through this research and M. Nishitsuji and Dr. A. Tamura for their fruitful discussion on the STO process.

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