# Design and Performance of a $Ka$-Band Monolithic Phase Shifter Utilizing Nonresonant FET Switches

Kenichi Maruhashi, *Member, IEEE*, Hiroshi Mizutani, *Member, IEEE*, and Keiichi Ohata, *Member, IEEE*

***Abstract*—This paper describes design consideration and performance of a $Ka$-band monolithic phase shifter utilizing nonresonant FET switches. The switches show broad-band on/off characteristics up to 60 GHz without using inductors; thus, robust circuit design is possible for a switched-line phase shifter. To determine circuit topology, we introduce a schematic design approach. As a result, desired phase shift as well as good matching characteristics can be realized. The developed 4-bit monolithic phase shifter demonstrates an overall phase deviation less than 5° rms and an insertion loss variation less than 0.65 dB rms from 33 to 35 GHz. For all 16 states, the insertion loss is measured to be 13.1±1.1 dB and the VSWR is less than 1.6. The chip size of the monolithic phase shifter is 2.5 mm × 2.2 mm.**

***Index Terms*—Millimeter-wave phase shifter, MMIC's, MMIC phase shifters, MODFET switches.**

## I. Introduction

PHASE shifters are key components for phased-array antenna systems. Monolithic implementation is necessary for low cost and high producibility. Several monolithic phase shifters have been reported at $Ka$- and $Q$-bands [1]–[3]. In these frequency bands, switched-line configuration has advantages of applicable phase-shift characteristics to the above systems and small chip size due to simple circuit and layout designs. FET switches are advantageous over their p-i-n diode counterparts [4] for a simple epitaxial structure and a small number of fabrication steps in the monolithic integrated-circuit (IC) process, and for negligible current to drive switches.

A conventional switched-line phase shifter at $Ka$-band employs resonant switches, which consist of FET's and spiral inductors [1], [2]. In order to obtain good isolation characteristics for the off-state switch, a precise model or well-established data base for the inductors is needed at the operating frequency. Moreover, for a relatively wide-band phase shifter, eliminating resonance is desirable for reduced sensitivity to process variation and design tolerance. However, at $Ka$-band, it had been difficult to achieve sufficient isolation for the FET switches without resonance, due to parasitics. Recently, we have developed a nonresonant FET switch operating from dc to 60 GHz [5], [6]. Based on ohmic electrode sharing technology (OEST), parasitics around the switch have been reduced. The size of the switch is almost as small as that of an FET having same gatewidth, indicating that the developed switch is suitable for monolithic phase shifters.

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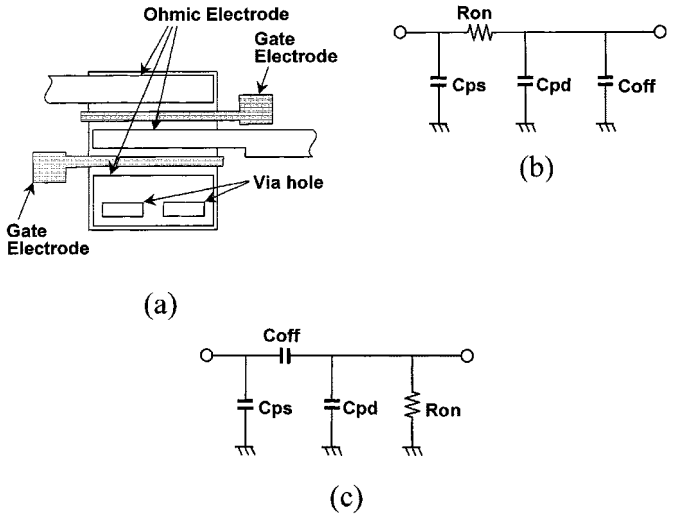


Fig. 1. OEST switch. (a) Layout pattern. (b) On-state equivalent circuit. (c) Off-state equivalent circuit.

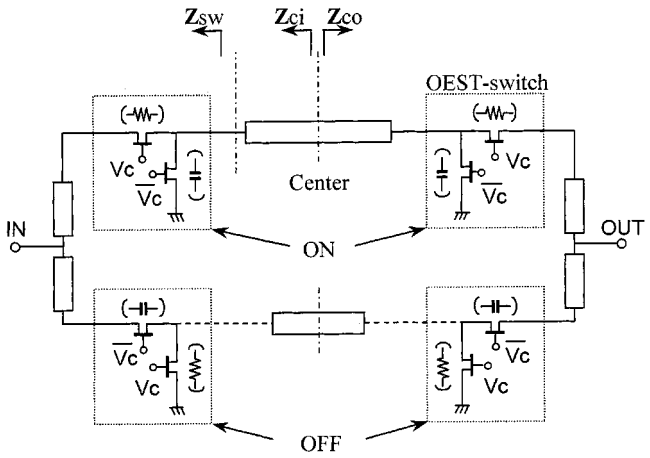


Fig. 2. Circuit scheme for a switched-line phase shifter.

In this paper, we demonstrate the design process and performance of a $Ka$-band monolithic phase shifter using the OEST switches. The fabricated switched-line phase shifter shows good phase-shift characteristics with high design feasibility.

## II. Circuit Design

A layout and on- and off-state equivalent circuits of the OEST switch are shown in Fig. 1. The switch consists of cascade-connected series and shunt FET's. Reduction of parasitic induc-

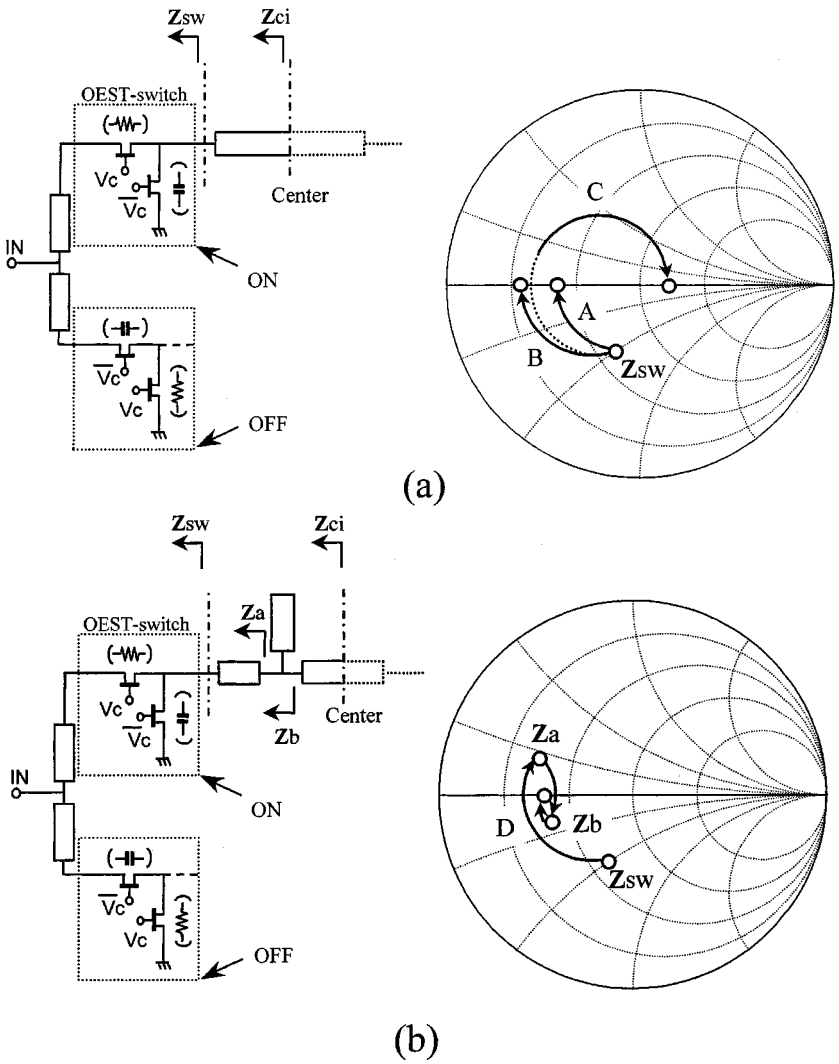


Fig. 3. Impedance responses: (a) when the reference lines and the delay lines of the 22.5°- and 180°-bit phase shifters and (b) when the delay line of the 90°-bit phase shifter are added to the switches.

tance and capacitance has been realized by arraying both FET's with a common electrode between them instead of using conventional wiring. This resulted in broad-band on/off characteristics up to 60 GHz without using inductors [5], [6]. The switches have small on-state series resistance (Ron) and small off-state series capacitance (Coff), which are essential for low insertion loss and high isolation, respectively. Over dc–40 GHz, the measured insertion loss was better than 1.5 dB and the isolation was larger than 22 dB. The switch power capability larger than 20 dBm has been reported at 40 GHz [6].

A circuit scheme for a switched-line phase shifter is shown in Fig. 2. The signal path is switched in order to obtain phase shift owing to the length difference between reference and delay lines. In phase-shifter design, two conditions must be satisfied. One is the matching condition and the other is the phase-shift condition. Since the OEST switches appear as capacitance connected between the line and ground, mismatch will occur. To obtain good phase shift and matching characteristics, a special design technique has been introduced as follows. Dividing the circuit shown in Fig. 2 at center, we define the impedance viewing from the center to input port as $Z_{\rm ci}$, and the impedance viewing from the center to output port as $Z_{\rm co}$. At this design step, lossless circuits are assumed and, therefore, matching condition is expressed as $Z_{\rm ci} = Z_{\rm co}^*$. Since $Z_{\rm ci}$ is identical to $Z_{\rm co}$ due to circuit symmetry, $Z_{\rm ci}$ (or $Z_{\rm co}$) should be real ($\mathrm{Im}(Z_{\rm ci}) = 0$) and plotted on the $X$-axis in the Smith Chart. For a half-set of the divided circuit in Fig. 2, the phase-shift condition is that the phase should delay half of the desired phase shift for a whole phase shifter.

The circuit topology can be found using a schematic design concept as follows. The impedance responses are shown in Fig. 3(a) when the reference line for each single-bit phase shifter and the delay lines of the 22.5°- and 180°-bit phase shifters are added to the switches. The impedance $Z$ is described as

$$Z = \frac{Z_{\rm sw}\cos\theta + jZ_0\sin\theta}{\cos\theta + j(Z_{\rm sw}/Z_0)\sin\theta} \tag{1}$$

where $Z_{\rm sw}$ is the impedance viewing into the output of the switch (see Fig. 2), and $Z_0$ and $\theta$ are characteristic impedance and electrical length in angle unit of the line. $Z_{\rm sw}$ has a negative imaginary value due to the capacitive nature of the switch. For

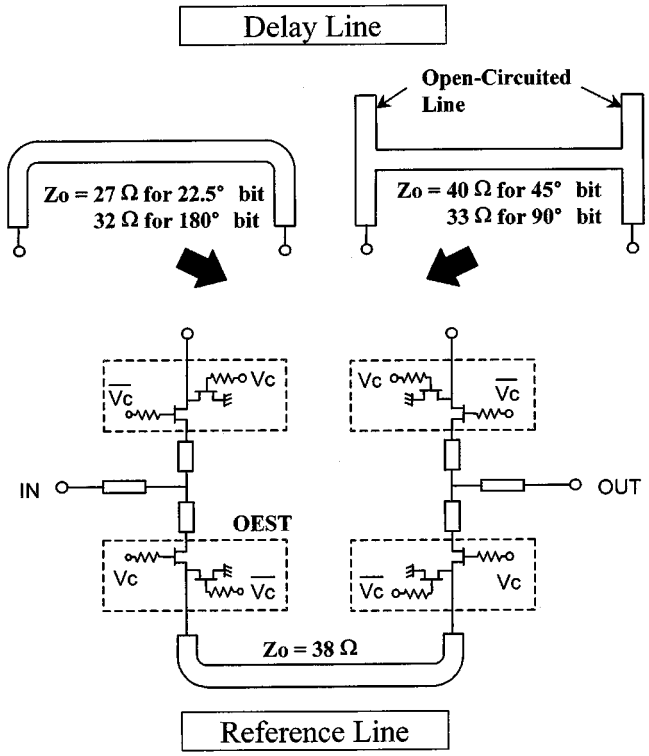


Fig. 4. Complete circuit design of each single-bit phase shifter.

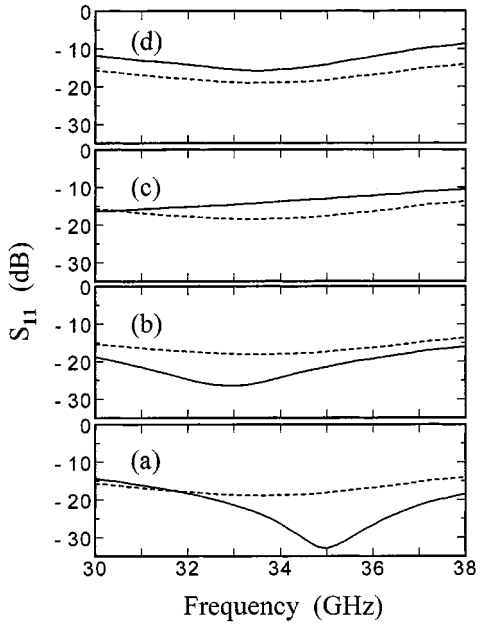


Fig. 5. Measured return loss for: (a) 22.5°-, (b) 45°-, (c) 90°-, and (d) 180°-bit phase shifters. Solid and dotted lines represent data when a signal passed through the delay and reference lines, respectively.

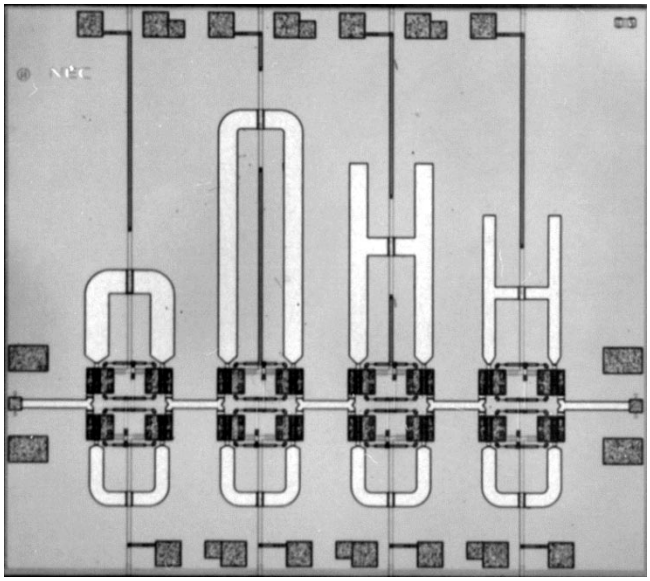

Fig. 6. Chip photograph for the fabricated 4-bit monolithic phase shifter (2.5 mm × 2.2 mm).

the reference line design, an appropriate line is added so that $Z$ moves from $Z_{\rm sw}$ along a locus (A) to the $X$-axis on the Smith Chart. This means that the matching condition ($\mathrm{Im}(Z_{\rm ci}) = 0$) is satisfied. For the delay line design of the 22.5°-bit phase shifter, a lower impedance line is used so that $Z$ moves along a locus (B) to the $X$-axis. The difference of characteristic impedance produces the phase difference between reference and delay lines, while the imaginary part of $Z$ is equal to zero for both cases. For the delay line design of the 180°-bit phase shifter, the line longer than the reference line by a quarter-wave length provides a phase difference of 90° at the center of the line. This move $Z$ along a locus (C) to the $X$-axis. The impedance response is shown in Fig. 3(b) when the delay line of the 90°-bit phase shifter added to the switch. In this case, the desired phase difference between the reference and delay lines cannot be produced by using conventionally fabricated microstrip lines ($Z_0$ : 25–75 Ω), and $Z$ moves from $Z_{\rm sw}$ along a locus (D) to have a positive imaginary value. To move it back to the $X$-axis, an additional capacitive open-circuited line is incorporated in the delay line. The characteristic impedance also needs to be optimized. The design approach for the delay line of the 45°-bit phase shifter is the same as that of the 90°-bit phase shifter.

Complete circuit design of each single-bit phase shifter is shown in Fig. 4. Length and width for lines were optimized in detail involving the effects of bends, T-junctions, loss in the line and switches to obtain good return loss and desired phase shift on a circuit simulator. Characteristic impedance's of all lines are lower than 50 Ω. Return loss better than 18 dB was designed for each-bit phase shifter over a frequency range from 32.5 to 35.5 GHz. For the 4-bit phase shifter, the maximum phase deviation to the desired phase was designed to be 6° rms for 16 states over the same frequency range, which is mainly determined by a linear phase-frequency relation for the delay lines. With this circuit topology, the layout is simple, which is an advantage of the switched-line configuration.

## III. Fabrication Process and Device Characteristics

The employed monolithic-microwave integrated-circuit (MMIC) process has been developed for millimeter-wave high-power applications [7]. The heterojunction FET's (HJFET's) for the switch elements consist of an InGaAs channel layer sandwiched between Si-doped AlGaAs layers. This structure leads to high current density, which is essential

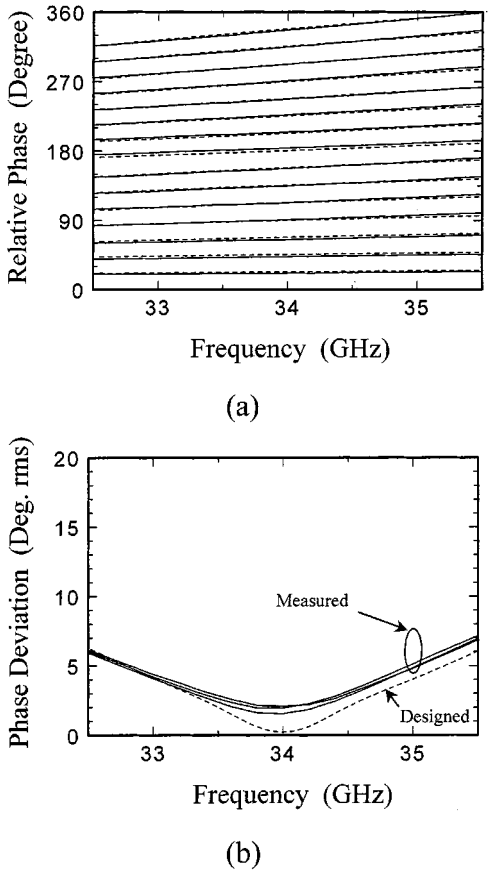


Fig. 7. Phase-shift characteristics of the phase shifter. (a) Phase delay for all 16 states. Solid lines represent measured data and dotted lines represent designed data. (b) rms phase deviations to the desired phase for three different chips.

for low insertion loss of the switch. The HJFET has a T-shaped gate with 0.15-$\mu$m length. The device exhibited a typical transconductance of 400 mS/mm and an $f_{\max}$ of 200 GHz with a reverse gate–drain breakdown voltage of 10 V. For the OEST switch with 100-$\mu$m-gate-wide FET's, $R_{\rm on}$ and $C_{\rm off}$ were estimated to be 9 $\Omega$ and 10 fF. Parasitic capacitance's $C_{\rm ps}$ and $C_{\rm pd}$, as shown in Fig. 1, were also estimated to be both 10 fF.

## IV. Phase-Shifter Performance

To confirm design feasibility, return loss and phase delay were measured for each single-bit phase shifter. As shown in Fig. 5, the measured return loss was better than 12 dB for each single-bit phase shifter over a frequency range from 32.5 to 35.5 GHz. The insertion loss variation of each single-bit phase shifter was from 3.0 to 3.8 dB, regardless of which reference or delay line was selected. At 34 GHz, the phase-shift deviation to the desired value was less than 2.5° for each single-bit phase shifter.

A chip photograph for the fabricated 4-bit monolithic phase shifter is shown in Fig. 6. The 22.5°-, 180°-, 90°-, and 45°-bit phase shifters are connected in series. The chip size is 2.5 mm $\times$ 2.2 mm $\times$ 0.04 mm. MMIC chips were tested using RF probes. Control voltages of 0 and $-5$ V were applied to the OEST switches. The phase-shift characteristics are shown in Fig. 7. For 16 states, the measured and designed relative phases were

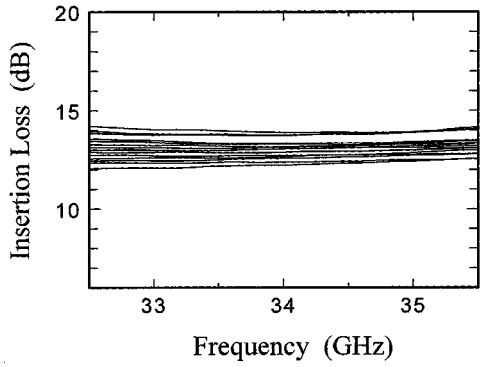


Fig. 8. Measured insertion loss of the phase shifter for all 16 states.

good agreement. The rms phase deviations to the desired phase were measured for three different chips. The phase deviations were less than 5° rms from 33 to 35 GHz and 7° rms from 32.5 to 35.5 GHz. At the center frequency of 34 GHz, a phase deviation less than 2.2° rms was obtained.

The measured insertion loss is shown in Fig. 8. An insertion loss for 16 states was 13.1$\pm$1.1 dB from 34 to 36 GHz. This value is comparable to the published data (12.8$\pm$1.8 dB from 35 to 37 GHz) for the FET-switch-based 4-bit phase shifter [3]. The excellent flatness of insertion loss versus frequency was originated from broad-band switch characteristics. An insertion-loss variation less than 0.65-dB rms was measured from 33 to 35 GHz. Over this frequency range, the measured input and output VSWR's were better than 1.6 for all 16 states.

## V. Conclusion

Design consideration and performance of a $Ka$-band monolithic phase shifter utilizing broad-band nonresonant FET switches were described in this paper. In the circuit design, characteristic impedance's for the reference and delay lines were optimized and additional open-circuited lines were introduced into delay lines of the 45°- and 90°-bit phase shifters based on the schematic design approach. The 4-bit switched-line monolithic phase shifter demonstrated an overall phase deviation less than 5° rms and an insertion loss variation less than 0.65-dB rms from 33 to 35 GHz. An insertion loss of 13.1$\pm$1.1 dB and VSWR less than 1.6 were obtained for 16 states. The developed phase shifter featuring small chip size as well as excellent performance promises great applicability to $Ka$-band phased-array antenna systems.

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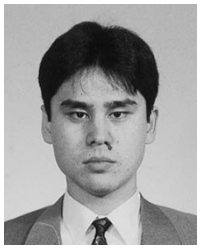

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