A Single-Chip GaAs MMIC Image-Rejection Front-End for Digital European Cordless Telecommunications

Farahnaz Sabouri-S., Christian Christensen, *Life Member, IEEE*, and Torben Larsen, *Member, IEEE*

***Abstract*—An active image-rejection filter is presented in this paper, which applies actively coupled passive resonators. The filter has very low noise and high insertion gain, which may eliminate the use of a low-noise amplifier (LNA) in front-end applications. The GaAs monolithic-microwave integrated-circuit (MMIC) chip area is 3.3 mm^2. The filter has 12-dB insertion gain, 45-dB image rejection, 6.2-dB noise figure, and dissipates 4.3 mA from a 3-V supply. A MMIC mixer is also presented. The mixer applies two single-gate MESFET's on a 2.2-mm^2 GaAs substrate. The mixer has 2.5-dB conversion gain and better than 8-dB single-sideband (SSB) noise figure with a current dissipation of 3.5 mA applying a single 5-V supply. The mixer exhibits very good local oscillator (LO)/RF and LO/IF isolation of better than 30 and 17 dB, respectively. Finally, the entire front-end, including the LNA, image rejection filter, and mixer functions is realized on a 5.7-mm^2 GaAs substrate. The front-end has a conversion gain of 15 dB and an image rejection of more than 53 dB with 0-dBm LO power. The SSB noise figure is better than 6.4 dB. The total power dissipation of the front-end is 33 mW. The MMIC's are applicable as a single-block LNA and image-rejection filter, mixer, and single-block front-end in digital European cordless telecommunications. With minor modifications, the MMIC's can be applied in other wireless communication systems working around 2 GHz, e.g., GSM-1800 and GSM-1900.**

***Index Terms*—Active filter, mixer, MMIC, single chip front-end.**

I. Introduction

THE European mobile and cordless market is developing rapidly. This, together with rapid development of new technologies and circuit topologies, have made many companies (e.g., National Semiconductor, Santa Clara, CA, Philips, Eindhoven, The Netherlands, Motorola, Phoenix, AZ, and Siemens, Munich, Germany) start development of RF application-specific integrated circuits (RF ASIC's). Consequently, many chipsets combining different functions of transmit/receive modules for mobile and cordless standards have been made available in the last few years. However, filtering functions are still placed off-chip in almost all available chipsets and reported research work in this area [1]–[6]. This paper concentrates on development of an active image-rejection filter applying GaAs monolithic-microwave integrated-circuit (MMIC) technology for use in a digital European cordless telecommunications (DECT) front-end as one of the main challenges of increasing the level of integration [7]. However, an integrated filter alone cannot serve for size, power, or even cost unless it is integrated with the rest of the front-end. Therefore, this paper aims at developing an integrated receiver front-end consisting of the low-noise amplifier (LNA), image-rejection filter, and the mixer in one single chip. This paper treats a specific system where knowledge of the application has been deployed in the circuit design. To the authors' knowledge, this is the first active filter with low noise and high gain in one and the same circuitry.

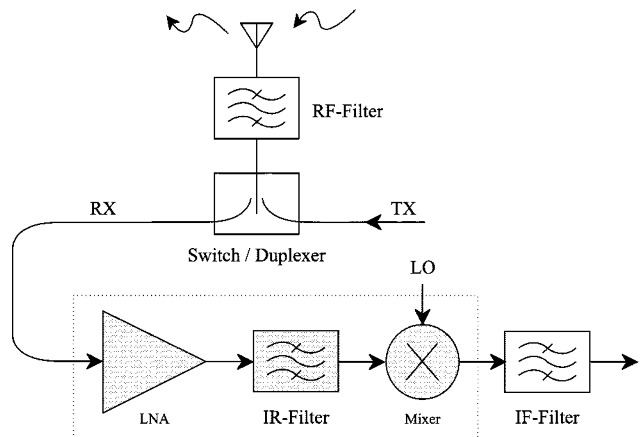

Fig. 1. Block diagram of a typical heterodyne radio receiver front-end.

II. Circuit Design

This paper presents the development of three GaAs MMIC's with very low power dissipation for cordless and mobile telephone systems working around 2 GHz. The specifications are, though, drawn from the DECT standard [8]. The developed MMIC's are: 1) an LNA and image rejection filter; 2) a mixer; and 3) a receiver front-end consisting of an LNA, an image rejection filter, and a mixer. A block diagram of the receiver front-end of a typical heterodyne radio receiver is shown in Fig. 1, in which the MMIC circuit is highlighted.

The applied process is a 0.5-μm ion-implanted GaAs process from GEC-Marconi Materials Technology (GMMT), Caswell,

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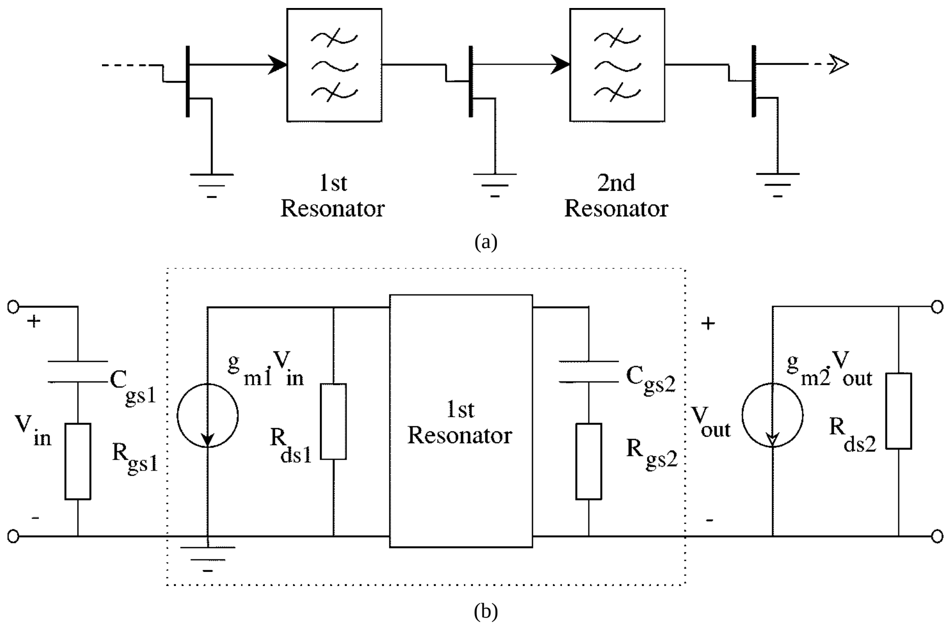

Fig. 2. (a) Basic configuration of the actively coupled resonators. (b) Resonator loaded with the output of the preceding transistor and the input of the succeeding transistor.

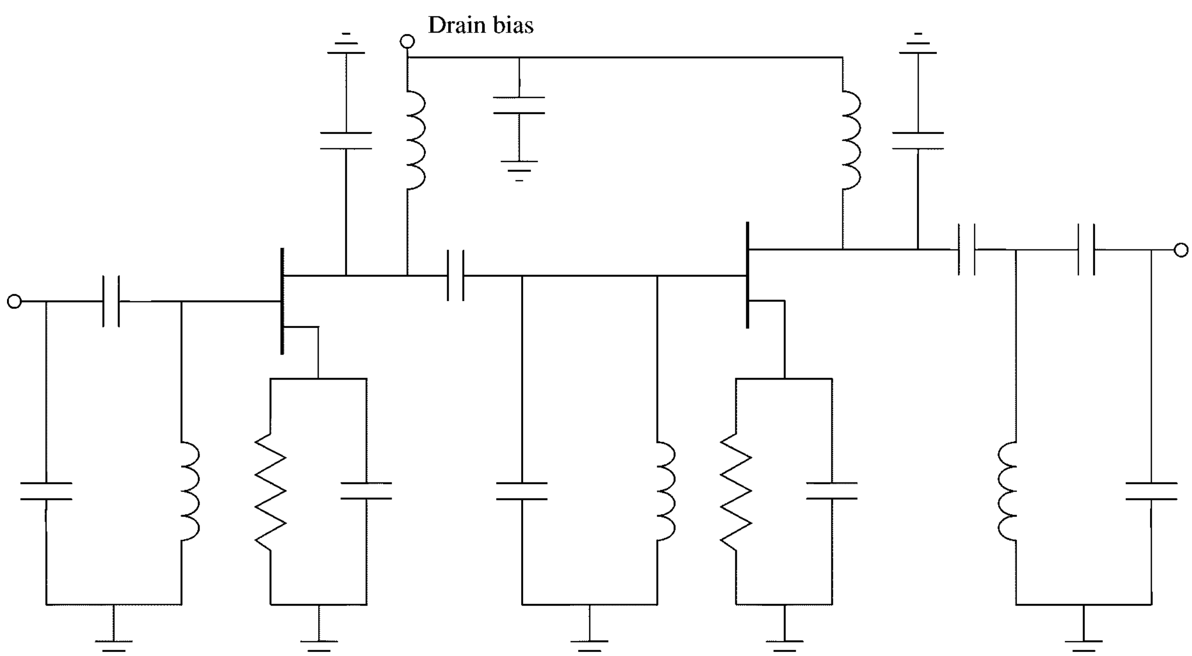

Fig. 3. Circuit diagram of the proposed active filter.

U.K.; the F20 process [9]. The Foundry provides accurate small-signal as well as large-signal models for simulations.

A. LNA and IR Filter

According to the filter's application in cordless and/or mobile telephone handsets, the circuit should be suitable for mass production. Hence, the circuit should not require any post-fabrication tuning or off-chip components. It is also important that the number of bias lines is low such that simple biasing circuitry is applicable. As a demand on high degree of integration, high insertion gain and low noise is of importance in order to somehow integrate the LNA, usually preceding the image-rejection filter, into the same circuit. The low microwave frequency restricts the design further to only apply more lossy lumped elements rather than large distributed elements.

Excellent works are reported on narrow-band active filter configurations over the last few years [10]–[14]. However, these solutions are not restricted to the above-mentioned requirements due to the specific application and mass production and, in the best case, either suffer from demands on post-fabrication tuning or insertion loss. The noise figure is not addressed in the mentioned works but may be quite high according to Krantz's [15] investigations. This paper presents an active image-rejection filter suitable for mass production with simple circuitry and low power consumption. Furthermore, the proposed filter

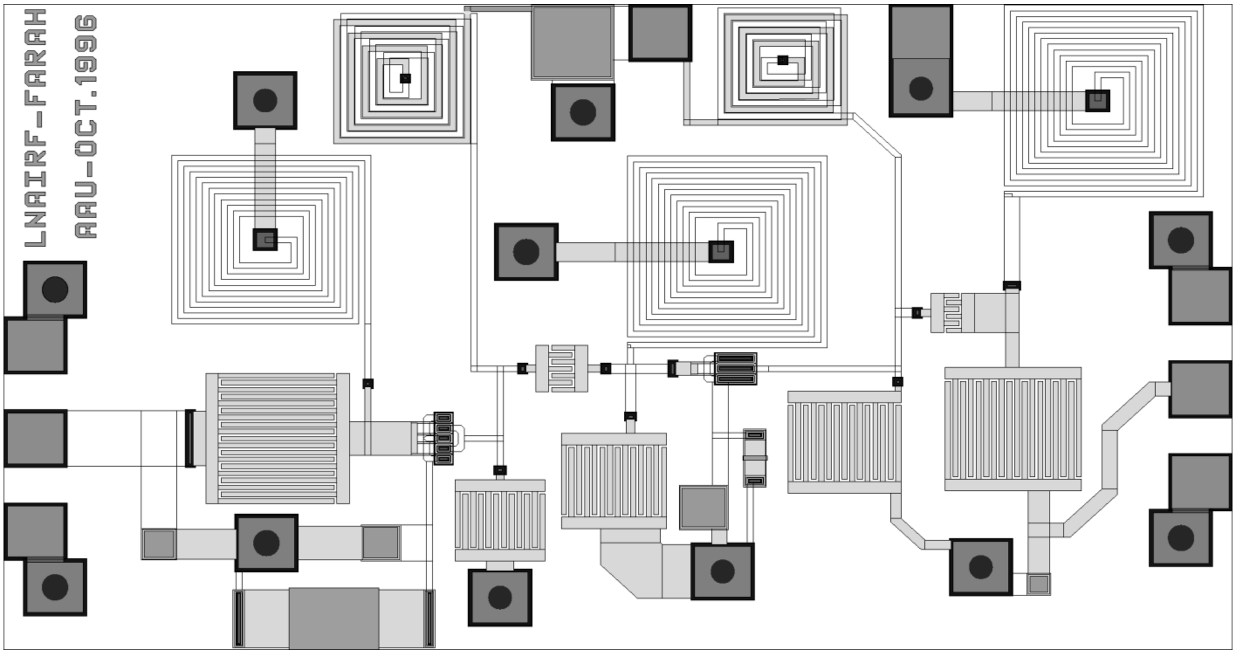

Fig. 4. Layout of the proposed active filter.

has high insertion gain and low noise figure, which eliminates the need for an LNA before the filter in a DECT front-end.

Applying actively coupled resonators in a cascade configuration, shown in Fig. 2(a), the circuit sensitivity to process tolerances is reduced due to the noninteractive resonators. At the same time, the task of designing a high-order filter is reduced to simple low-order sections. The transistors are not actually a part of the resonators, but are integrated into the resonators in calculations, since they do not act as true unilateral gain sections. By this method, the influence of the port impedances is reduced by including the influence of the transistors' input and output impedances in the resonators' transfer characteristic. This is illustrated in Fig. 2(b), where the transistor is modeled with only its gate–source capacitance and resistance at the input and transconductance and channel resistance at the output.

Different filter section types can then be applied to achieve the desired characteristic. However, investigations among parallel and series bandpass, band-reject, and elliptic filter configurations show that the parallel bandpass configuration is best regarding out-of-band rejection and spurious responses [16]. It also has the advantage that grounded inductors in the resonators can serve as choke inductors as well as dc grounding of the gates in a self-biasing circuit.

The obtainable Q value in one resonator section determines the number of resonators needed in the cascade configuration. For MMIC implementation at this low microwave frequency, i.e., around 2 GHz, spiral inductors should be used to reduce the chip size. However, the area of the spiral inductor is still large compared to that of other lumped elements. This results in increased costs and unavoidable parasitic effects with low Q values. Different active inductor configurations as an alternative to the spiral inductor has been investigated [16]. Two active inductor circuits has been designed and their measured results are compared with passive spiral inductors from the applied process with the same inductance value. This has shown that the active

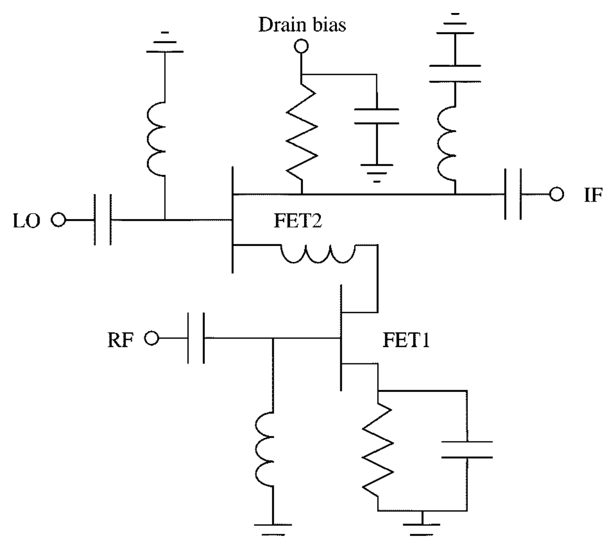

Fig. 5. Circuit diagram of the mixer.

inductors have almost the same Q value with significant power consumption and contribution to noise. Hence, passive spiral inductors are applied in the resonators.

The filter is matched to 50 Ω at both ports applying tapped-capacitor matching, which resembles a bandpass response and can be used to improve the attenuation. In order to reduce the number of bias lines, the self-biasing method is applied with a single 3-V power supply. The series feedback capacitor in the biasing circuitry is further applied to adjust the transistors input impedance for better gain and noise performance. The first resonator is optimized for better noise performance applying a 4×30 μm MESFET. As the second FET, a 2×75 μm device is applied to improve the insertion gain. Both FET's operate at around 10% of the drain–source saturation current. The final circuit configuration is shown in Fig. 3.

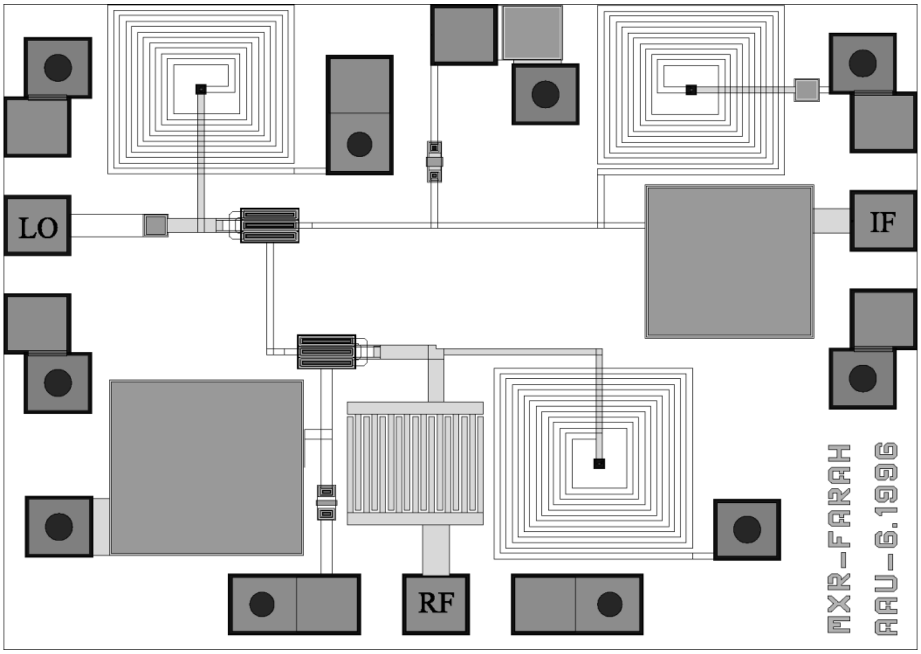

Fig. 6. Circuit layout of the mixer.

The circuit is fabricated on 3.3-mm^2 GaAs substrate. In order to reduce the circuit sensitivity to process tolerances, interdigital capacitors are applied rather than overlay capacitors where the capacitance value allow this since the interdigital capacitors' variation due to process tolerances is negligible compared to about 15% for overlay capacitors. This results in more chip area, but the benefit of reducing the sensitivity to process tolerances is of much more importance for the yield. The circuit layout is shown in Fig. 4.

B. Mixer

A mixer with conversion gain, low-current dissipation, and good built-in local oscillator (LO)/RF isolation is required. The latter to eliminate any couplers/filters, which usually occupy much chip space. A dual-gate FET mixer can serve for these requirements. However, a reliable nonlinear model for a dual-gate MESFET from the applied GaAs process is not available. Dual-gate FET's are normally modeled as a cascade of two single-gate MESFET's [17]. The same principle is used in the real configuration; i.e., applying two single-gate MESFET's in cascode to resemble a dual-gate MESFET in realizing a mixer with good LO/RF isolation with few components. The mixer is biased in a low-noise mixer mode [18], where the lower FET is biased in its linear region and the upper FET in the current saturated region. Both FET's are gate biased close to pinchoff. The frequency conversion takes place inside the lower FET using its transconductance g_m and channel resistance $R_{\rm ds}$ as the main nonlinearities, while the upper FET acts mainly as an IF post-amplifier. The noise figure is reasonably low due to a low device current. The circuit schematic including bias is shown in Fig. 5.

Self-biasing circuitry is applied to reduce the number of bias lines. Hence, the gates are grounded applying inductors and the source voltage is raised with the desired gate–source voltage using a resistor with a bypass capacitor at the FET1's source. This may degrade the conversion gain due to the rather low IF frequency of 110 MHz. A level-shifting diode can be used to avoid this drawback [19]. Applying a spiral inductor as choke inductor for drain bias degrades the conversion gain due to the stray capacitance. A resistor is, therefore, used for dc injection. This has resulted in an increase in the desired dc supply to 5 V. Applying an off-chip choke inductor a 3 V dc supply is sufficient. L-type matching circuits are applied at RF and LO ports, where the grounded inductor also provides the necessary dc grounding of the gates as well as bypassing the IF signal at these ports. A series resonant circuit at LO frequency is used at the IF to short circuit the LO at this port. Two 2 $\times$ 100 μm MESFET's are applied as single-gate FET's. The circuit is fabricated on 2.2-mm^2 GaAs substrate with the layout shown in Fig. 6.

C. Single-Chip Front-End

The previously presented circuits are fabricated on one single-chip circuit by simply cascading these circuits and optimizing for the port mismatch and other changes resulted from the new layout. All functions including the matching networks and biasing circuitry are integrated on-chip. Separate dc power supply is desired, since the mixer applies 5 V. Using one off-chip choke inductor, the mixer can work with 3 V and, hence, a single 3-V power supply is sufficient for the entire front-end. The circuit is fabricated on 2.4 $\times$ 2.4 mm GaAs substrate. The layout is shown in Fig. 7.

III. Results

A. LNA and IR Filter

The measured transfer characteristic is shown in Fig. 8 by means of $|S_{21}|$ within the band of interest.

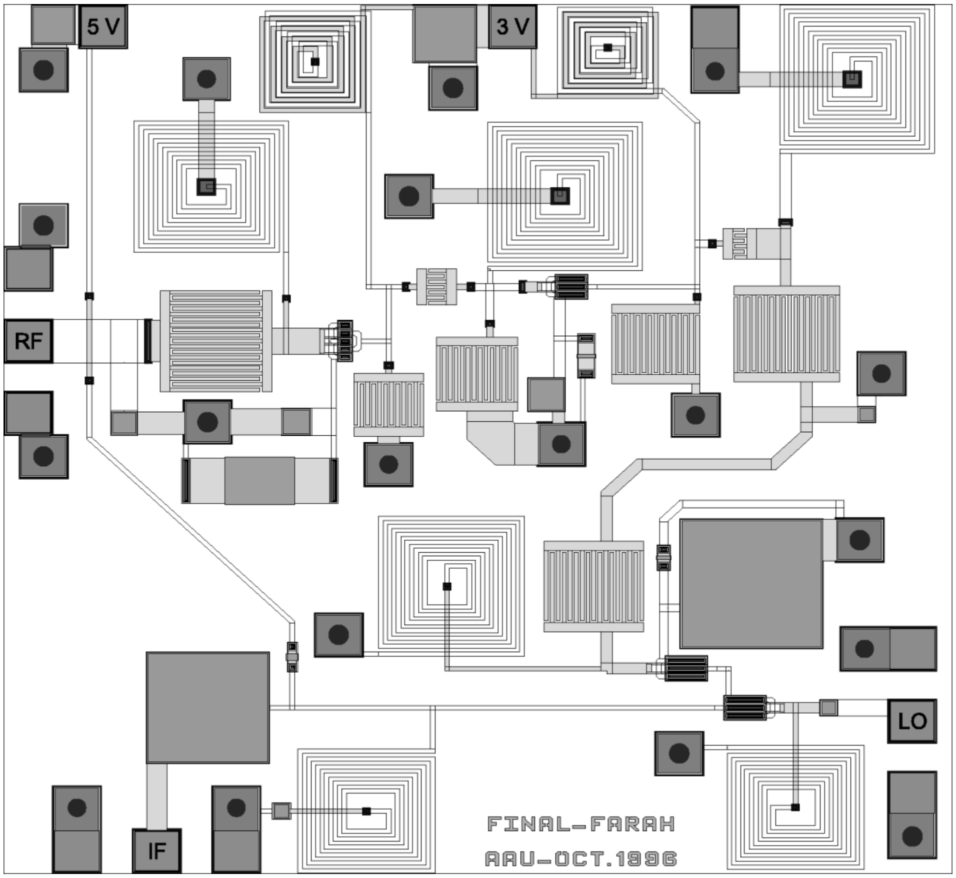

Fig. 7. Circuit layout of the entire front-end.

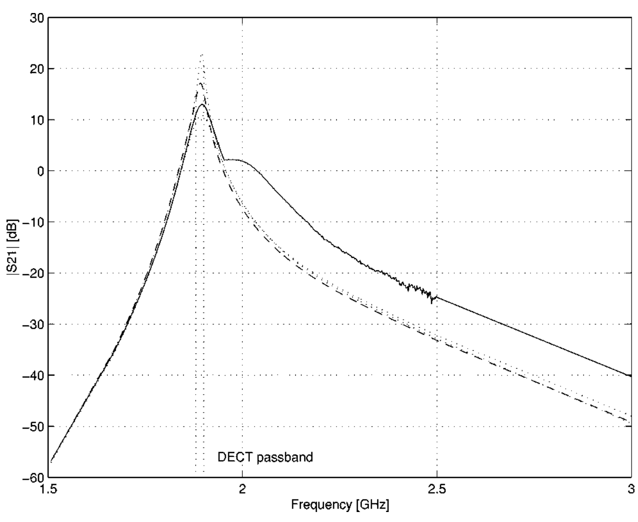

Fig. 8. Measured (solid) and simulated (dashed and dotted) transfer characteristic for the filter.

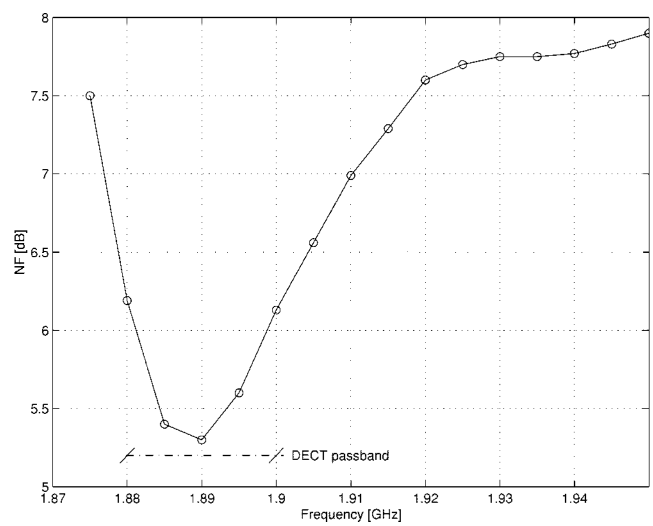

Fig. 9. Measured noise figure for the filter.

The dashed curve on Fig. 8 indicates the simulated transfer characteristic of the center design while the dotted curves are worst-case simulation results due to the variations in the components according to process tolerances. The filter introduces 11–13-dB insertion gain within the DECT band (i.e., 1880–1900 MHz) and has an image rejection higher than 45 dB at the image frequency of 1.68 GHz. $|S_{11}|$ and $|S_{22}|$ are measured less than -15 dB within the DECT band. The measured results match reasonably with the expected ones below 3 GHz. The applied electrical model for the spiral inductors is only valid up to 80% of the spirals' self resonance, i.e., around 2.9 GHz. The difference between measured and simulated results is expected to be caused by intercomponent coupling. The noise performance is illustrated in Fig. 9, which shows a noise figure of 6.2 dB within the DECT band.

Measurements on 20 samples from the same wafer show less than 0.6% variation in the current dissipation and less than 0.2% in the small-signal S-parameters as well as noise performance.

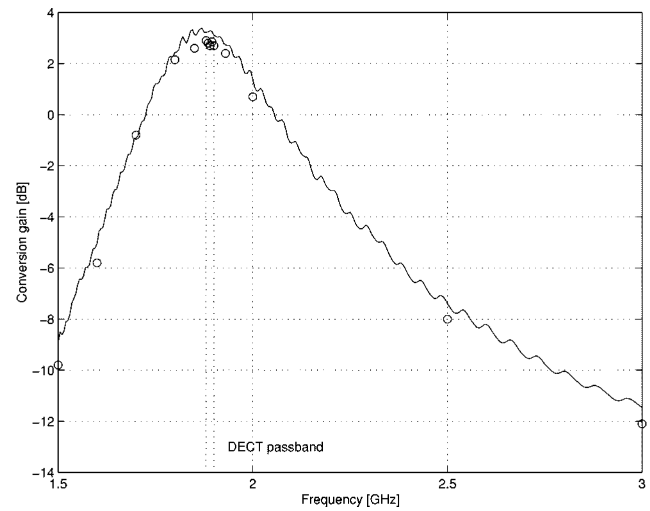

Fig. 10. Measured (circles) and simulated conversion gain for the mixer.

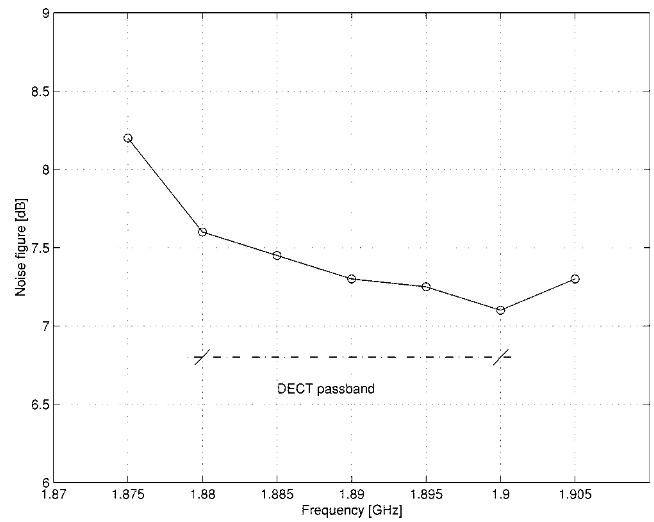

Fig. 11. Measured SSB noise figure for the mixer.

It is worth noting that, even though the filter is active, it does not directly degrade intermodulation distortion (IMD) performance at a system level as it is part of the LNA—the LNA must be there anyway to amplify the generally weak received signal. It should also be noted that the active filter cannot directly be compared with a traditional LNA followed by a passive filter solution, as the active and filtering parts cannot be separated. What is important here is the system performance, where, of course, performance measures such as noise and IMD are also important.

B. Mixer

The frequency-dependent conversion gain is shown in Fig. 10. The LO power and IF frequency are 0 dBm and 110 MHz, respectively. The current dissipation is 3.5 mA with 5-V drain bias. The mixer has 2.5-dB conversion gain within the DECT band. Simulations with an off-chip choke inductor for drain bias instead of the resistor show that the conversion gain can be increased by a minimum of 5 dB.

The LO/RF isolation and LO/IF isolation are measured better than 30 and 17 dB, respectively. The return loss at RF is better than −20 dB, while it is only about −8 dB at LO. Hence, an improvement of the return loss at LO may increase the conversion gain. The two-tone third-order input intercept point is measured to −3.5 dBm. The single sideband (SSB) noise figure is measured better than 8 dB, as shown in Fig. 11.

C. Single-Chip Front-End

The frequency-dependent conversion gain is shown in Fig. 12. The LO power and IF frequency are 0 dBm and 110 MHz, respectively. The current dissipation is 4.8 and 3.6 mA from 3- and 5-V dc supply, respectively. The conversion gain is 15 dB within the DECT band. The image signal at 1.68 GHz is attenuated by a minimum of 53 dB relative to the passband. RF/IF and LO/IF isolation are about 11 and 18 dB, respectively. The 1-dB compression point is measured to −20 dBm, which is well above −33 dBm, the minimum received signal strength indicator (RSSI) level in DECT.

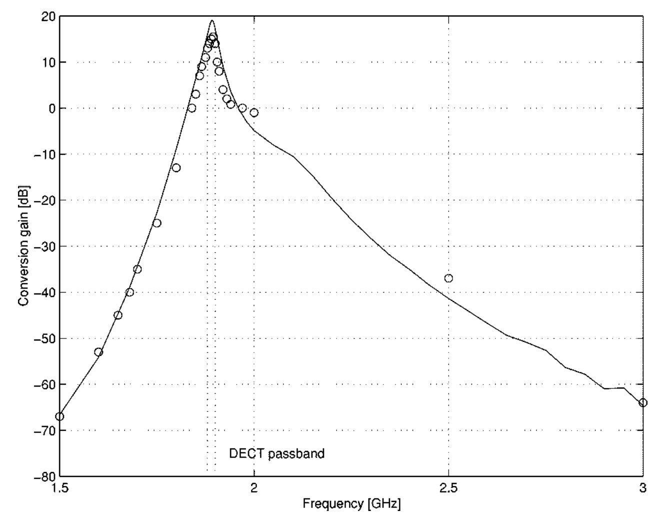

Fig. 12. Measured (circles) and simulated conversion gain for the front-end.

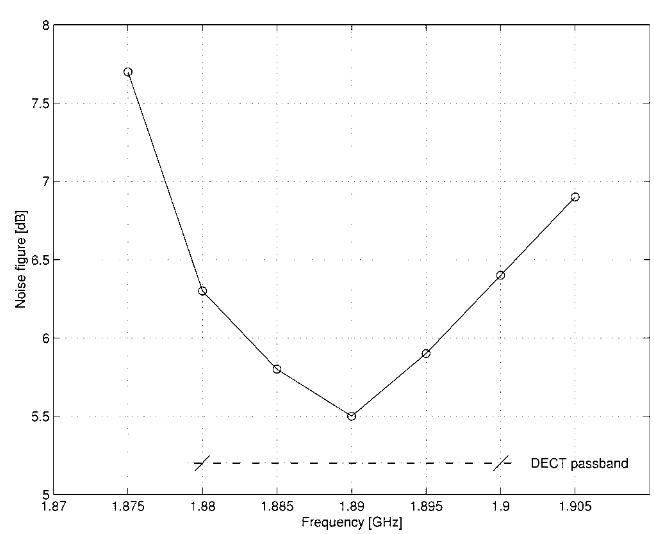

Fig. 13. Measured SSB noise figure for the front-end.

The SSB noise figure is measured better than 6.4 dB, as shown in Fig. 13. Measurements are performed on 15 samples, which show negligible variation in all performance.

IV. Conclusion

GaAs MMIC's with low current and small size were developed for cordless front-end applications. An active image-rejection filter is presented for use in a DECT front-end applying actively coupled passive resonators. With high gain and low noise figure, this circuit also fulfills the demands on the LNA in DECT application. Hence, there is no need for an extra LNA in front of the image-rejection filter in a DECT receiver front-end. A mixer with high LO/RF and RF/LO is also presented applying two single-gate MESFET's in cascode. The LNA/IR filter is integrated with the mixer on one single chip. The front-end exhibits high gain and low noise with very high image rejection dissipating a total of 33-mW power. The high image rejection also eliminates the necessity of an extra RF filter before the LNA.

This solution as the first one within its type requires no off-chip components or post-fabrication tuning and it has good margins for changes in performance due to process tolerances. Hence, the designed circuit is suitable for direct usage in the receiver front-end of commercial cordless and mobile telephone handsets.

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