CAD-Oriented Equivalent-Circuit Modeling of On-Chip Interconnects on Lossy Silicon Substrate

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***Abstract*—A new, comprehensive CAD-oriented modeling methodology for single and coupled interconnects on an Si–SiO_2 substrate is presented. The modeling technique uses a modified quasi-static spectral domain electromagnetic analysis which takes into account the skin effect in the semiconducting substrate. equivalent-circuit models with only ideal lumped elements, representing the broadband characteristics of the interconnects, are extracted. The response of the proposed SPICE compatible equivalent-circuit models is shown to be in good agreement with the frequency-dependent transmission line characteristics of single and general coupled on-chip interconnects.**

***Index Terms*—Coplanar strip line, equivalent circuit, interconnects, microstrip line, on-chip interconnects, silicon substrate, skin effect, spectral domain approach, SPICE model.**

I. Introduction

THERE has been an increasing interest in RF and microwave integrated circuits in CMOS technology due to the fabrication cost advantage of CMOS integrated circuits, especially for wireless consumer applications. Furthermore, the *ad hoc* demand for the system-on-a-chip (SOC) requires mixed-signal integration on a common silicon substrate for high speed analog/RF circuits and high speed digital very large scale integration (VLSI). However, unlike microwave integrated circuits on low loss substrates, such as Alumina and SI–GaAs, the lossy nature of the highly doped silicon substrate can have a significant impact on the performance of on-chip interconnects in CMOS integrated circuits, such as increased loss and dispersion. The frequency-dependent distribution of longitudinal currents in the substrate (which is usually referred as *substrate skin effect*, as well as the shunt currents can give rise to a significant frequency-dependence of the interconnect characteristics, and, therefore, must be included in the interconnect model of the design tool. Interconnect models in available RF/microwave design tools, however, are based on lossless or low-loss substrates and, therefore, may not accurately model interconnects on substrates with significant loss such as in CMOS technology. In this paper we present a new comprehensive CAD-oriented equivalent-circuit modeling methodology for single and coupled interconnects on general lossy silicon substrate (Fig. 1).

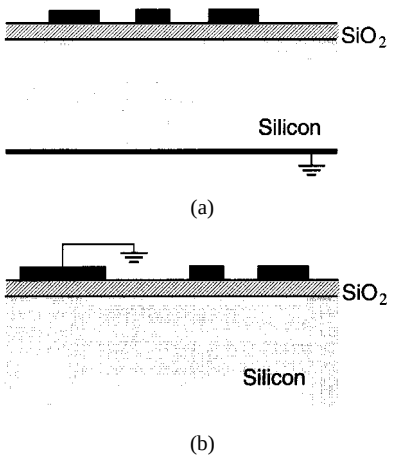

Fig. 1. Typical on-chip interconnects used in silicon-based RF and mixed-signal integrated circuits: (a) with ground plane and (b) co-planar interconnects without ground plane.

The broad-band transmission line behavior of interconnects on lossy silicon substrate (metal-insulator-semiconductor transmission line) has been characterized by experiment (e.g., [1]–[3]), by rigorous analytical and numerical approaches (e.g., [1], [4]–[6]), and more recently in terms of approximate closed-form expressions for the frequency-dependent transmission line parameters [7], [8]. The silicon interconnects represent an important class of lossy and dispersive transmission line structures and, therefore, should be described by generalized telegrapher's equations with equivalent frequency-dependent distributed parameter matrices, i.e., $[R(\omega)]$, $[L(\omega)]$, $[G(\omega)]$, and $[C(\omega)]$ to facilitate the circuit level analysis and design of RF and digital integrated circuits. In recent years, much effort has been put into the analysis and simulation of dispersive interconnects using different techniques including the inverse Laplace Transform approach [9] and methods based on moment matching (e.g., [10]). Although some of these approaches are compatible with general purpose circuit simulators such as SPICE, it is advantageous to represent the broad-band interconnect characteristics in terms of equivalent circuits consisting exclusively of ideal lumped elements.

In this paper, we present new CAD-oriented equivalent-circuit models for single and coupled interconnects on lossy silicon substrate, which accurately model the frequency-depen-

Manuscript received June 15, 2000. This work was supported in part by the NSF Center for the Design of Analog and Digital Integrated Circuits (CDADIC) and Hewlett-Packard Company.

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Publisher Item Identifier S 0018-9480(00)07410-X.

dent behavior of the interconnect structure. The equivalent-circuit models are fully SPICE compatible and can be incorporated directly into common circuit simulators and RF/microwave design tools such as HP–ADS [11]. The modeling technique is based on an efficient quasi-static spectral domain approach [12], which includes the substrate skin effect. In Section II, the quasi-static electromagnetic characterization of on-chip interconnects is described, and results are compared and validated with corresponding full wave solutions. New equivalent-circuit models for single and general asymmetric coupled interconnects are proposed in Section III. The model is developed from the distributed frequency-dependent line parameters using a simple extraction procedure and accurately captures the specific characteristics of on-chip interconnects such as *frequency-dependent loss and coupling*. The proposed lumped element model is further validated in terms of the scattering parameters and time-domain step response of a typical coupled interconnect structure.

II. Quasi-Static Characterization of Interconnects on a Lossy Substrate

The per unit length (p.u.l.) shunt admittance components $C(\omega)$, $G(\omega)$ and series impedance counterparts $L(\omega)$, $R(\omega)$ of single and coupled on-chip interconnects can be efficiently determined by quasi-static analysis, as demonstrated below. Since the quasi-static formulation is readily extended to the multiconductor case, the discussion is focused here on the single conductor case. The shunt admittance components are determined by solving the Laplace equation for the electrostatic potential. To account for the shunt substrate loss, an effective complex dielectric constant $\epsilon_{re} = \epsilon_r - j\sigma/\omega\epsilon_0$ is defined, where ϵ_r and σ are the relative permittivity and the conductivity of the substrate, respectively. The complex capacitance $C(\omega) + G(\omega)/j\omega$ is here efficiently determined using the well-known quasi-static spectral domain approach (e.g., [13], [14]).

For lossless or low loss dielectric substrates, the distributed inductance can be computed directly from the distributed capacitance C_{air} obtained with all dielectric layers removed. However, for substrates with higher conductivity, such as in CMOS technology, the inductance becomes frequency-dependent due to the variation of magnetic flux penetration into the silicon substrate as a function of frequency, which is called the *substrate skin effect*. In this case, the expression for inductance calculation $L = \mu_0\epsilon_0 C_{\text{air}}^{-1}$ is no longer valid since the substrate skin effect results in a frequency-dependent *effective permeability* different from μ_0. Furthermore, the substrate skin effect also contributes to the series resistance $R(\omega)$, in addition to the conductor loss including the skin effect in the interconnect metallization.

The approach for evaluating the p.u.l. series impedance components is analogous to the computation of the shunt admittance components by considering the complex equivalent inductance

$$L(\omega) + R(\omega)/j\omega = \Psi/I = \oint \vec{A}\cdot\vec{dl}/I \qquad (1)$$

where I is the total current on the conductor, Ψ is the magnetic flux linkage p.u.l. associated with the interconnect, and $\vec{A}$ is the vector magnetic potential. For a z-directed current on the conducting strip, only the z-component of the vector magnetic potential $\vec{A}$ is nonzero. In addition, A_z is constant on the conductor

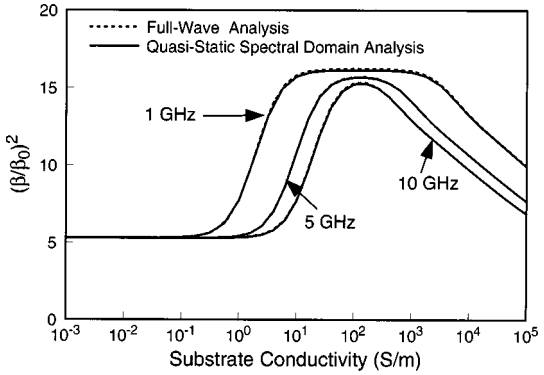


Fig. 2. The square of the normalized phase constant versus substrate conductivity for three different frequencies for a single interconnect (width $=1$ μm, conductor thickness $=1$ μm, $h_1 = 2$ μm, and $h_2 = 500$ μm).

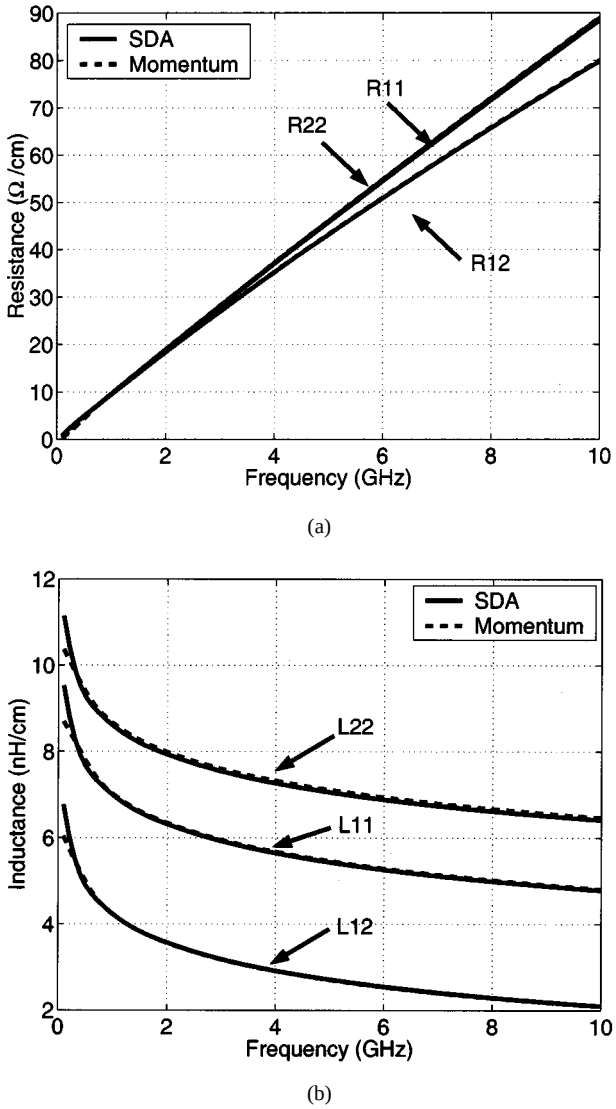


Fig. 3. Self and mutual p.u.l. impedance parameters: (a) resistance and (b) inductance. The curves for the two self-resistances R_{11} and R_{22} are not distinguishable.

surface (zero-thickness) and is equal to the p.u.l. flux linkage Ψ. Therefore, the resistance and inductance p.u.l. can be found by solving for the current distribution on the conductor given the vector magnetic potential on the conductor. A_z satisfies the following equation:

$$\nabla^2 A_z(x, y) - j\omega\mu_0\sigma_i A_z(x, y) = 0 \tag{2}$$

as well as the boundary conditions at the interface between the ith and the $(i+1)$th layer, i.e.,

$$\frac{\partial A_{i+1}(x,y)}{\partial y} - \frac{\partial A_i(x,y)}{\partial y} = \begin{cases} \mu_0 J_z, & \text{on strip} \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

and

$$\frac{\partial A_{i+1}(x,y)}{\partial x} - \frac{\partial A_i(x,y)}{\partial x} = 0. \tag{4}$$

Here, the x-direction is parallel to and the y-direction is perpendicular to the strip.

The quasi-static equation given in (2) can be efficiently solved by a modified spectral domain approach [12]. Equation (2) in the transformed (spectral) domain is given by

$$\frac{d^2}{dy^2}\tilde{A}_z(\alpha, y) = (\alpha^2 + j\omega\mu\sigma_i)\tilde{A}_z(\alpha, y). \tag{5}$$

This equation together with the boundary conditions (3) and (4) reduces to the algebraic form

$$\tilde{A}_z(\alpha) = \tilde{G}_A(\alpha)\tilde{J}_z(\alpha) \tag{6}$$

which is evaluated at the oxide-air interface (plane of interconnect) in Fig. 1(a). For the microstrip structure shown in Fig. 1(a), a suitable Green's function is given by

$$\tilde{G}_A(\alpha) = \frac{\mu_0}{\alpha + \alpha_1 p} \tag{7}$$

with

$$p = \frac{\alpha_1 + \alpha_2 \coth(\alpha_2 h_2)\coth(\alpha_1 h_1)}{\alpha_2 \coth(\alpha_2 h_2) + \alpha_1 \coth(\alpha_1 h_1)} \tag{8}$$

where $\alpha_i = \sqrt{\alpha^2 + j\omega\mu_0\sigma_i}$, and h_1 and h_2 are the thicknesses of the SiO_2 layer and Si layer, respectively. The unknown strip current density in (4) is expanded in terms of Chebyshev basis functions. A set of algebraic equations is obtained by applying the Galerkin method to (7) and its solution leads to the coefficients of the basis function for the strip current density.

The spectral domain formulation has been extended to the coplanar strip line interconnect structure (without ground plane) as shown in Fig. 1(b). Coplanar structures are useful for handling active devices in the integrated circuits where the number of vias can be significantly reduced. The spectral domain Green's function of magnetic potential for the coplanar structure shown in Fig. 1(b) is given by

$$\tilde{G}_{Ac}(\alpha) = \frac{1}{\alpha + \alpha_1 \cdot \dfrac{\alpha_1 + \alpha_2 \coth(\alpha_1 h_1) q}{\alpha_2 q + \alpha_1 \coth(\alpha_1 h_1)}} \tag{9}$$

with

$$q = \frac{\alpha_2 + \alpha \coth(\alpha_2 h_2)}{\alpha + \alpha_2 \coth(\alpha_2 h_2)} \tag{10}$$

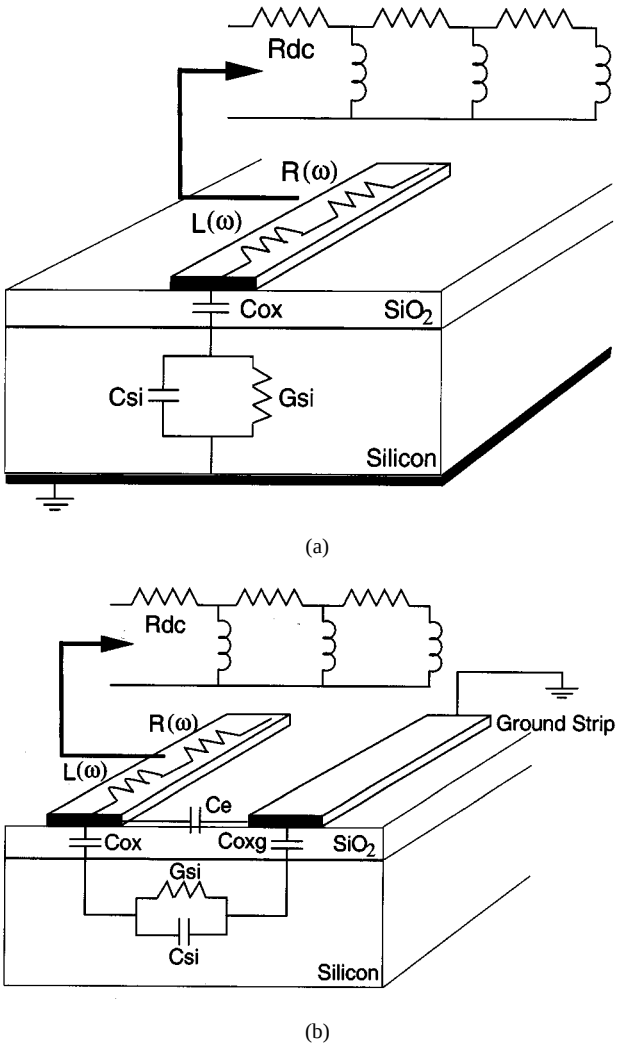


Fig. 4. Equivalent-circuit model for singel interconnect on silicon substrate: (a) microstrip configuration and (b) coplanar-strip configuration.

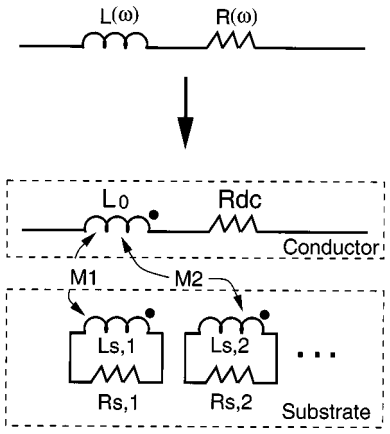
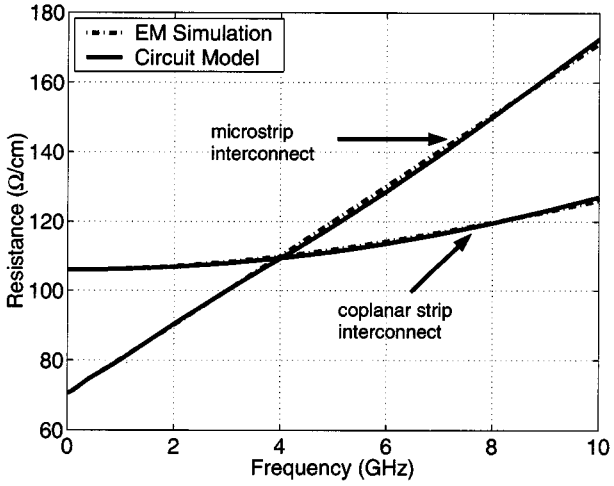
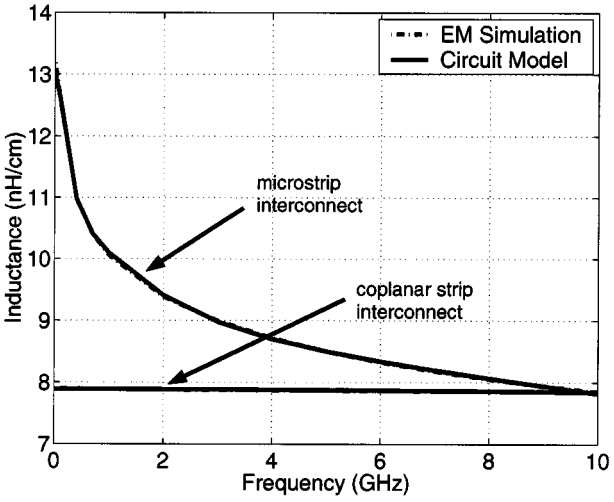


Fig. 5. New equivalent-circuit model for p.u.l. impedance based on effective substrate current loops.

where h_1 and h_2 are the thickness of the SiO_2 layer and Si layer, respectively, and $\alpha_i = \sqrt{\alpha^2 + j\omega\mu_0\sigma_i}$. With the ground plane removed, the complex *partial inductances* for the signal conductor(s) and the ground conductor, respectively, are obtained.

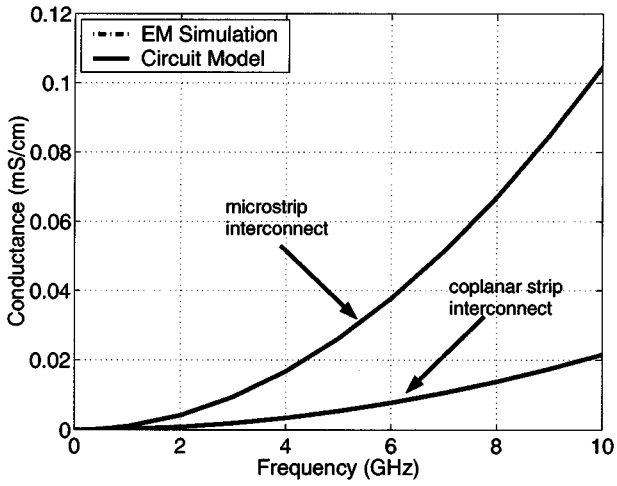


(a)

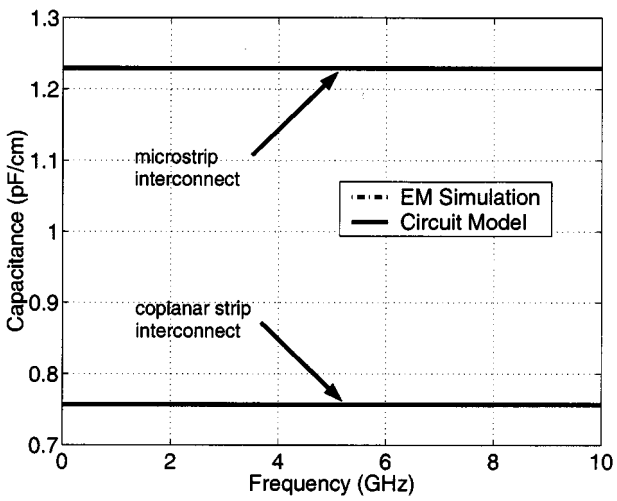


(b)

Fig. 6. The computed and equivalent-circuit model frequence response of (a) resistance and (b) inductance.



(a)



(b)

Fig. 7. The computed and equivalent-circuit model frequence response of (a) conductance and (b) capacitance.

The effective inductance and associated resistance of a single coplanar interconnect are given by

$$L(\omega) = L_s(\omega) + L_g(\omega) - 2L_{sg}(\omega) \tag{11}$$

and

$$R(\omega) = R_s(\omega) + R_g(\omega) - 2R_{sg}(\omega). \tag{12}$$

Here $L_s(\omega)$ and $L_g(\omega)$ are the p.u.l. partial inductances of the signal conductor and the ground conductor, respectively, and L_{sg} is the p.u.l. partial mutual inductance between the signal and ground conductor. $R_s(\omega)$, $R_g(\omega)$, and $R_{sg}(\omega)$ are self and mutual resistances associated with the corresponding partial inductances.

It should be emphasized that the distributed resistance obtained from the imaginary part of the complex inductance results from the skin effect in the semiconducting silicon substrate. For conductors with finite thickness, the contribution of the conducting strip including the conductor skin effect to the distributed resistance $R(\omega)$ is calculated separately and added to $R(\omega)$.

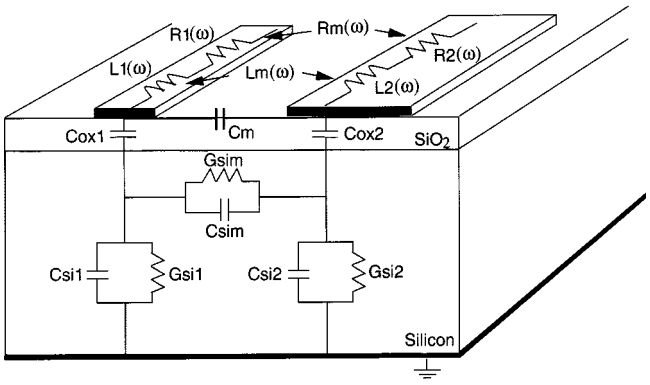


Fig. 8. P.u.l. equivalent-circuit model for the shunt self- and mutual admittances of a general coupled interconnect structure on a Si–SiO_2 substrate.

Fig. 2 illustrates the significance of the frequency-dependent inductance in the propagation characteristics of a single interconnect on a lossy substrate. With increasing substrate conductivity, the interconnect behavior goes from the dielectric quasi-TEM mode through the slow-wave mode region to

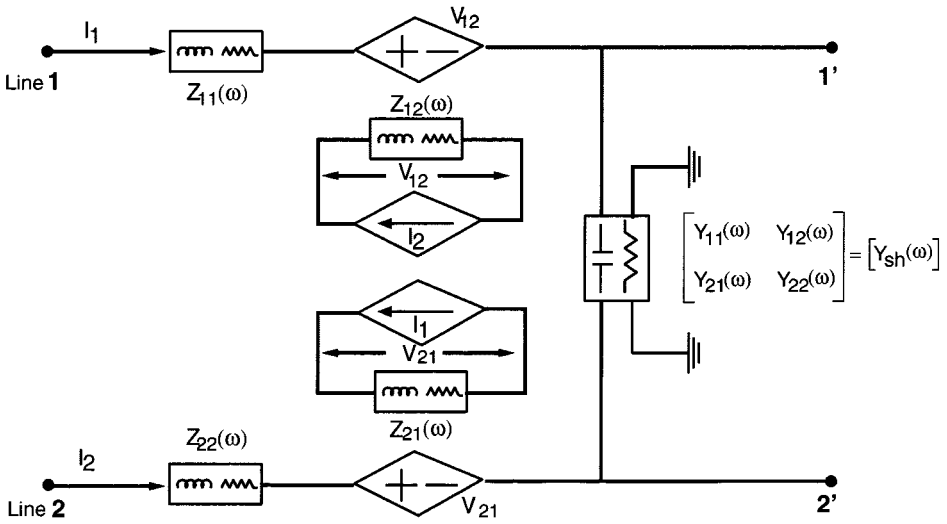


Fig. 9. P.u.l. equivalent-circuit model for a general asymmetric coupled on-chip interconnect structure in CMOS technology, where the explicit equivalent-circuit topologies for $Z_{11}(\omega)$, $Z_{12}(\omega)$, and $Z_{22}(\omega)$ are shown in Fig. 5 (impedance part) and the explicit equivalent-circuit topoloy for the shunt admittance network $[Y_{sh}(\omega)]$ is shown in Fig. 8.

the skin-effect mode [1]. In the skin-effect region the line inductance is reduced due to the presence of the longitudinal substrate current. To demonstrate the accuracy of the quasi-static calculation of the interconnect line parameters, Fig. 2 also includes the corresponding full wave solution.

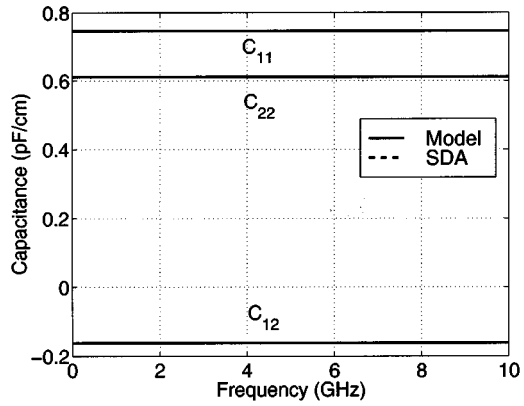
The frequency-dependent p.u.l. inductance and resistance parameters for an *asymmetrically* coupled interconnect structure on a heavily doped CMOS substrate (resistivity $\rho_{si} = 0.01$ Ω-cm) are shown in Fig. 3. The interconnects are placed on a 500-μm silicon substrate with a 2-μm oxide layer. The width of the conductors is 25 μm and 10 μm, respectively, and the spacing between the two conductors is 10 μm. To emphasize the series resistance due to the skin effect in the silicon substrate, the conductors are chosen to have zero resistivity and thickness. Since the conductor width does not significantly affect the resistance contribution from the lossy substrate, the curves for the two self-resistances in Fig. 3(a) are not distinguishable. This "intrinsic loss" phenomenon illustrates an important characteristic of on-chip interconnects on lossy substrate. The p.u.l. parameters are also extracted from the S-parameters obtained by the full wave electromagnetic field solver HP Momentum [11]. The comparison shows good agreement between the quasi-static and the full wave solutions.

III. Equivalent Circuit Modeling

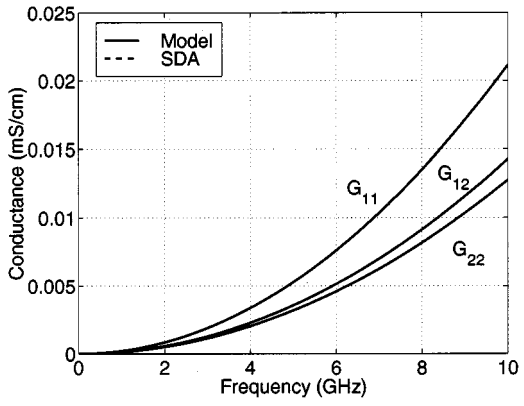
In this section, equivalent-circuit models consisting of ideal lumped elements are developed for both single and general asymmetric coupled on-chip interconnects. The model parameters are extracted from the frequency-dependent line parameters obtained by the quasi-static electromagnetic analysis described in Section II.

A. Single Interconnect

The equivalent-circuit model for a basic cell, which represents an electrically short single interconnect, is shown in Fig. 4. For longer on-chip interconnects the basic cells are cascaded.



(a)



(b)

Fig. 10. Self and mutual p.u.l. shunt admittance components: (a) capacitance and (b) conductance. The solid lines in the figures are obtained with the equivalent-circuit model, and the dashed lines are the result from the spectral domain method.

The equivalent-circuit model for the p.u.l. shunt admittance $G(\omega) + j\omega C(\omega)$ is based on the physical structure and consists of ideal R and C elements. The equivalent circuit used for a

microstrip interconnect consists of the capacitance C_{ox} representing the oxide layer, in series with the capacitance C_{si} and parallel conductance G_{si} to represent the semiconducting substrate [Fig. 4(a)]. The three equivalent-circuit parameters are extracted from the shunt admittance $G(\omega) + j\omega C(\omega)$ at one frequency point by using the additional relationship $G_{si}/C_{si} = \sigma/\epsilon$. The agreement between the extracted model and the frequency-dependent admittance is excellent and found to be virtually independent of the choice of matching frequency [15]. For a coplanar strip interconnect, the equivalent circuit includes additional capacitances representing the coupling capacitance C_e between the signal conductor and the ground conductor at the air-oxide interface, and the capacitance C_{oxg} between the ground conductor and the bulk silicon substrate.

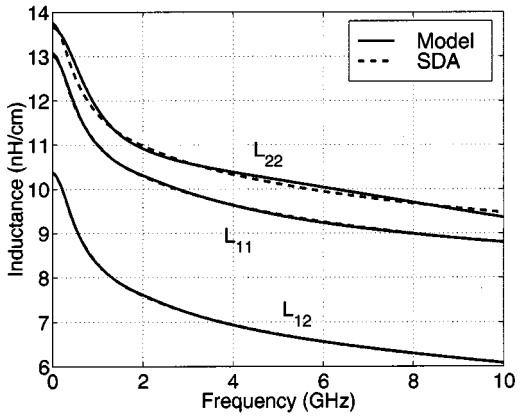
The equivalent-circuit model for the p.u.l. series impedance $R(\omega) + j\omega L(\omega)$ is derived by constructing a rational function with forced passivity from the computed frequency-dependent series impedance [16]. The approximating rational function has the general form

$$F(j\omega) = \frac{A_0 + A_1(j\omega) + A_2(j\omega)^2 + \cdots + A_m(j\omega)^m}{1 + B_1(j\omega) + B_2(j\omega)^2 + \cdots + B_n(j\omega)^n} \tag{13}$$

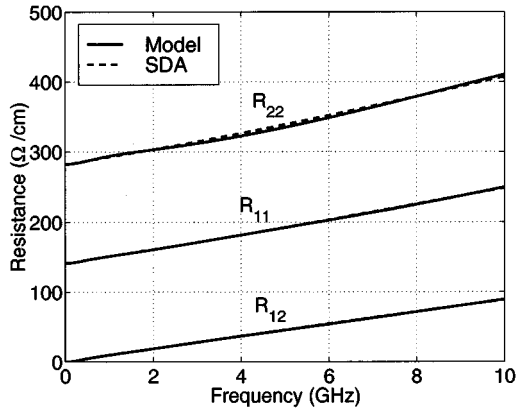
and can be synthesized in terms of ideal R and L elements in a ladder-type canonical topology [17]–[19] as shown in Fig. 4. Here, an alternative equivalent circuit providing more physical insight is proposed. In the model shown in Fig. 5, the inductance L_0 and resistance R_{dc} in the main branch represent the interconnect inductance and resistance at the low frequency limit where the substrate skin effect can be neglected. The inductance $L_{s,i}$ and resistance $R_{s,i}$ simulate the ith effective substrate current loop. The inductive coupling between the metallization and the conducting substrate is represented by the mutual inductances M_i between $L_{s,i}$ and L_0. The equivalent series impedance in the model can be written as

$$Z(j\omega) = R_{dc} + j\omega L_0 - \frac{M_1(j\omega)^2}{j\omega L_{s,1} + R_{s,1}} - \frac{M_2(j\omega)^2}{j\omega L_{s,2} + R_{s,2}} - \cdots. \tag{14}$$

The lumped element values can easily be extracted from the approximated rational polynomial function. Typically, the fitting process for rational polynomial approximation over a broad-band frequency range leads to an overdetermined linear system of equations [20], [21]. Here, a robust rational approximation approach similar to [22] is employed to determine the coefficients of the numerator and denominator polynomials. The order of the rational approximation depends on how much $R(\omega)$ and $L(\omega)$ vary with frequency, which is mainly determined by the substrate conductivity and thickness. Simulations for various substrate structures have shown that up to three effective substrate current loops typically are sufficient for modeling medium and heavily doped silicon substrates. In addition, the proposed equivalent-circuit model can easily be extended to include the skin effect in the interconnect metallization.



(a)



(b)

Fig. 11. Self and mutual p.u.l. series impedance components (a) inductance and (b) resistance. The solid lines in the figures are obtained with the equivalent-circuit model, and the dashed lines are the results from the spectral domain method.

To exemplify the accuracy of the proposed models, the equivalent circuits for a microstrip interconnect and a coplanar strip interconnect are extracted from quasi-static electromagnetic simulation. Both interconnects are on a 500-μm silicon substrate (resistivity $\rho_{si} = 0.01$ Ω-cm) with a 2-μm oxide layer. The cross section of the microstrip is 4 μm by 1μm. The cross sections of the signal conductor and the ground conductor in the coplanar strip structure are 4 μm by 1μm and 8 μm by 1 μm, respectively, and the spacing between the signal and the ground conductor is 8 μm. As shown in Figs. 6 and 7, the frequency response of the extracted equivalent-circuit model is in excellent agreement with that computed from the quasi-static spectral domain approach. As expected, the lossy silicon substrate has more significant impact on the frequency-dependence of the line parameters for microstrip interconnect as compared to the coplanar strip interconnect.

B. General Asymmetric Coupled Interconnects

A common approach to analyzing multiple coupled lines uses the normal mode method (e.g., [24]–[26]). However, the decoupling of general dispersive asymmetric coupled interconnects in terms of a normal mode approach leads to frequency-dependent complex controlled sources, which cannot be directly imple-

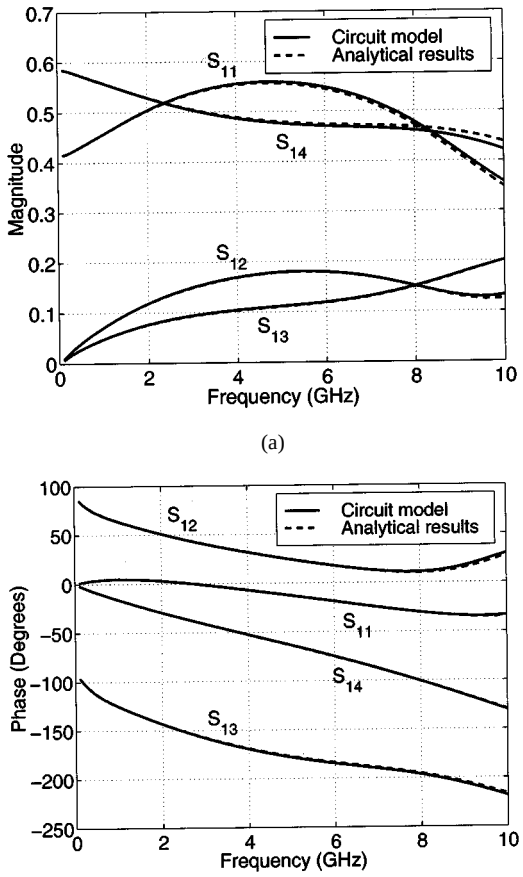


Fig. 12. S-parameter validation for modeling of asymmetric coupled interconnects: (a) magnitude and (b) phase.

mented in standard circuit simulators. In this section, the modeling technique for a single interconnect described above is extended to a fully SPICE-compatible equivalent-circuit model for general asymmetric coupled interconnects.

First, the self and mutual p.u.l. shunt admittances are synthesized in terms of a network composed of R, C lumped elements. A new equivalent-circuit topology for the shunt admittances of general coupled on-chip microstrip interconnects based upon the physical substrate struture is shown in Fig. 8. In this model, C_{ox1} and C_{ox2} represent the oxide capacitances between the conductors and the bulk substrate, and C_m represents the capacitive coupling through the oxide layer as well as air. The equivalent circuit for the silicon substrate has the same 2-port π topology as for the oxide layer where each capacitance is replaced by a parallel combination of capacitance and conductance to represent the lossy nature of the silicon substrate. The extraction technique is based on a network (matrix) decomposition and pole extraction. The open-circuit impedance matrix corresponding to the shunt admittance matrix Y_{sh} can be expressed by the series connection of two 2-port subnetworks

$$[Z_y] = [Y_{sh}]^{-1} = [Z_{ox}] + [Z_{\rm Si}] \tag{15}$$

where the impedance matrices $[Z_{ox}]$ and $[Z_{\rm Si}]$ correspond to the π-type network representing the oxide layer and the silicon substrate, respectively. The three capacitances representing the oxide layer can be extracted first by identifying that each element of matrix $[Z_{ox}]$ has a pole at $\omega = 0$ while the poles of $[Z_{\rm Si}]$ are nonzero. Therefore, C_{ox1}, C_{ox2}, and C_m are obtained by extracting the poles at $\omega = 0$ from each element of $[Z_y]$ by means of a rational polynomial approximation procedure. The circuit elements representing the silicon layer correspond directly to the entries in $[Z_{\rm Si}]^{-1}$, which can be obtained by subtracting the known $[Z_{ox}]$ from $[Z_y]$.

Likewise, the self and mutual p.u.l. series impedances are represented by R, L lumped elements. Consider the differential voltages in the transmission line equations for two coupled lines

$$-\frac{dV_1}{dx} = z_{11}(\omega)I_1 + z_{12}(\omega)I_2 \tag{16}$$

$$-\frac{dV_2}{dx} = z_{21}(\omega)I_1 + z_{22}(\omega)I_2 \tag{17}$$

where V_1, V_2 and I_1, I_2 are the voltages and currents on the two lines, respectively, and $z_{ij}(\omega) = R_{ij}(\omega) + j\omega L_{ij}(\omega)$, are the p.u.l. self and mutual impedances. Introducing two auxiliary voltage sources, $V_{12} = z_{12}(\omega)I_2$ and $V_{21} = z_{21}(\omega)I_1$, (16) and (17) can be written as

$$-\frac{dV_1}{dx} = z_{11}(\omega)I_1 + V_{12} \tag{18}$$

$$-\frac{dV_2}{dx} = z_{22}(\omega)I_2 + V_{21}. \tag{19}$$

Equations (18) and (19) lead to the equivalent-circuit representation for coupled interconnects shown in Fig. 9. In this model, self and mutual p.u.l. impedance parameters are realized in terms of R, L lumped elements via rational approximations in the same way as for a single interconnect. Thus, the frequency-dependent resistive and inductive coupling between the lines is modeled by a set of ideal current-controlled current sources (CCCS) and voltage-controlled voltage sources (VCVS) with real and constant coefficients (=1.0).

The models for the series impedance components and the shunt admittance components are combined in a π or a Γ configuration forming a complete p.u.l. equivalent circuit for general coupled interconnects (Fig. 9). This model can be extended to general multiple coupled interconnects.

IV. Model and Simulation Results

To illustrate and validate the proposed equivalent-circuit modeling methodology, an asymmetric coupled interconnect structure on a 300-μm silicon substrate (resistivity $\rho_{\rm Si} = 0.01\ \Omega \cdot$ cm) with a 3-μm oxide layer is considered. The cross sections of the conductors are 2 μm by 1 μm and 1 μm by 1 μm, respectively. The spacing between the two conductors is 2 μm. The interconnect structure is 5.0 mm long. The modeling procedure is detailed below.

1) The structure is solved for its p.u.l. $[R]$, $[L]$, $[G]$, and $[C]$ matrices using the quasi-TEM spectral domain methods described in Section II.
2) The frequency-dependent p.u.l. parameters are synthesized in terms of four-port lumped equivalent circuits as shown in Fig. 9 and described in the previous section.

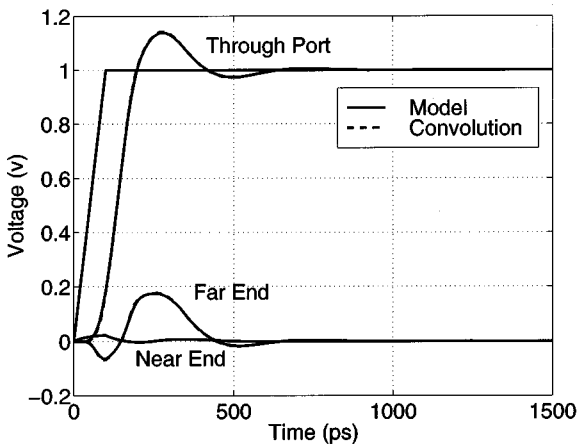


Fig. 13. Voltage step response of an asymmetric coupled interconnect structure.

3) The length of a basic cell (hence, the total number of cells, N) is determined [23], and the lumped elements are scaled to the chosen length. In this example, $N = 10$ basic cells are used.
4) The N cells are cascaded to form a complete equivalent circuit for the given structure.

Figs. 10 and 11 show the frequency-dependent p.u.l. parameters. The solid lines are computed from the equivalent-circuit model and the dashed lines are the results from the quasi-static electromagnetic characterization. The frequency response of the extracted equivalent-circuit model agrees well with that computed by the spectral domain approach.

In order to evaluate the performance of the cascaded equivalent-circuit model, the four-port scattering parameters are rigorously computed from a normal mode approach for asymmetric coupled transmission lines in an inhomogeneous medium [27]. Fig. 12 shows the comparison of the S-parameters from analytical results and from the simulation of the cascaded equivalent-circuit model in HP–ADS. To further illustrate the broad-band performance of the proposed interconnect model, a time-domain analysis for a voltage step input is performed for the asymmetric coupled interconnect structure. The proposed equivalent-circuit model has been implemented in the circuit simulator as a subcircuit. The results presented in Fig. 13 show excellent agreement between the circuit model approach and the direct implementation based on convolution.

V. Conclusion

We have developed a comprehensive modeling approach for frequency-dependent on-chip interconnects on a lossy (CMOS) substrate. The modified quasi-static spectral domain approach provides accurate interconnect characteristics as validated by comparison with full wave solutions. The extracted equivalent-circuit models consist of only ideal SPICE elements and accurately represent the broad-band frequency response of the frequency-dependent interconnects. The models can be readily incorporated into common circuit simulators as subcircuit prototype and should be useful in the design of RF and mixed-signal integrated circuits in CMOS technology.

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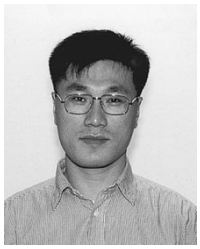

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