A New Lumped-Elements Power-Combining Amplifier Based on an Extended Resonance Technique

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***Abstract*—A technique for combining power FETs in the output stage of a power amplifier is presented. The active devices are combined with simple inductor/capacitor networks and can be laid out across a single die while still allowing each device to be independently accessed for biasing. The inductors can range from fully integrated spirals to simple wire bonds, making this technique applicable over a broad range of frequencies. For linear RF power applications this is an effective technique for spreading more heat, while at high frequencies the junction parasitics are easily absorbed into this type of design. DC losses are minimized since each device can be biased individually, furthermore, it is possible to adjust the bias separately for each device to account for device nonuniformity across the die.**

***Index Terms*—Extended resonance, power amplifier, power combining.**

I. Introduction

PROPER thermal management is crucial to successful RF power amplifier design, particularly during low-efficiency, linear operation. When the operating temperature of the device rises, the threshold voltage, transconductance, and output resistance are among the critical devices parameters that are affected. In extreme cases, the device may self-bias and oscillate uncontrollably. Emerging wide-band and multicarrier modulation formats are particularly susceptible to this effect, since high peak-to-average power ratios demand that the amplifier be backed off several decibels from saturation. For typical surface-mount power amplifiers, the thermal path follows the die, through the die attach material, through the package to an external heat sink. Device layout should account for proper gate finger spacing within a unit cell FET to prevent overheating. Multiple FET cells are often combined in parallel, as in Fig. 1(a), to increase the heat spread through the GaAs [1], [2]. Arranged this way, however, the dc bias is usually applied at a single point off-chip since it is difficult to access each FET cell individually. Thus, there is additional dc power loss through the RF matching circuit, which will degrade the power-added efficiency. This can be avoided by laying out the FET cells in series [3], [4], as shown in Fig. 1(b), where the dc and RF paths are separate. Furthermore, the bias on each FET can be adjusted independently when the RF power dividing/combining functions are implemented with a series capacitor between each FET. This is particularly useful when compensating for nonuniform threshold voltages among the devices.

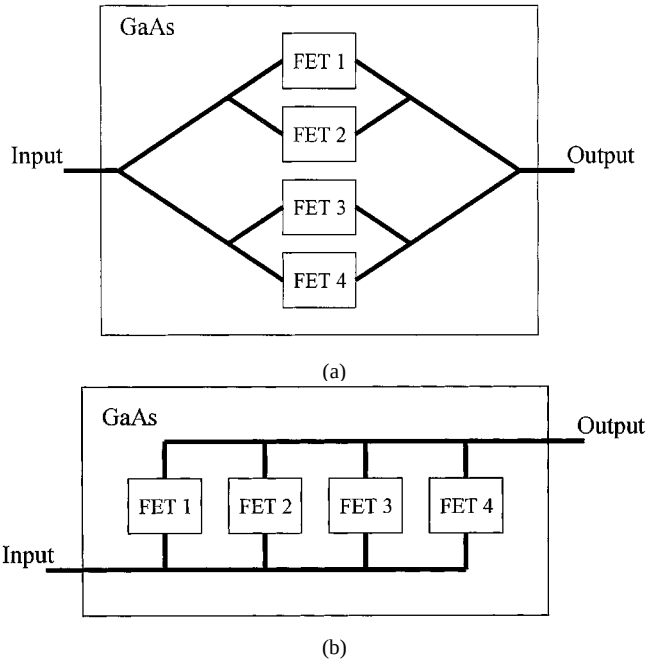

Fig. 1. (a) Parallel FET combining. (b) Series FET combining

An extended resonance technique was recently introduced [5] and [6] to combine MESFETs as shown in Fig. 1(b) using transmission lines. In this paper, the extended resonance approach is implemented with lumped inductors and capacitors, which further reduce the overall size of the resulting power-combining structure. The following analysis covers the implementation of this approach taking into account the finite Q and parasitics of the on-chip components. The power-combining efficiency is derived based on the number of FETs and the Q values of the series-combining elements in the circuit.

II. Design

A generic N-way extended resonance power-combining amplifier is shown in Fig. 2. In Fig. 2(a), the gates of the devices are series connected with inductors L_{g1} through $L_{g(N-1)}$, and the drains of the devices are series connected with L_{d1} through $L_{d(N-1)}$. Although superficially similar to a chain combiner or a distributed amplifier, this technique has its own unique method

Manuscript received November 4, 1998.

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Publisher Item Identifier S 0018-9480(00)07406-8.

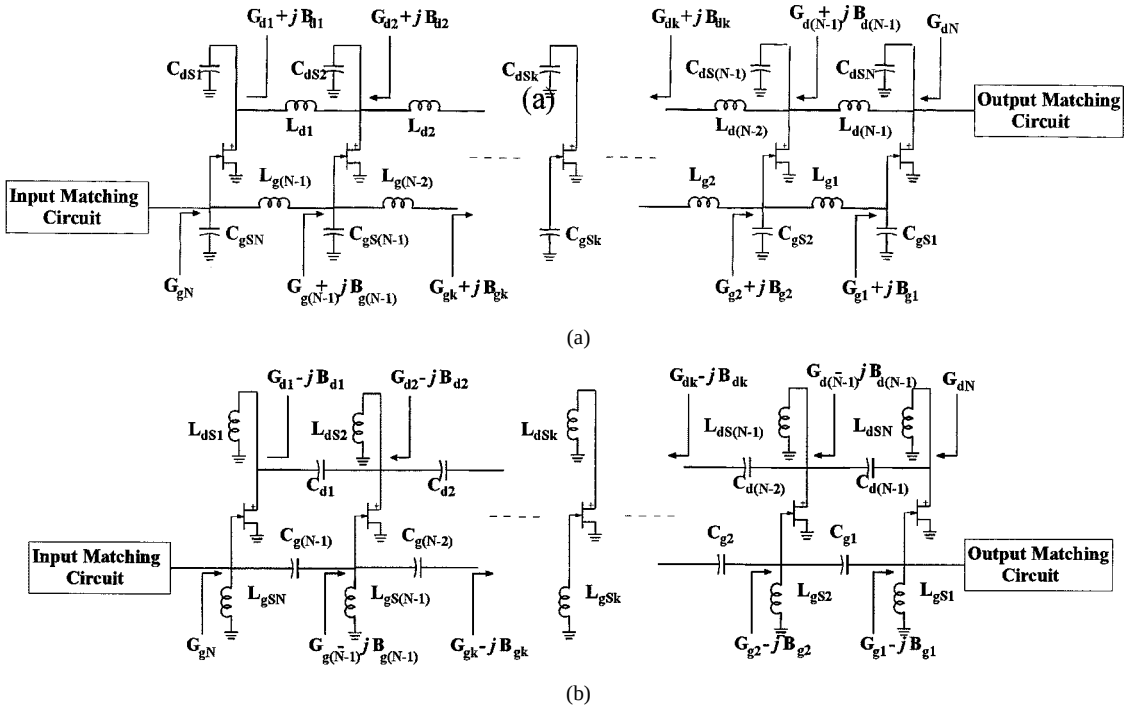


Fig. 2. (a) Inductively coupled devices in an N-way extended resonance power-combining amplifier. (b) Capacitively coupled devices in an N-way extended resonance power-combining amplifier.

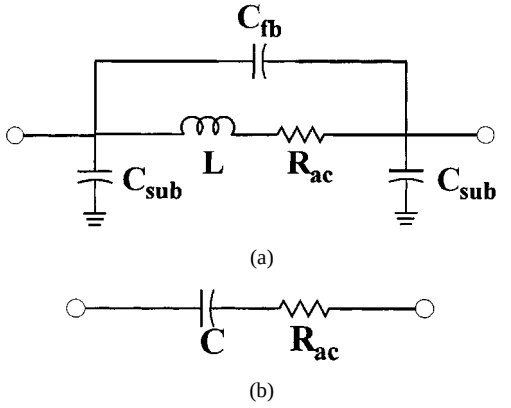


Fig. 3. (a) Spiral inductor model. (b) MIM capacitor model.

of dividing the input power equally between each gate and then combining the output power in a coherent manner from each drain. This is done by converting the admittance at a given gate (or drain) junction of each FET to the conjugate admittance at the gate (or drain) at an adjacent FET, whereby the susceptance of this conjugate admittance cancels out a portion of the susceptance at the FET junction. Meanwhile, the real component of the gate (or drain) admittance accumulates such that the input conductance is N times the input conductance of a single FET, and the output conductance is N times the effective output conductance of a single FET. This results in equal voltages and equal currents at the gates and the drains. Capacitors C_{g1} through $C_{g(N-1)}$ in the input circuit and C_{d1} through $C_{d(N-1)}$ in the output circuit are used to help equalize the phase delays between each FET in the input and output circuits.

The primary functional difference between the amplifier circuit in Fig. 2(b) and the circuit in Fig. 2(a) is that the dc bias on each gate/drain can be adjusted individually since the FETs in Fig. 2(b) are dc isolated. The gates are connected in series with capacitors C_{g1} through $C_{g(N-1)}$, and the drains are connected in series with capacitors C_{d1} through $C_{d(N-1)}$. Inductors L_{g1} through $L_{g(N-1)}$, in the input circuit and L_{d1} through $L_{d(N-1)}$ in the output circuit, aid in equalizing the phase delays between each FET the input and output circuits.

To account for the parasitics typically associated with integrated inductors and capacitors, generic models are given for these elements in Fig. 3(a) and (b). The spiral inductor model in Fig. 3(a) includes the intrinsic feedback capacitance, C_f (a function of L), the capacitive coupling through the substrate $C_{\rm sub}$, and the frequency-dependent conductor loss R_{ac}. The MIM capacitor model in Fig. 3(b) includes the parallel plate capacitance C and the conductor loss R_{ac}.

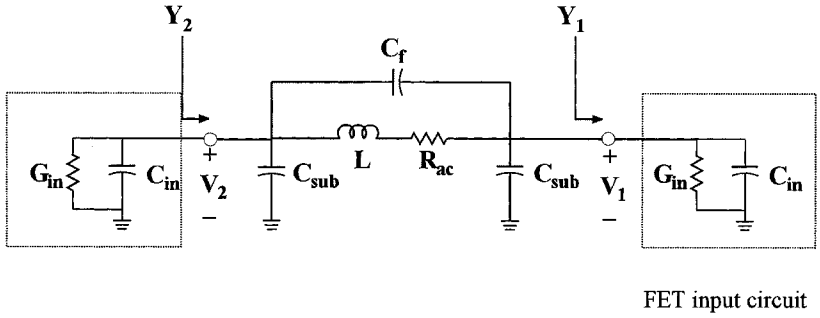
A. Inductively Coupled Devices

To demonstrate a simple two-way power divider across a single inductor, an equivalent MESFET input admittance, $Y_1 = G_{\rm in} + j2\pi f_o C_{\rm in}$, is located at each end of the inductor shown in Fig. 4(a). The admittance looking into the overall inductor model is $Y_2 = G_2 + jB_2$, where it is shown in (1) and (2) at the bottom of the following page. When applying a voltage source at terminal 2 of the inductor, the resulting voltage at the device terminals is found from the transfer function

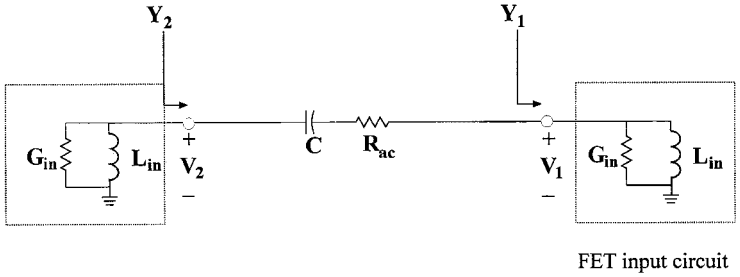
$$V_2 = V_1 \frac{G_2 + j\left(B_2 - 2\pi f_0 C_{\rm sub}\right)}{G_{\rm in} + j2\pi f_0 \left(C_{\rm in} + C_{\rm sub}\right)} \tag{3}$$

where V_1 and V_2 are the voltages at terminals 1 and 2 of the inductor, respectively. Enforcing the condition $|V_1| = |V_2|$, (3) can be rewritten as

$$G_2^2 + \left(B_2 - 2\pi f_0 C_{\rm sub}\right)^2 = G_{\rm in}^2 + \left(2\pi f_0\right)^2 \left(C_{\rm in} + C_{\rm sub}\right)^2 \tag{4}$$



(a)



(b)

Fig. 4. Power dividing based on: (a) inductively coupled and (b) capacitively coupled FET input circuits.

where the task is to determine the correct value of L that will satisfy (4). The inductor model in Fig. 3(a) will be considered for three separate cases:

1) R_{ac}, C_f, and $C_{\rm sub} = 0$ (ideal inductor);
2) $R_{ac} = 0$ (lossless inductor);
3) C_f and $C_{\rm sub} = 0$ (lossy inductor).

This will allow us to determine how strongly each of the inductor parasitics impacts the overall design and whether any of these effects can ultimately be neglected.

R_{ac}, C_f, and $C_{\rm sub} = 0$ (Ideal Inductor): For an ideal inductor, (1) and (2) reduce to

$$G_2 = \frac{G_{\rm in}}{1 + 2\pi f_0 L\left(2\pi f_0 L G_{\rm in}^2 - 4\pi f_0 C_{\rm in} + (2\pi f_0)^3 L C_{\rm in}^2\right)} \tag{5}$$

$$B_2 = \frac{2\pi f_0 C_{\rm in} - 2\pi f_0 L G_{\rm in}^2 - (2\pi f_0)^3 L C_{\rm in}^2}{1 + 2\pi f_0 L\left(2\pi f_0 L G_{\rm in}^2 - 4\pi f_0 C_{\rm in} + (2\pi f_0)^3 L C_{\rm in}^2\right)}. \tag{6}$$

Substituting (5) and (6) into (4), it can easily be shown that

$$L = \frac{2C_{\rm in}}{G_{\rm in}^2 + (2\pi f_0)^2 C_{\rm in}^2}. \tag{7}$$

The voltage phase delay across the inductor is found from (3), to be

$$\phi_{12} = -2\arctan\frac{2\pi f_0 C_{\rm in}}{G_{\rm in}}. \tag{8}$$

$R_{ac} = 0$ (Lossless Inductor): For a lossless inductor that has only capacitive parasitics, (1) and (2) reduce to (9) and (10),

$$G_2 = \frac{\left[G_{\rm in}\left(1-(2\pi f_0)^2 L C_f\right) - (2\pi f_0)^2 R_{ac} C_f\left(C_{\rm sub}+C_{\rm in}\right)\right]\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]}{\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]^2 + \left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]^2}$$
$$+ \frac{2\pi f_0\left[R_{ac}G_{\rm in}C_f + \left(C_{\rm sub}+C_{\rm in}\right)\left(1-(2\pi f_0)^2 L C_f\right)\right]\left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]}{\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]^2 + \left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]^2} \tag{1}$$

and

$$B_2 = \frac{2\pi f_0\left[R_{ac}G_{\rm in}C_f + \left(C_{\rm sub}+C_{\rm in}\right)\left(1-(2\pi f_0)^2 L C_f\right)\right]\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]}{\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]^2 + \left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]^2}$$
$$- \frac{\left[G_{\rm in}\left(1-(2\pi f_0)^2 L C_f\right) - (2\pi f_0)^2 R_{ac} C_f\left(C_{\rm sub}+C_{\rm in}\right)\right]\left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]}{\left[1 + G_{\rm in}R_{ac} - (2\pi f_0)^2 L\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right]^2 + \left[2\pi f_0\left(G_{\rm in}L + R_{ac}\left(C_f + C_{\rm sub} + C_{\rm in}\right)\right)\right]^2}$$
$$+ j2\pi f_0 C_{\rm sub} \tag{2}$$

shown at the bottom of this page. By substituting (9) and (10) into (4), L is expressed as

$$L = \frac{2\left(C_{\text{in}}+C_{\text{sub}}\right)}{G_{\text{in}}^2+(2\pi f_0)^2\left(C_{\text{in}}+C_{\text{sub}}\right)\left(C_{\text{in}}+C_{\text{sub}}+2C_f\right)} \tag{11}$$

While the substrate capacitance C_{sub} can simply be absorbed into C_{in}, C_f slightly reduces the value of L. The ratio of (11) to (7) (with $C_{\text{sub}} = 0$) is

$$\frac{L_{\text{eqn. (11)}}}{L_{\text{eqn. (7)}}} = \frac{G_{\text{in}}^2 + (2\pi f_0)^2 C_{\text{in}}^2}{G_{\text{in}}^2 + (2\pi f_0)^2 (C_{\text{in}})(C_{\text{in}} + 2C_f)} \tag{12}$$

and as long as C_f is relatively small compared to C_{in}, it can be neglected. As will be shown, additional shunt capacitance is sometimes necessary with C_{in} in order to equalize the phase delays between the dividing and combining circuits, further diminishing the effect that C_f has on the value of L. From (3), the new phase delay across the inductor is

$$\varphi_{12} = -2\arctan\left[\frac{2\pi f_0(C_{\text{in}} + C_{\text{sub}})}{G_1}\right]. \tag{13}$$

C_{sub} and $C_f = 0$ (Lossy Inductor): For a lossy inductor with a series equivalent RF resistance R_{ac}, the inductor Q at frequency f_0 is defined as $Q = 2\pi f_0 L/R_{ac}$.

Now (1) and (2) reduce to (14) and (15), shown at the bottom of this page. Using (4) to solve for L

$$L = \frac{(2\pi f_0)C_{\text{in}} - \dfrac{G_{\text{in}}}{Q}}{\pi f\left(G_{\text{in}}^2 + (2\pi f_0)^2 C_{\text{in}}^2\right)\left(1 + \dfrac{1}{Q^2}\right)}. \tag{16}$$

Substituting (16) into (14) and (15)

$$G_2 = \frac{G_{\text{in}}\left(1 - \dfrac{1}{Q^2}\right) + \dfrac{(4\pi f_0)\,C_{\text{in}}}{Q}}{\left(1 + \dfrac{1}{Q^2}\right)} \tag{17}$$

$$B_2 = \frac{\dfrac{2G_{\text{in}}}{Q} - (2\pi f_0)C_{\text{in}}\left(1 - \dfrac{1}{Q^2}\right)}{\left(1 + \dfrac{1}{Q^2}\right)}. \tag{18}$$

As long as the Q is relatively high, $G_2 \approx G_1$ and $B_2 \approx -B_1$. After substituting (17) and (18) into (3), the phase delay across the inductor is

$$\phi_{12} = -\arctan\left[\frac{2\left(2\pi f_0 C_{\text{in}} - \dfrac{G_{\text{in}}}{Q}\right)\left(\dfrac{2\pi f_0 C_{\text{in}}}{Q} + G_{\text{in}}\right)}{\left(G_{\text{in}}^2 - (2\pi f_0)^2 C_{\text{in}}^2\right)\left(1 - \dfrac{1}{Q^2}\right) + \dfrac{8\pi f_0 C_{\text{in}} G_{\text{in}}}{Q}}\right]. \tag{19}$$

As seen from (16) and (19), L and ϕ_{12} are strongly dependent on Q. Moreover, Q itself is a function of L, lending to an iterative solution of (17)–(19).

B. Capacitively Coupled Devices

Referring to the circuit in Fig. 4(b), the equivalent MESFET input admittance at port 1, $Y_1 = G_{\text{in}} - j[1/(2\pi f_0 L_{\text{in}})]$, is transformed $Y_2 = G_2 + jB_2$ at terminal 2 of the capacitor, where it is shown in (20) and (21) at the bottom of the following page where $Q = 1/2\pi f_0 C R_{ac}$. The ratio of RF voltages across the

$$G_2 = \frac{G_{\text{in}}\left(1 - (2\pi f_0)^2 L C_f\right)^2}{\left[1 - (2\pi f_0)^2 L\left(C_f + C_{\text{sub}} + C_{\text{in}}\right)\right]^2 + \left[2\pi f_0\left(G_{\text{in}} L\right)\right]^2} \tag{9}$$

$$B_2 = \frac{2\pi f_0\left[\left(C_{\text{sub}} + C_{\text{in}}\right)\left(1 - (2\pi f_0)^2 L C_f\right)\right]\left[1 - (2\pi f_0)^2 L\left(C_f + C_{\text{sub}} + C_{\text{in}}\right)\right]}{\left[1 - (2\pi f_0)^2 L\left(C_f + C_{\text{sub}} + C_{\text{in}}\right)\right]^2 + \left[2\pi f_0\left(G_{\text{in}} L\right)\right]^2} - \frac{\left[G_{\text{in}}\left(1 - (2\pi f_0)^2 L C_f\right)\right]\left[2\pi f_0\left(G_{\text{in}} L\right)\right]}{\left[1 - (2\pi f_0)^2 L\left(C_f + C_{\text{sub}} + C_{\text{in}}\right)\right]^2 + \left[2\pi f_0\left(G_{\text{in}} L\right)\right]^2} + 2\pi f_0 C_{\text{sub}} \tag{10}$$

$$G_2 = \frac{G_{\text{in}} + \dfrac{1}{Q}(2\pi f_0) L\left[G_{\text{in}}^2 + (2\pi f_0)^2 C_{\text{in}}^2\right]}{\left[1 + 2\pi f_0 L\left(\dfrac{G_{\text{in}}}{Q} - 2\pi f_0 C_{\text{in}}\right)\right]^2 + \left[2\pi f_0 L\left(G_{\text{in}} + \dfrac{2\pi f_0 C_{\text{in}}}{Q}\right)\right]^2} \tag{14}$$

$$B_2 = \frac{2\pi f_0\left[C_{\text{in}} - L\left(G_{\text{in}}^2 + (2\pi f_0)^2 C_{\text{in}}^2\right)\right]}{\left[1 + 2\pi f_0 L\left(\dfrac{G_{\text{in}}}{Q} - 2\pi f_0 C_{\text{in}}\right)\right]^2 + \left[2\pi f_0 L\left(G_{\text{in}} + \dfrac{2\pi f_0 C_{\text{in}}}{Q}\right)\right]^2} \tag{15}$$

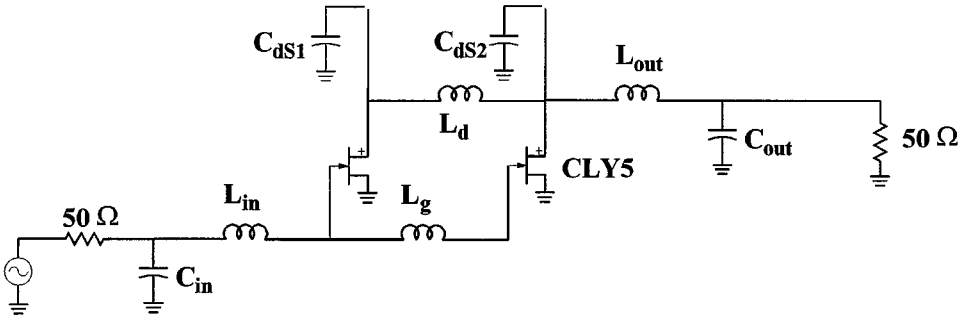


Fig. 5. Power-combining amplifier employing a pair of CLY5 MESFETs.

MIM capacitor is shown in (22), at the bottom of this page. Setting $|V_1| = |V_2|$ and solving for C

$$C = \frac{1}{2}\frac{\left(G_{\text{in}}^2 + \frac{1}{(2\pi f_0 L_{\text{in}})^2}\right)\left(1+\frac{1}{Q^2}\right)}{\frac{1}{L_{\text{in}}} - \frac{2\pi f_0 G_{\text{in}}}{Q}} \tag{23}$$

Equations (20) and (21) reduce to (24) and (25) as follows:

$$G_2 = \frac{G_{\text{in}}\left(1-\frac{1}{Q^2}\right) + \frac{2}{2\pi f_0 L_{\text{in}} Q}}{\left(1+\frac{1}{Q^2}\right)} \tag{24}$$

$$B_2 = \frac{\frac{1}{2\pi f_0 L_{\text{in}}}\left(1-\frac{1}{Q^2}\right) - \frac{2G_{\text{in}}}{Q}}{\left(1+\frac{1}{Q^2}\right)} \tag{25}$$

and the phase delay across the capacitor is shown in (26).

$$\phi_{12} = \arctan\left[\frac{2\left(\frac{1}{2\pi f_0 L_{\text{in}}} - \frac{G_{\text{in}}}{Q}\right)\left(\frac{1}{2\pi f_0 L_{\text{in}} Q} + G_{\text{in}}\right)}{\left(G_{\text{in}}^2 - \frac{1}{(2\pi f_0)^2 L_{\text{in}}^2}\right)\left(1-\frac{1}{Q^2}\right) + \frac{4G_{\text{in}}}{2\pi f_0 L_{\text{in}} Q}}\right]. \tag{26}$$

III. Power-Combining Amplifier Design

The power-combining amplifiers shown in Fig. 2(a) and (b) are implementations of the above approach, where each amplifier consists of separate N-way dividing (input) and N-way combining (output) circuits which are extensions of the two-way divider/combiner designs presented above. Applying (16) to the input circuit in Fig. 2(a), each inductor in the input circuit is expressed as

$$L_{gk} = \frac{(2\pi f)C_{gk} - \frac{G_{gk}}{Q}}{\pi f\left(G_{gk}^2 + (2\pi f)^2 C_{gk}^2\right)\left(\frac{1}{Q^2}+1\right)} \tag{27}$$

where k is an integer from 1 to N, and where G_{gk} and C_{gk} are the effective conductance and capacitance, respectively, looking to the right at the gate junction of device k. It can be shown that

$$G_{gk} = \frac{G_g\left(k+\frac{1}{Q^2}\right) + \frac{4\pi f}{Q}\left(\frac{k-1}{2}C_g + \sum_{i\,\text{even}} C_{gSi}\right)}{1+\frac{1}{Q^2}}, \quad \text{for } k\text{odd} \tag{28}$$

$$G_{gk} = \frac{kG_g + \frac{4\pi f}{Q}\left(\frac{k}{2}C_g + \sum_{i\,\text{odd}} C_{gSi}\right)}{1+\frac{1}{Q^2}}, \quad \text{for } k \text{ even} \tag{29}$$

$$G_2 = \frac{G_{\text{in}} + \frac{1}{2\pi f_0 CQ}\left(G_{\text{in}}^2 + \frac{1}{(2\pi f_0 L_{\text{in}})^2}\right)}{\left[1+\frac{1}{2\pi f_0 C}\left(\frac{G_{\text{in}}}{Q} - \frac{1}{2\pi f_0 L_{\text{in}}}\right)\right]^2 + \left[\frac{1}{2\pi f_0 C}\left(G_{\text{in}} + \frac{1}{2\pi f_0 L_{\text{in}} Q}\right)\right]^2} \tag{20}$$

$$B_2 = \frac{\frac{1}{2\pi f_0 C}\left(G_{\text{in}}^2 + \frac{1}{(2\pi f_0 L_{\text{in}})^2}\right) - \frac{1}{2\pi f_0 L_{\text{in}}}}{\left[1+\frac{1}{2\pi f_0 C}\left(\frac{G_{\text{in}}}{Q} - \frac{1}{2\pi f_0 L_{\text{in}}}\right)\right]^2 + \left[\frac{1}{2\pi f_0 C}\left(G_{\text{in}} + \frac{1}{2\pi f_0 L_{\text{in}} Q}\right)\right]^2} \tag{21}$$

$$\frac{V_1}{V_2} = \frac{1}{1 + \frac{G_{\text{in}}}{2\pi f_0 CQ} - \frac{1}{(2\pi f_0)^2 L_{\text{in}} C} - j\left(\frac{1}{(2\pi f_0)^2 L_{\text{in}} CQ} + \frac{G_{\text{in}}}{2\pi f_0 C}\right)} \tag{22}$$

and (30) and (31), as shown at the bottom of this page.

Similarly for the drain circuit in Fig. 2(a)

$$L_{dk}=\frac{(2\pi f)C_{dk}+\dfrac{G_{dk}}{Q}}{\pi f\left(G_{dk}^2+(2\pi f)^2C_{dk}^2\right)\left(\dfrac{1}{Q^2}+1\right)} \tag{32}$$

$$G_{dk}=\frac{-G_d\left(k+\dfrac{1}{Q^2}\right)+\dfrac{4\pi f}{Q}\left(\dfrac{k-1}{2}C_d+\displaystyle\sum_{i\,\text{even}}C_{dSi}\right)}{1+\dfrac{1}{Q^2}}$$

for k odd (33)

$$G_{dk}=\frac{-kG_d+\dfrac{4\pi f}{Q}\left(\dfrac{k}{2}C_d+\displaystyle\sum_{i\,\text{odd}}C_{dSi}\right)}{1+\dfrac{1}{Q^2}},\quad \text{for } k \text{ even} \tag{34}$$

and (35) and (36), as shown at the bottom of this page. The phase delay between each MESFET in Fig. 2(a) is

$$\phi_{gk}=-\arctan\left[\frac{2\left(2\pi f_0C_{gk}-\dfrac{G_{gk}}{Q}\right)\left(\dfrac{2\pi f_0C_{gk}}{Q}+G_{gk}\right)}{\left(G_{gk}^2-(2\pi f_0C_{gk})^2\right)\left(1-\dfrac{1}{Q^2}\right)+\dfrac{8\pi f_0G_{gk}C_{gk}}{Q}}\right] \tag{37}$$

$$\phi_{dk}=-\arctan\left[\frac{2\left(2\pi f_0C_{dk}+\dfrac{G_{dk}}{Q}\right)\left(\dfrac{2\pi f_0C_{dk}}{Q}-G_{dk}\right)}{\left(G_{dk}^2-(2\pi f_0C_{dk})^2\right)\left(1-\dfrac{1}{Q^2}\right)-\dfrac{8\pi f_0G_{dk}C_{dk}}{Q}}\right] \tag{38}$$

where ϕ_{gk} is the incremental phase delay between each gate and ϕ_{dk} is the incremental phase delay between each drain. To achieve coherent combining in the output circuit, $\phi_{gk}=\phi_{d(N-k)}$ [or $\phi_{g(N-k)}=\phi_{dk}$].

Applying (23) to the power-combining amplifier in Fig. 2(b), each capacitor in the gate circuit is

$$C_{gk}=\frac{1}{2}\frac{\left(G_{gk}^2+\dfrac{1}{(2\pi f_0L_{gk})^2}\right)\left(1+\dfrac{1}{Q^2}\right)}{\left(\dfrac{1}{L_{gk}}-\dfrac{2\pi f_0G_{gk}}{Q}\right)} \tag{39}$$

where

$$G_{gk}=\frac{G_g\left(k+\dfrac{1}{Q^2}\right)+\dfrac{2}{2\pi f_0Q}\left(\dfrac{k-1}{2L_g}+\displaystyle\sum_{i\,\text{even}}\frac{1}{L_{gSi}}\right)}{1+\dfrac{1}{Q^2}},$$

for k odd (40)

$$G_{gk}=\frac{kG_g+\dfrac{2}{2\pi f_0Q}\left(\dfrac{k}{2L_g}+\displaystyle\sum_{i\,\text{odd}}\frac{1}{L_{gSi}}\right)}{1+\dfrac{1}{Q^2}},$$

for k even (41)

$$C_{gk}=\left(\sum_{i\,\text{odd}}C_{gSi}\right)\frac{C_g\left(1+\dfrac{k}{Q^2}\right)-\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{even}}C_{gSi}\right)+\dfrac{(k-1)G_g}{(2\pi f)Q}}{1+\dfrac{1}{Q^2}}\quad \text{for } k \text{ odd} \tag{30}$$

$$C_{gk}=\left(\sum_{i\,\text{even}}C_{gSi}\right)\frac{\dfrac{k}{Q^2}C_g-\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{odd}}C_{gSi}\right)+\dfrac{kG_g}{(2\pi f)Q}}{1+\dfrac{1}{Q^2}}\quad \text{for } k \text{ even} \tag{31}$$

$$C_{dk}=\left(\sum_{i\,\text{odd}}C_{dSi}\right)\frac{C_d\left(1+\dfrac{k}{Q^2}\right)-\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{even}}CB_{dSi}\right)+\dfrac{(k-1)(-G_d)}{(2\pi f)Q}}{1+\dfrac{1}{Q^2}},\quad \text{when } k \text{ is odd} \tag{35}$$

$$C_{dk}=\left(\sum_{i\,\text{even}}C_{dSi}\right)\frac{\dfrac{k}{Q^2}C_d-\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{odd}}C_{dSi}\right)+\dfrac{k(-G_d)}{(2\pi f)Q}}{1+\dfrac{1}{Q^2}},\quad \text{when } k \text{ is even} \tag{36}$$

and (42) and (43), as shown at the bottom of this page. Similarly for the drain circuit in Fig. 2(b)

$$C_{dk} = \frac{1}{2}\frac{\left(G_{dk}^2 + \dfrac{1}{(2\pi f_0 L_{dk})^2}\right)\left(1+\dfrac{1}{Q^2}\right)}{\left(\dfrac{1}{L_{dk}} + \dfrac{2\pi f_0 G_{dk}}{Q}\right)} \tag{44}$$

where

$$G_{dk} = \frac{-G_d\left(k+\dfrac{1}{Q^2}\right) + \dfrac{2}{2\pi f_0 Q}\left(\dfrac{k-1}{2L_d} + \displaystyle\sum_{i\,\text{even}} \frac{1}{L_{dSi}}\right)}{1+\dfrac{1}{Q^2}}, \quad \text{for } k \text{ odd} \tag{45}$$

$$G_{dk} = \frac{-kG_d + \dfrac{2}{2\pi f_0 Q}\left(\dfrac{k}{2L_d} + \displaystyle\sum_{i\,\text{odd}} \frac{1}{L_{dSi}}\right)}{1+\dfrac{1}{Q^2}}, \quad \text{for } k \text{ even} \tag{46}$$

and (47) and (48), shown at the bottom of the next page. The phase delay between each MESFET in Fig. 2(b) is

$$\phi_{gk} = \arctan\frac{2\left(\dfrac{1}{2\pi f_0 L_{gk}} - \dfrac{G_{gk}}{Q}\right)\left(\dfrac{1}{2\pi f_0 L_{gk} Q} + G_{gk}\right)}{\left(G_{gk}^2 - \dfrac{1}{(2\pi f_0 L_{gk})^2}\right)\left(1-\dfrac{1}{Q^2}\right) + \dfrac{4G_{gk}}{2\pi f_0 L_{gk} Q}} \tag{49}$$

$$\phi_{dk} = \arctan\frac{2\left(\dfrac{1}{2\pi f_0 L_{dk}} + \dfrac{G_{dk}}{Q}\right)\left(\dfrac{1}{2\pi f_0 L_{dk} Q} + G_{dk}\right)}{\left(G_{dk}^2 - \dfrac{1}{(2\pi f_0 L_{dk})^2}\right)\left(1-\dfrac{1}{Q^2}\right) - \dfrac{4G_{dk}}{2\pi f_0 L_{dk} Q}} \tag{50}$$

where ϕ_{gk} is the incremental phase delay between each gate and ϕ_{dk} is the incremental phase delay between each drain. Again, achieve coherent combining in the output circuit, $\phi_{gk} = \phi_{d(N-k)}$ [or $\phi_{g(N-k)} = \phi_{dk}$].

IV. Power-Combining Efficiency

By definition, the power-combining efficiency of an N-device amplifier output stage is the ratio of the total output power of divided by N times the output power from a single-device output stage. While under ideal conditions the power-combining efficiency is 100%, this does not take into account reflective losses due to amplitude/phase mismatches within the circuit as well as physical circuit losses.

Reflective losses can be compensated through proper tuning, although physical circuit losses manifested in finite inductor and capacitor Q values cannot be recovered. For a given inductor Q, the input circuit efficiency is

$$\eta_{\text{input}} = \frac{NG_g\left[1+\dfrac{1}{Q^2}\right]}{\left[G_g\left(N+\dfrac{1}{Q^2}\right) + \dfrac{4\pi f}{Q}\left(\dfrac{N-1}{2}C_g + \displaystyle\sum_{i\,\text{even}} C_{gSi}\right)\right]}, \quad \text{for } N \text{ odd} \tag{51}$$

$$\frac{1}{L_{gk}} = \left(\sum_{i\,\text{odd}} \frac{1}{L_{gSi}}\right)\frac{\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{even}} \frac{1}{L_{gSi}}\right) - \dfrac{1}{L_g}\left(1+\dfrac{k}{Q^2}\right) - \dfrac{(k-1)2\pi f_0 G_g}{Q}}{1+\dfrac{1}{Q^2}}, \quad \text{for } k \text{ odd} \tag{42}$$

$$\frac{1}{L_{gk}} = \left(\sum_{i\,\text{even}} \frac{1}{L_{gk}}\right)\frac{\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{odd}} \frac{1}{L_{gSi}}\right) - \dfrac{k}{L_g Q^2} - \dfrac{2k\pi f_0 G_g}{Q}}{1+\dfrac{1}{Q^2}}, \quad \text{for } k \text{ even} \tag{43}$$

$$\frac{1}{L_{dk}} = \left(\sum_{i\,\text{odd}} \frac{1}{L_{dSi}}\right)\frac{\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{even}} \frac{1}{L_{dSi}}\right) - \dfrac{1}{L_d}\left(1+\dfrac{k}{Q^2}\right) - \dfrac{2(k-1)\pi f_0(-G_d)}{Q}}{1+\dfrac{1}{Q^2}}, \quad \text{when } k \text{ is odd} \tag{47}$$

$$\frac{1}{L_{dk}} = \left(\sum_{i\,\text{even}} \frac{1}{L_{dSi}}\right)\frac{\left(1-\dfrac{1}{Q^2}\right)\left(\displaystyle\sum_{i\,\text{odd}} \frac{1}{L_{dSi}}\right) - \dfrac{k}{L_d Q^2} - \dfrac{2k\pi f_0(-G_d)}{Q}}{1+\dfrac{1}{Q^2}}, \quad \text{when } k \text{ is even} \tag{48}$$

TABLE I
ELEMENT VALUES FOR THE TWO—DEVICE AMPLIFIER AS A FUNCTION OF INDUCTORS' Q

Q	L_g	L_d	C_{dS1}	C_{dS2}	L_{in}	C_{in}	L_{out}	C_{out}
INF	2.3nH	2.6nH	6.5pF	6.5pF	3.1nH	8.6pF	3.3nH	7.9pF
50	2.2nH	2.6nH	5.9pF	5.9pF	3.1nH	8.6pF	3.3nH	7.9pF
20	2.1nH	2.5nH	5.1pF	5.1pF	3.1nH	8.7pF	3.3nH	7.8nH
10	1.9nH	2.4nH	3.9pF	3.9pF	3.2nH	8.9pF	3.2nH	7.7nH
5	1.5nH	2.0nH	1.7pF	1.7pF	3.2nH	9.2pF	3.0nH	7.8pF

$$\eta_{\text{input}} = \frac{NG_g\left[1+\frac{1}{Q^2}\right]}{\left[NG_g + \frac{4\pi f}{Q}\left(\frac{N}{2}C_g + \sum_{i\,\text{odd}} C_{gSi}\right)\right]},$$
for N even (52)

which is simply NG_g divided by either (26) or (27), where $k = N$. Similarly, the combining efficiency of the output circuit in Fig. 2(a) is

$$\eta_{\text{output}} = \frac{-G_d\left(N+\frac{1}{Q^2}\right)+\frac{4\pi f}{Q}\left(\frac{N-1}{2}C_d+\sum_{i\,\text{even}} C_{dSi}\right)}{-NG_d\left(1+\frac{1}{Q^2}\right)},$$
for N odd (53)

$$\eta_{\text{output}} = \frac{-NG_d+\frac{4\pi f}{Q}\left(\frac{N}{2}C_d+\sum_{i\,\text{odd}} C_{dSi}\right)}{-NG_d\left(1+\frac{1}{Q^2}\right)},$$
for N even (54)

which is either (31) or (32) (with $k = N$) divided by NG_d. The overall power-combining efficiency of the amplifier in Fig. 2(a) is therefore

$$\eta_{\text{combining}} = \frac{G_g}{-G_d} \cdot \frac{-G_d\left(N+\frac{1}{Q^2}\right)+\frac{4\pi f_0}{Q}\left(\frac{N-1}{2}C_d+\sum_{i\,\text{even}} C_{dSi}\right)}{G_g\left(N+\frac{1}{Q^2}\right)+\frac{4\pi f_0}{Q}\left(\frac{N-1}{2}C_g+\sum_{i\,\text{even}} C_{gSi}\right)},$$
for N odd (55)

$$\eta_{\text{combining}} = \frac{G_g}{-G_d}\,\frac{-NG_d+\frac{2}{Q}\left(\frac{N}{2}B_d+\sum_{i\,\text{odd}} B_{dSi}\right)}{NG_g+\frac{2}{Q}\left(\frac{N}{2}B_g+\sum_{i\,\text{odd}} B_{gSi}\right)},$$
for N even. (56)

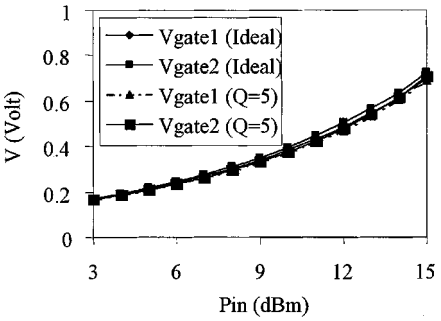


Fig. 6. Inductively coupled two-device amplifier: gate voltage versus pin with ideal inductors, and with inductors having $Q = 5$.

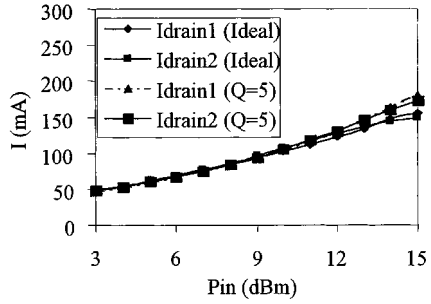


Fig. 7. Inductively coupled two-device amplifier: drain current versus pin with ideal inductors, and with inductors having $Q = 5$.

The input circuit efficiency for the power amplifier in Fig. 2(b) is

$$\eta_{\text{input}} = \frac{NG_g\left[1+\frac{1}{Q^2}\right]}{\left[G_g\left(N+\frac{1}{Q^2}\right)+\frac{2}{2\pi f_0 Q}\left(\frac{N-1}{2L_g}+\sum_{i\,\text{even}}\frac{1}{L_{gSi}}\right)\right]},$$
for N odd (57)

$$\eta_{\text{input}} = \frac{NG_g\left[1+\frac{1}{Q^2}\right]}{\left[NG_g+\frac{2}{2\pi f_0 Q}\left(\frac{N}{2L_g}+\sum_{i\,\text{odd}}\frac{1}{L_{gSi}}\right)\right]},$$
for N even. (58)

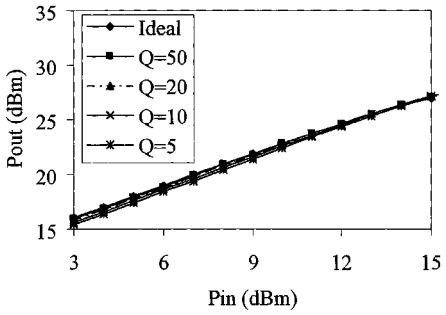


Fig. 8. Inductively coupled two-device amplifier: pout versus pin.

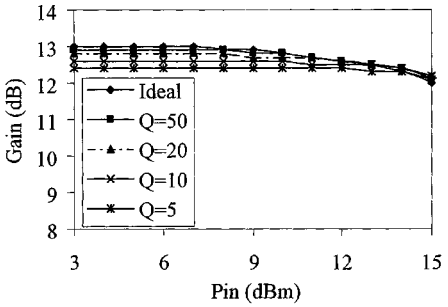


Fig. 9. Inductively coupled two-device amplifier: gain versus pin.

The output circuit efficiency for the power amplifier in Fig. 2(b) is

$$\eta_{\text{output}} = \frac{-G_d\left(N+\frac{1}{Q^2}\right)+\frac{2}{2\pi f_0 Q}\left(\frac{N-1}{2L_d}+\sum_{i\,\text{even}}\frac{1}{L_{dSi}}\right)}{-NG_d\left(1+\frac{1}{Q^2}\right)}$$

for N odd (59)

$$\eta_{\text{output}} = \frac{-NG_d+\frac{2}{2\pi f_0 Q}\left(\frac{N}{2L_d}+\sum_{i\,\text{odd}}\frac{1}{L_{dSi}}\right)}{-NG_d\left(1+\frac{1}{Q^2}\right)}$$

for N even (60)

and the overall power-combining efficiency for the amplifier in Fig. 2(b) is

$$\eta_{\text{combining}} = \frac{G_g}{-G_d} \cdot \frac{-G_d\left(N+\frac{1}{Q^2}\right)+\frac{2}{2\pi f_0 Q}\left(\frac{N-1}{2L_d}+\sum_{i\,\text{even}}\frac{1}{L_{dSi}}\right)}{G_g\left(N+\frac{1}{Q^2}\right)+\frac{2}{2\pi f_0 Q}\left(\frac{N-1}{2L_g}+\sum_{i\,\text{even}}\frac{1}{L_{gSi}}\right)},$$

for N odd (61)

$$\eta_{\text{combining}} = \frac{G_g}{-G_d}\,\frac{-NG_d+\frac{2}{2\pi f_0 Q}\left(\frac{N}{2L_d}+\sum_{i\,\text{odd}}\frac{1}{L_{dSi}}\right)}{NG_g+\frac{2}{2\pi f_0 Q}\left(\frac{N}{2L_g}+\sum_{i\,\text{odd}}\frac{1}{L_{gSi}}\right)},$$

for N even. (62)

V. Power Amplifier Simulations

A nonlinear circuit simulator (HP ADS™) has been used to verify the design procedure for a two-way and a four-way power-combining amplifier with inductively coupled devices. A nonlinear Materka model is used to represent the Siemens CLY5 MESFETs, and the devices are biased at 5 V, 20% I_{DSS} ($V_p = -3.15$, $I_{\text{DSS}} = 880$ mA). Based on matching a single device to a load admittance $Y_L = 60$ mS, the CLY5 model predicts a 1-dB compressed output power ($P_{1\text{ dB}}$) of 27 dBm with a linear gain of 13 dB at 900 MHz, using HP ADS™ software. This corresponds to $Y_g = G_g + j2\pi f_0 C_g = 68.8 + j42.2$ mS and $Y_d = G_d + j2\pi f_0 C_d = 60$ mS. The two-way and the four-way power-combining amplifiers employ inductively coupled devices so that the power-combining efficiency can be observed as a function of series inductor Q values.

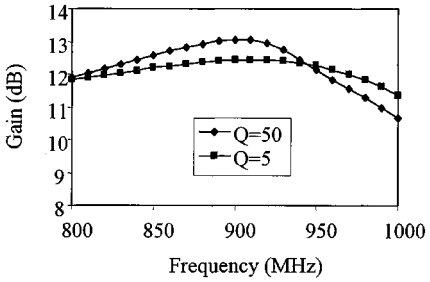


Fig. 10. Comparison of the frequency response for the two-device amplifier with different inductor Q values.

A schematic for the two-device power-combining amplifier is shown in Fig. 5. The amplifier was initially designed assuming infinite Q for the series inductors, then the components were adjusted in order to maintain equal voltages and currents at all the devices as the Q was gradually reduced to five. The final input and output matching circuits to 50 Ω are each designed with a single series L-shunt C matching network. The matching networks use lossless elements, therefore all circuit loss is attributed to the loss within the dividing/combining networks themselves and not the external matching circuits. Table I shows the element values for the two device amplifier for various inductor Q values. Figs. 6 and 7 show the magnitude of the gate voltage and drain current for each device versus input power for ideal inductors and inductors having $Q = 5$. As long as the devices are not driven into saturation, equal voltages and currents are maintained at each device. The input power level is swept to 15 dBm, at which level the gain of the amplifier is compressed by roughly 1 dB. This is where the device impedances begin to change and the power-combining process starts to break down, due mainly to the mismatch that arises between the phase delays in the input circuit and the phase delays in the output circuits. The output currents no longer add coherently, resulting in an overall gain drop. Figs. 8 and 9 illustrate the output power and gain versus input power as a function of inductor loss. When the inductor Q is reduced to 5, the linear gain drops

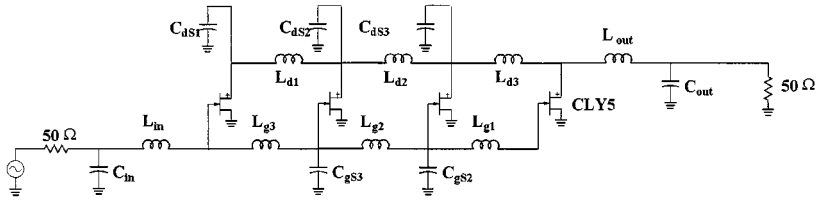
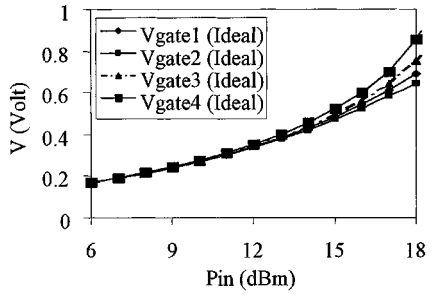


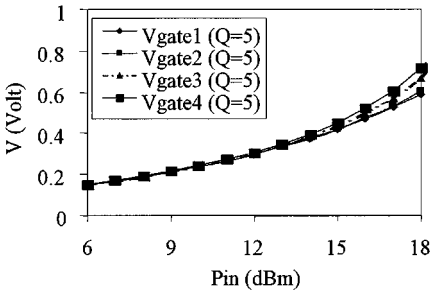
Fig. 11. Power-combining amplifier employing four CLY5 MESFETs.

TABLE II
ELEMENT VALUES FOR THE FOUR—DEVICE AMPLIFIER AS A FUNCTION OF INDUCTORS' Q

Q	L_{g1}	L_{g2}	L_{g3}	L_{d1}	L_{d2}	L_{d3}	C_{gS2}	C_{gS3}	C_{dS1}	C_{dS2}	C_{dS3}	L_{in}	C_{in}	L_{out}	C_{out}
INF	2.3nH	1.0nH	0.7nH	2.5nH	1.2nH	0.9nH	12pF	25pF	6.0pF	16pF	30pF	3.1nH	8.6pF	3.3nH	7.9pF
50	2.2nH	1.1nH	0.7nH	2.6nH	1.3nH	0.9nH	15pF	30pF	6.0pF	19pF	30pF	3.1nH	8.6pF	3.3nH	7.9pF
20	2.1nH	1.0nH	0.7nH	2.6nH	1.3nH	0.9nH	13pF	30pF	5.1pF	16pF	26pF	3.1nH	8.7pF	3.3nH	7.8pF
10	1.9nH	0.9nH	0.6nH	2.6nH	1.3nH	0.9nH	13pF	30pF	4.5pF	14pF	22pF	3.2nH	8.9pF	3.2nH	7.7pF
5	1.5nH	0.7nH	0.5nH	2.5nH	1.0nH	0.8nH	10pF	30pF	3.0pF	9.0pF	14pF	3.2nH	9.2pF	3.0nH	7.8pF

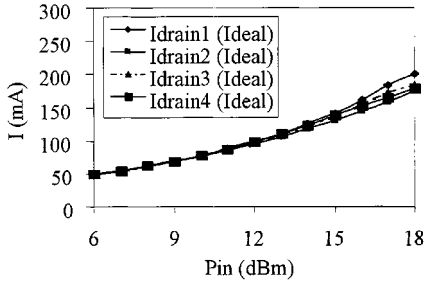


(a)

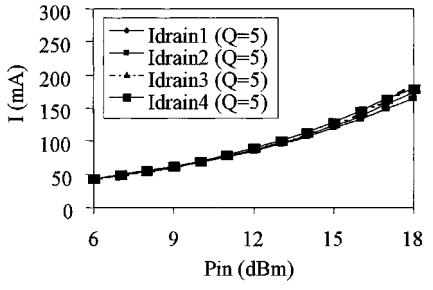


(b)

Fig. 12. Inductively coupled four-device amplifier: Gate voltage versus Pin, for (a) ideal inductors, and (b) for inductors with $Q = 5$.



(a)



(b)

Fig. 13. Inductively coupled four-device amplifier: drain current versus pin (a) ideal and (b) $Q = 5$.

by 0.7 dB, indicating a power-combining efficiency of 85.1%. From (53), the power-combining efficiency of the same amplifier based on the component values shown in Fig. 5 should be 86%. Fig. 10 shows the linear gain of the amplifier versus frequency simulated for $Q = 50$ and for $Q = 5$. The 0.5 dB bandwidth is approximately 90 MHz when $Q = 50$ and 140 MHz when $Q = 5$.

A schematic of the four-device power-combining amplifier is shown in Fig. 11. Again, the amplifier was initially designed assuming infinite Q for the series inductors, then the components were adjusted in order to maintain equal voltages and currents at all the devices as the Q was gradually reduced to five. The final input and output matching circuits to 50 Ω are implemented

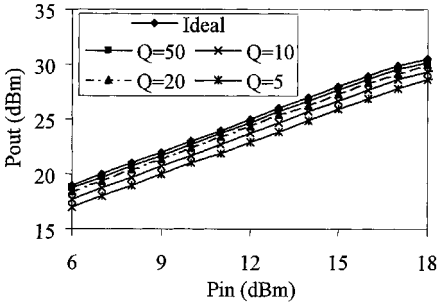


Fig. 14. Inductively coupled four-device amplifier: pout versus pin.

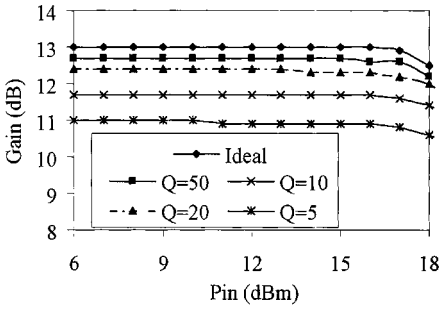


Fig. 15. Inductively coupled four-device amplifier: gain versus pin.

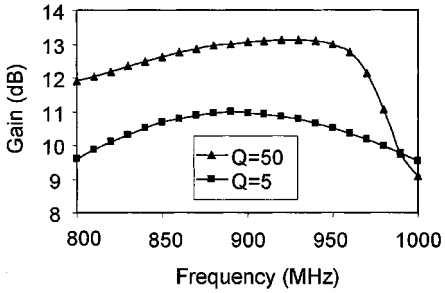


Fig. 16. Comparison of the frequency response for the four-device amplifier with different inductor Q values.

with lossless LC matching networks, so that the circuit loss is attributed only to that within the dividing/combining networks. Table II shows the element values for the four-device amplifier circuit. Figs. 12 and 13 illustrate the magnitude of the gate voltage and drain current for each device versus input power as a function of Q. The input power level is swept to 18 dBm, at which point the amplifier is compressed by approximately 1 dB. Figs. 14 and 15 illustrate the output power and gain versus input power as a function of inductor loss. When $Q = 5$, the linear gain is 10.9 dB, which corresponds to a power combining efficiency of 61.5%. Calculating the power-combining efficiency from (56) with the component values as shown in Fig. 11, the result is off by 0.2%. Fig. 16 shows the linear gain of the amplifier versus frequency simulated for $Q = 50$ and for $Q = 5$.

VI. Conclusion

A technique has been presented for designing multidevice power amplifier output stages in order to avoid thermal problems typically encountered with large periphery devices under linear operation. The proposed dividing/combining circuits have a simple topology as well as being versatile for both compact on-chip and off-chip combining/dividing solutions.

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