Design Rule Development for Microwave Flip-Chip Applications

Daniela Staiculescu, Joy Laskar, *Member, IEEE*, and Emmanouil (Manos) M. Tentzeris, *Member, IEEE*

***Abstract*—This paper presents a novel experimental approach for the analysis of factors to be considered when designing a flip-chip package. It includes the design of an experiment and statistical analysis of the outputs and uses both test-structure measurements and full-wave simulation techniques in the 1–35-GHz frequency range. The most significant factors are found to be, from the most to least important, the length of the area where the device and substrate overlap (referred to as conductor overlap), the bump diameter, and the width of the coplanar-waveguide transmission-line launch. These results are valid for conductor overlaps between 300–500 μm. For a lower value (120 μm), the significance level of the overlap decreases and the bump height also becomes significant. Test-structure measurements in the 120–200-μm overlap range validate this result and demonstrate the decrease in the significance level. The substrate thickness in the 10–25-mil interval is found to be statistically insignificant, therefore, it can be eliminated from further analysis. This approach provides a foundation for development of a set of design rules for RF and microwave flip-chip similar to RF integrated-circuit design rules.**

***Index Terms*—Design rules, flip chip, statistical analysis.**

I. Introduction

ALONG WITH the recent advances in microwave and millimeter-wave system development, the choice of the interconnection solution has become a very important issue since the performance of the system is determined in part by the interconnection geometry. For microwave circuit applications, low-cost, high-density, and short transition interconnect are considered to be the main advantages of the flip-chip technique. Since it gained attention as a potential interconnection solution for microwave and millimeter-wave applications, the flip-chip technology has been electrically, mechanically, and thermally analyzed for understanding its advantages and limitations [1]. The factors that affect the electrical performance of a flip-chip interconnection have been established, and their importance investigated. They include the bump height [2], bump horizontal diameter [3], and conductor overlap [4]. The bump height should be made as short as possible for low parasitic inductance, with a minimum height for avoiding the parasitic modes coupled into the chip-substrate assembly. Conductor overlap and horizontal diameter should be kept as low as possible for reducing parasitic fringing capacitance at the interconnection. Other aspects include the effect of the resin underfill [5] and use of multiple bumps [6]. The next step is to gain a general understanding of all the involved factors, their relative importance, and the interaction between them. The design of experiments (DOE) method presented in this paper allows these goals to be achieved.

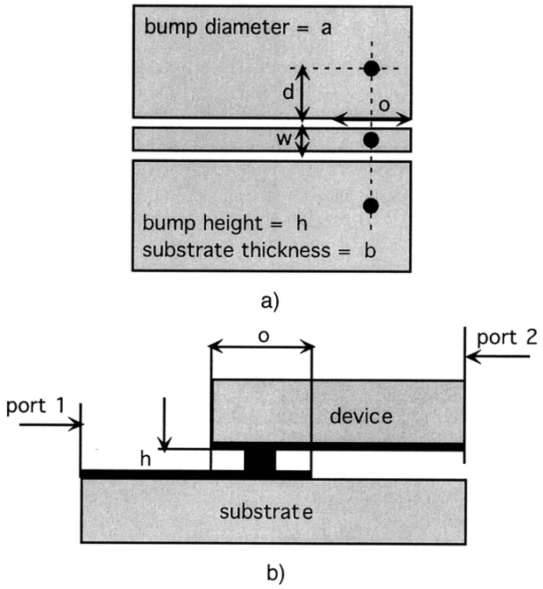

Fig. 1. Analyzed structure. (a) 15 schematic of the bump configuration. (b) Side view of the simulated test structure for the analytical DOE.

II. Experiment

A designed experiment is a series of tests in which a set of input variables is purposely changed so that the experimenter can observe and identify the reasons for changes in the output response. Previous work shows the use of the design of experiments in modeling of microwave/millimeter-wave integrated circuits [7], [8].

This paper represents the first application of the DOE in microwave flip-chip design rule development. The 2^{6-1} fractional factorial [9] analytical experiment is based on full-wave simulations and is validated with a full factorial experiment based on measurements of test structures.

For the simple flip-chip configuration presented in Fig. 1, the input variables to be considered in the experiment are defined as follows:

- o conductor overlap; the bumps are always placed in the center of the overlap area;
- w CPW signal linewidth;
- d distance from ground bump center to the edge of the ground plane;
- a bump diameter;

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TABLE I
VARIABLES FOR THE 2^{6-1} EXPERIMENT

	LEVEL -	LEVEL +
A = substrate thickness	10 mil	25 mil
B = CPW signal width	220 μm	300 μm
C = conductor overlap	300 μm	500 μm
D = distance from edge of ground	50 μm	200 μm
E = bump diameter	50 μm	200 μm
F = bump height	25 μm	100 μm

TABLE II
2^{6-1} EXPERIMENT

Run #	A	B	C	D	E	F=ABCD	|S11|@20GHz
1	-	-	-	-	-	-	-14.1
2	+	-	-	-	-	+	-15.2
3	-	+	-	-	-	+	-14.6
4	+	+	-	-	-	-	-15.1
5	-	-	+	-	-	+	-11.8
6	+	-	+	-	-	-	-10.8
7	-	+	+	-	-	-	-13
8	+	+	+	-	-	+	-12.2
9	-	-	-	+	-	+	-16.5
10	+	-	-	+	-	-	-14.7
11	-	+	-	+	-	-	-15.5
12	+	+	-	+	-	+	-16
13	-	-	+	+	-	-	-12
14	+	-	+	+	-	+	-12.3
15	-	+	+	+	-	+	-11.6
16	+	+	+	+	-	-	-12
17	-	-	-	-	+	+	-12.6
18	+	-	-	-	+	-	-13.8
19	-	+	-	-	+	-	-14.4
20	+	+	-	-	+	+	-13.8
21	-	-	+	-	+	-	-11.5
22	+	-	+	-	+	+	-9.8
23	-	+	+	-	+	+	-10.4
24	+	+	+	-	+	-	-11.4
25	-	-	-	+	+	-	-13.4
26	+	-	-	+	+	+	-13.1
27	-	+	-	+	+	+	-13.2
28	+	+	-	+	+	-	-14.8
29	-	-	+	+	+	+	-9.9
30	+	-	+	+	+	-	-10.9
31	-	+	+	+	+	-	-12.6
32	+	+	+	+	+	+	-11.5

h bump height;
b substrate thickness.

Finite-element method (FEM) simulations are performed to test structures similar to the one presented in Fig. 1(b). The output variable is the magnitude of S_{11} at 20 GHz. The structure length is chosen such as $|S_{11}|$ variation to 35 GHz does not contain any singularity. This makes the variation of the output variable anywhere in the 1–35-GHz frequency range relevant to the experiment. The two levels chosen for each input variable are presented in Table I.

A 2^{6-1} fractional factorial design was chosen for the six variables. The experiment consists of $2^5 = 32$ treatment combinations, presented in Table II. Only one replicate of each treatment combination has been recorded since there is no variability among the simulations. The last column shows the value from the simulated output. Statistical analysis has been performed and an analysis of variance (ANOVA) is presented in Table III.

TABLE III
ANOVA TABLE FOR THE 2^{6-1} EXPERIMENT

Source	Sum of Squares	df	Mean Square	F
A	2.812E-03	1	2.812E-03	.009
B	2.940	1	2.940	9.080
C	69.325	1	69.325	214.091
D	.945	1	.945	2.919
E	12.878	1	12.878	39.769
F	.945	1	.945	2.919
A * B	.228	1	.228	.704
A * C	.525	1	.525	1.622
A * D	2.531E-02	1	2.531E-02	.078
A * E	.113	1	.113	.348
A * F	1.240	1	1.240	3.830
B * C	9.031E-02	1	9.031E-02	.279
B * D	2.531E-02	1	2.531E-02	.078
B * E	.633	1	.633	1.954
B * F	.945	1	.945	2.919
C * D	9.031E-02	1	9.031E-02	.279
C * E	.750	1	.750	2.317
C * F	.475	1	.475	1.468
D * E	.138	1	.138	.426
D * F	.113	1	.113	.348
E * F	4.133	1	4.133	12.763
Error	3.238	10	.324	

The last column in Table III represents the F statistic for all six input variables and all two-factor interactions. Variables with higher F values are more statistically significant. The threshold value for statistical significance has been calculated to be 3.2 for this application [9]. Every variable or interaction with an F value higher than 3.2 is considered to be statistically significant. As shown in the table, the highest value of F has been obtained for the conductor overlap ($F = 214.091$), then bump diameter ($F = 39.769$) and the coplanar waveguide (CPW) signal width ($F = 9.080$). The substrate thickness has a very low F statistic (0.009), therefore, it will be eliminated from further analysis.

An unexpected result is the statistical insignificance of the bump height, which is known as a very important factor in flip-chip design. All the conclusions are valid only for the specified interval for each variable [9]. Looking at the conductor overlap, the defined interval is between 300–500 μm. The large values of the overlap have been imposed by the bump diameter since the smallest overlap has to be larger than the largest diameter. The parasitic capacitance of the interconnection is due to both overlap and bump height. In the case of the large overlap, it can be assumed that all the parasitic capacitive effect is due to the overlap and edge effect, which results in the bump height becoming insignificant. Therefore, further bump-height analysis has been performed for a lower value of the overlap. Three values for the bump height, i.e., 25, 60, and 100 μm, have been combined with a 120-μm overlap. The other variables have been chosen as follows: distance to the edge of the ground

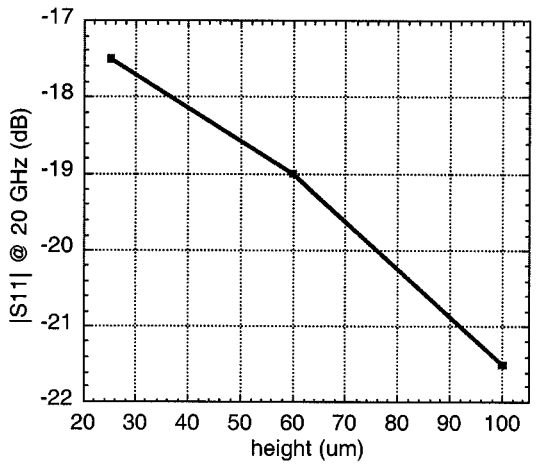

Fig. 2. FEM simulation of variation with bump height.

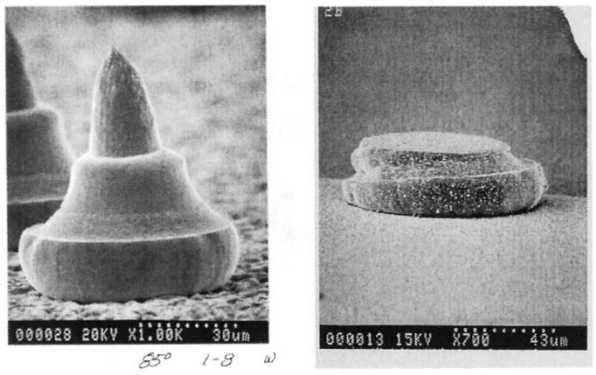

Fig. 3. Stud bump before and after thermosonic attachment.

plane $= 50$ μm, CPW width $= 220$ μm, and bump diameter $= 50$ μm. The result of the simulated $|S_{11}|$ at 20 GHz versus bump height is presented in Fig. 2.

The variation is more than 4 dB, and the comparison with the variation of the output for the entire experiment (Table II) of maximum 6.7 dB shows that the bump height is a significant factor for smaller values of the overlap.

III. Test Structures

The experiment has been verified with test-structure design, fabrication, and measurements. The RF test articles utilized substrates and die made from 99.6% Alumina (Au), 10-mil thick with 50-μm of sputtered Au. The substrates were bumped with 1-mil wire (99% Au 1% Pd), bump size ranged from 66 to 70 μm in diameter and from 43 to 47 μm in height. Dies were attached to the bumped substrates by a process known as "thermosonic flip chip." This process uses a combination of heat, pressure, and ultrasonic energy to form a bond between the bump and metallization on the joining surface. The process parameters used to create these samples were 180 °C base temperature, 50 g per bump force, and a system power setting of 6 on a 40-W ultrasonic power generator. Equipment used was an SEC Model 410 Flip Chip Bonder. Based on samples created during the build of these test articles, the interconnect bump has a standoff height of 20–30 μm and a shear strength of approximately 30 g per bump. Pictures of the stud bump before and after thermosonic attachment are shown in Fig. 3.

The fabrication process used did not allow variation with bump height and bump diameter and the substrate thickness has been eliminated from further analysis because of very low statistical significance. Therefore, only three variables have been included in the new experiment: CPW width (w), conductor

TABLE IV
VARIABLES FOR THE 2^3 EXPERIMENT

Variable	LEVEL -	LEVEL +
d	50 μm	200 μm
o	120 μm	200 μm
w	120 μm	220 μm

TABLE V
2^3 EXPERIMENT

Run #	d	o	w
1	-	-	-
2	+	-	-
3	-	+	-
4	+	+	-
5	-	-	+
6	+	-	+
7	-	+	+
8	+	+	+

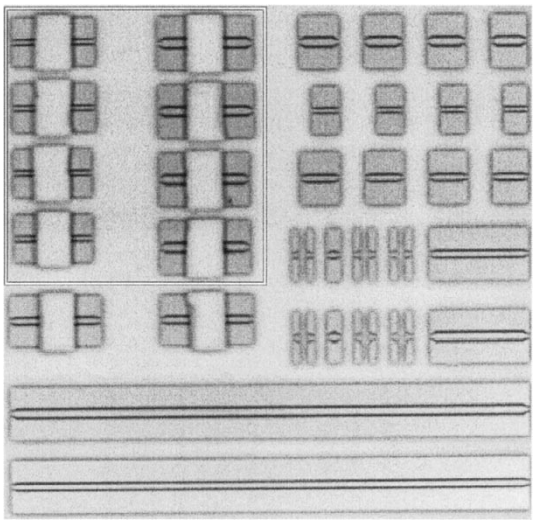

Fig. 4. Test board.

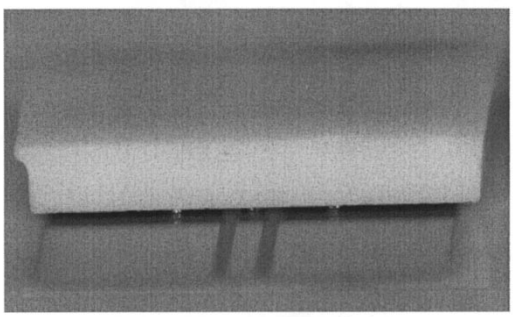

Fig. 5. Side view of attached assembly.

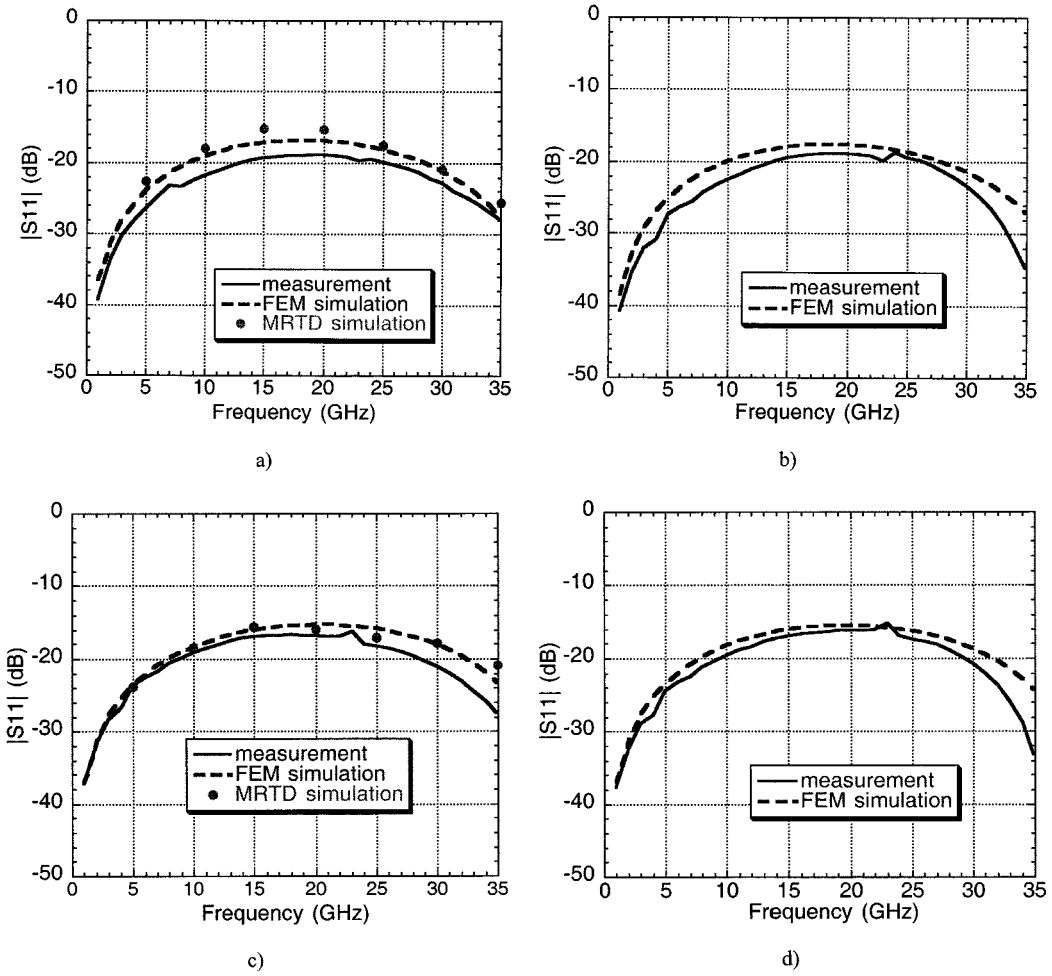

Fig. 6. Measurements versus simulations for the four analyzed test structures; FEM simulation and measurements are validated with MRTD simulation for cases (a) and (c). (a) Number 5 ($d = 50$ μm, $o = 120$ μm). (b) Number 6 ($d = 200$ μm, $o = 120$ μm). (c) Number 7 ($d = 50$ μm, $o = 200$ μm). (d) Number 8 ($d = 200$ μm, $o = 200$ μm).

overlap (o), and distance from the center of the ground bump to the edge of the ground plane (d). This experiment includes three variables and is a full factorial experiment, with $2^3 = 8$ treatment combinations. The "$-$" and "$+$" levels for the three variables mentioned above are shown in Table IV and the eight treatment combinations are presented in Table V. A picture of the test board is shown in Fig. 4. The marked upper left-hand-side corner contains the eight test structures considered in the new design. Fig. 5 contains a side view of a fabricated flip-chip assembly. The measurements are performed using an HP8510B network analyzer with on-wafer ground–signal–ground probes. All structures are measured with 150-μm-wide pitch probes, therefore, the wide CPW transmission lines are tapered. Line-reflect-match (LRM) calibration is used for the narrow lines and custom thru-reflect-line (TRL) calibration for deembedding the effect of the tapering for the wide CPW.

The four results to be considered and analyzed are the ones showing variation with conductor overlap (o) and distance of ground bump from the edge of the ground plane (d). The plots showing the comparison between the measurements and FEM simulation for the four structures are shown in Fig. 6. In the experiment presented in Section II, o has been proven to have very high statistical significance, while d was below the threshold

TABLE VI
ANOVA TABLE FOR THE MEASUREMENT DATA ANALYSIS

Source	Sum of Squares	df	Mean Square	F
d	5.063E-02	1	5.063E-02	.153
o	4.306	1	4.306	13.023
Error	.331	1	.331	
Total	1210.513	4		

value of the F statistic, and therefore, has been declared statistically insignificant. Recording the same output variable, $|S_{11}|$ at 20 GHz for the four measurements and performing statistical analysis, the values for the statistical significance are shown in Table VI. Considering the same threshold value for the F statistic, o is found statistically significant and d insignificant, confirming the conclusion from Section II even if the overlap has been analyzed in a different range. The further bump-height analysis performed in Section II for a conductor overlap in this range (120 μm) showed that the bump height becomes significant for lower values of the overlap. Therefore, the significance level of o for the 120-μm value is expected to be lower than the one for the 300–500-μm range. The two F-values for the low overlap range (120–200 μm) and high overlap range

(300–500 μm) are 13 and 214, respectively, confirming this hypothesis.

The finite-difference time-domain (FDTD) [10] technique has also been used for the full-wave modeling of the flip-chip structures and validation of FEM simulation and measurements for two of the analyzed structures. To enhance the accuracy of the results, Haar wavelets of orders 0 and 1 were added close to the bumps, leading to a Haar-based multiresolution time-domain (MRTD) adaptive scheme [11] with only a minimal computational overhead, while providing locally four times higher resolution. The comparative results of the FEM and MRTD simulations with the measurements of the test structure for 120- and 200-μm overlaps and $d = 50$ μm in the 1–35-GHz frequency range are presented in Fig. 6(a) and (c).

IV. Conclusion

A novel experimental approach for flip-chip design rule development has been presented in this paper. The method is based on properly designing a factorial experiment and statistically analyzing the output. The most significant variables are the conductor overlap, bump diameter, and CPW signal width. The substrate thickness is not significant in the 10–25-mil range and it can be eliminated from the analysis. The bump height is not significant for large overlaps (300–500 μm), but becomes significant for smaller and, therefore, more practical overlap values (120–200 μm). The simulation results have been verified with test-structure measurement and analysis. The method is very flexible and can be extended to a larger number of variables and fabrication process evaluation. These results provide the foundation to develop a regression model and apply it to scale the lumped-element values in an equivalent-circuit model of the bump transition, for developing design rules and technical insight for flip-chip interconnections at RF and microwave frequencies.

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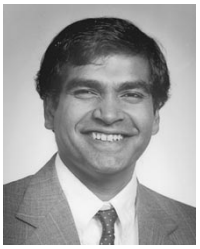

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