Domain Decomposition Approach for Capacitance Computation of Nonorthogonal Interconnect Structures

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***Abstract*—In this paper we apply the domain decomposition approach in conjunction with the finite difference (FD) method to compute efficiently the capacitance matrixes of crossovers and via type of interconnect structures, formed by traces that are nonorthogonal in general. In the past we have applied the FD method, in conjunction with the perfectly matched layer (PML) and the impedance boundary condition for FD mesh truncation, to compute the capacitances of orthogonal interconnect configurations. In this work we extend the above approach to apply to more general geometries, e.g., vias and crossovers with arbitrary angles. The paper presents some representative numerical results and examines the convergence and efficiency issues of the proposed algorithm.**

***Index Terms*—Capacitance, domain decomposition, finite-difference method, interconnects, nonorthogonal configurations.**

I. Introduction

ACCURATE evaluation of the self and mutual capacitances of off-chip and on-chip interconnect configurations is very important in high-speed digital design. In the deep-submicron range, complexities of these interconnect structures lead to computation times that can be prohibitively large. One practical approach to rendering a large problem manageable is to use the "divide and conquer" approach, realized by a domain decomposition scheme. Classical domain decomposition algorithms, such as the Schwartz or Schur complement methods [1], [2], have been developed for discrete approximations in the context of finite element (FE) or finite difference (FD) methods. In principle, the domain decomposition schemes can be applied in conjunction with any number of different solvers for the Poisson's equation with associated boundary conditions to compute the capacitance. The FD method, applied in the various sub-domains, appears to be the preferred choice when used in conjunction with iteration algorithms, because it enables us to compute the values of the electric potential at all of the mesh points in the sub-domain—including the overlap region.

The problems caused by the volume discretization, of the type considered in this paper, do not arise in approaches based on the boundary element method (BEM). As a general rule, the BEMs are numerically more efficient than the other techniques provided the environment of the interconnect is homogeneous, which, however, is seldom ever the case in real-world interconnect structures. A considerable improvement in the computational efficiency of the BEM has been achieved by using the fast multipole method (FMM); however, there is a time penalty to be paid in using this method when the interconnect is embedded in a multilayer dielectric. Though the latter problem is very conveniently and efficiently handled by using the closed-form Green's function, it is not well suited for analyzing nonplanar or conformal dielectrics. If the mesh truncation problem can be addressed in a convenient manner, the FD or FE schemes offer the best avenues for efficient solution of the capacitance problem involving dense interconnect configurations embedded in an inhomogeneous dielectric environment.

General-purpose field solvers based on the FD and FE schemes have been incorporated in many software packages. Methods based on the FD scheme have proven to be flexible and efficient for a wide class of practical configurations. However, the volume discretization employed in these methods often lead to large matrixes. In addition, one must successfully deal with two other issues when using the FD method for the capacitance computation of realistic interconnect structures. The first of these pertains to the truncation of the FD mesh when solving open region problems. In previous works, the authors have shown [3]–[5] how the perfectly matched layer (PML) can be used in conjunction with the impedance boundary condition and mesh refinement scheme for accurate mesh truncation.

In this work we focus on addressing the second difficulty that arises when one attempts to use the FD scheme to analyze interconnects whose geometries do not conform to a single Cartesian system of coordinates. While a simple staircasing approach may be used to handle this problem, the mesh descretization needed to maintain the accuracy of the calculation such that it is 3% or better is typically very fine in the staircase region. This, in turn, often translates to large computation times and CPU requirements for many realistic interconnect structures, especially in the deep-submicron range. To overcome this difficulty, we propose a novel approach based on the domain decomposition scheme and illustrate its application to the problem of capacitance calculation of crossovers formed by traces at different levels that are parallel to the ground plane, but not necessarily parallel to each other. Not only do we avoid the staircasing in this scheme, but we also maintain the number of unknowns at the same level as in case of corresponding parallel or orthogonal

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traces. Furthermore, the proposed scheme is well suited for parallel processing, which also helps reduce the computation time substantially, if utilized.

II. Formulation of the Problem

Interconnect structures of the type considered in this paper are a set of rectangular parallelepiped conductors and dielectric rods embedded in a layered dielectric medium. The capacitance of an N-conductor geometry can be described by an $N \times N$ capacitance matrix $[C]$. The diagonal entries C_{ii} of $[C]$, representing the self-capacitance of conductor i, are positive, while the nondiagonal entries C_{ij}, representing the coupling capacitance between conductors i and j, are negative. To determine the jth row of the capacitance matrix, we need only solve for the surface charges induced on each conductor, after setting the potential of the conductor j to a unity, while grounding the rest of the conductors. Then C_{ij} is numerically equal to the charge on the conductor i; this procedure is repeated N times to compute all rows of the matrix $[C]$.

The potential function $\varphi(\vec{r})(\vec{E}(\vec{r}) = -\nabla\varphi(\vec{r}))$ must satisfy the following:

1) Laplace's equation;
2) Dirichlet's boundary condition at the conductor surfaces;
3) continuity conditions at the dielectric interfaces.

To determine the entries in the nth row of the capacitance matrix, the potential of the nth line is set to 1 V, while the potentials of the other conductors and of the ground planes are set to 0 V. We then solve the following boundary value problem:

$$\begin{aligned}
&\nabla^2\varphi = 0\\
&\varphi(\vec{r}) = 1.0|_{\vec{r}\in S_n}\\
&\varphi(\vec{r}) = 0.0|_{\vec{r}\in S_m} \quad m = 1,\dots N, m \neq n\\
&\varphi(\vec{r}) = 0.0|_{\vec{r}\in S_q}
\end{aligned}$$

where $\{S_n\}_{n=1}^{N}$ are the surfaces of the conducting lines and S_q is the surface of the ground plane.

Let us assume that the edges of conductors and dielectric rods are parallel to the axes of a single Cartesian system of coordinates. Although this assumption is necessary to solve the problem using the conventional FD method, we will show later how one can relax this restriction and use a generalized version of the FD algorithm which is valid for geometries described by multiple systems of Cartesian coordinates.

Following the usual procedure for the FD method, we first set up a mesh to describe the geometry of the interconnect structure. The mesh is devised such that the nodes are placed on the surfaces of the metal traces as well as on the ground planes, and this enables us to generate a single mesh for the entire structure. As a result, the mesh is nonuniform in general, i.e., the x, y, and z dimensions of the cells can be different. After the mesh has been generated, we write the Laplace's equation in the corresponding FD form for all the nodes of the mesh. The equations for the internal nodes at the interfaces between dielectrics can be derived from the integral equation that corresponds to the Gauss's law, as follows:

$$\oint\!\!\!\!\!\!\iint_A \vec{D}(\vec{r})\vec{n}\,dA = \iiint_V \rho\,dv$$

where $\vec{D}$ is the electric flux density, $\vec{n}$ is the outward normal to the surface A, and ρ represents the charges located inside the volume V. If a volume does not contain the metal lines and the conductivity of the dielectrics inside the volume in negligibly small, we can assume that $\rho(\vec{r}) = 0|_{\vec{r}\in V}$.

III. Domain Decomposition Approach

Domain decomposition schemes are based on the concept of dividing the initial computational domain, containing all metal traces, into a system of subdomains. These subdomains are defined, with or without overlap regions, by taking the geometry of the interconnect structure into account in a systematic manner. Since the original boundary value problem is formulated in an unbounded domain, its decomposition into sub-domains does not help us circumvent the problem of mesh truncation. An approach that reduces the influence of the artificial boundary of the subdomain, and yet keeps the number of mesh points realistic for follow-up calculations, was considered in [3]–[5]. To reduce the number of the mesh nodes, i.e., the number of the FD equations, we use the static PMLs and impedance condition on $U = \varphi(\vec{r})$ at the artificial boundary Γ_∞. The material properties of this medium in the static PMLs are described by a diagonal tensor $\hat{\varepsilon}$, with corresponding tensor elements that are less then 1.0. Such tensor elements introduce a "stretching" of the distance between the mesh nodes, and thereby decrease the influence of the artificial boundary on the computed potential values in the interior region. A mixed or impedance condition, viz., $\{\partial/\partial n U(\vec{p}) + \alpha(\vec{p})U(\vec{p})\}|_{\vec{p}\in\Gamma} = 0$, is imposed on the potential function U at the outermost boundary Γ_∞. The coefficient α is a function of the coordinates (see [3] for details) and this function is determined by iterative recalculations. This boundary condition, when used in conjunction with the PMLs, enables us to obtain accurate results with only a single iterative refinement of α. Moreover, the α-technique offers considerable time saving if the interconnect structure is very long.

We consider an N-layer structure, shown in Fig. 1, where the traces in the different layers are either parallel or perpendicular to the local x-coordinate, and may form arbitrary angles with respect to each other. Within each level of this multilayer configuration, the interconnecting lines can be described in local system of Cartesian coordinates. For the sake of simplicity, we assume that these coordinate systems share a common z axis. We divide the computational domain into a multitude of subdomains at each level, with overlap regions in the z direction, and use the PML in conjunction with the α technique [3] to reduce the truncation errors introduced by the artificial boundaries (see Fig. 1).

The first step in the domain decomposition scheme is to define the key subdomains (at least one) to initiate the iteration process. It is essential that the key subdomain contain a metal line (or part of this line) with a nonzero potential. Our next step is to follow an iterative scheme as described below:

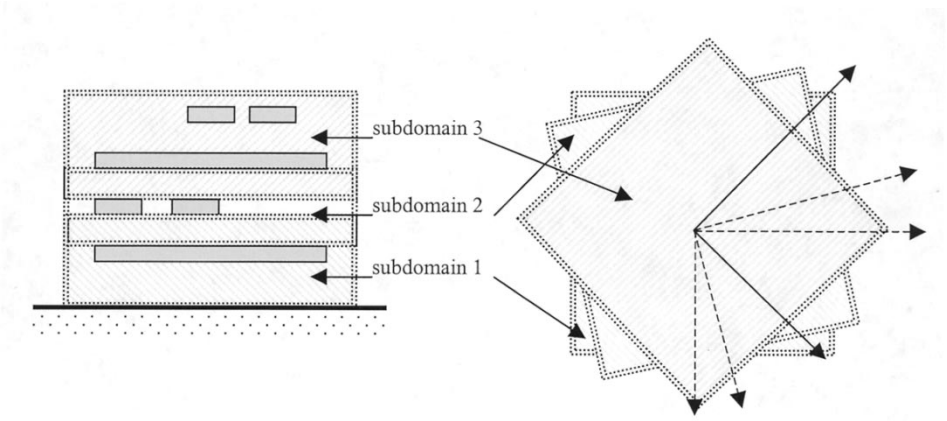

Fig. 1. Division of the computational domain into subdomains in vertical direction and rotation of the subdomains around the axis which is perpendicular to the ground plane.

Step 1) Calculate the electric potential in the key subdomain, say subdomain-1. To eliminate the influence of the artificial boundary, use PML and/or α boundary condition (for details, see [3]).

Step 2) During the first pass, use the results of the first step to compute the potential in the neighboring subdomain in a sequential manner. Use interpolation to obtain the potential values in the neighboring domains to handle the coordinate rotation.

Step 3) Follow a reverse path, once the first pass has been completed, and retrace the steps 1 and 2. Start with the farthest subdomains and progress toward the key subdomain, viz., subdomain-1.

Step 4) Repeat steps 1 and 2, moving forward once again, starting from the key subdomain and going to the most remote ones.

The situation considered above corresponds to the case where we only need in a single Cartesian system of coordinates to set up the FD mesh at each level, as is typically the case. In more general situation, where we may have nonparallel conductors at the same level, the domain decomposition scheme should be modified. Schematically, the iteration algorithm of calculation in two subdomains with nonparallel boundaries is depicted in Fig. 2. The boundaries marked by thick solid lines are artificial ones and require the applications of the PMLs in conjunction with the impedance boundary condition.

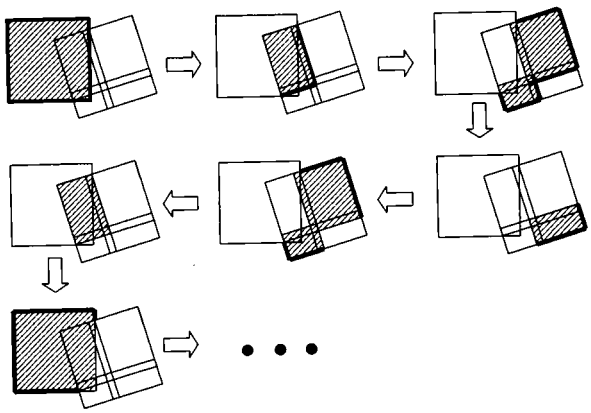

Fig. 2. Iterative scheme for the case of nonorthogonal interconnects located at the same level. The thick solid line indicates the artificial boundaries with PMLs and impedance boundary condition. The shaded area is the subdomain in which the potential is calculated at the iteration step.

IV. Test Cases

In this section, we present the two numerical results for two test cases to illustrate the application of the FD/PML approach and to compare the results of simulation with those derived by other simulation techniques. A variety of geometries have been analyzed by using this method to illustrate its versatility. The first test case we analyze is a simple case of a two-by-two crossover between two ground planes (see Fig. 3). The capacitance matrix of the crossover obtained by the dimension reduction technique and by Ansoft's SPICELINK can be found in [6]. The width, thickness, and length of each line are 1, 1, and 8 μm, respectively. The distances between the parallel lines, between the lines at the lower and upper levels, and from the ground planes to the lines all equal 1 μm. The dielectric constant of the medium is $\varepsilon = 3.9$. It takes 25.8 s on a Pentium PC 500 to compute all of the elements of the capacitance matrix, which is given below.

$$[C] = \begin{bmatrix} 1.486 & -0.387 & -0.185 & -0.185 \\ -0.387 & 1.486 & -0.185 & -0.185 \\ -0.185 & -0.185 & 1.486 & -0.387 \\ -0.185 & -0.185 & -0.387 & 1.486 \end{bmatrix} \text{ fF.}$$

The results obtained by the dimension reduction technique [6] are as follows:

$$[C] = \begin{bmatrix} 1.536 & -0.407 & -0.173 & -0.173 \\ -0.407 & 1.536 & -0.173 & -0.173 \\ -0.173 & -0.173 & 1.536 & -0.407 \\ -0.173 & -0.173 & -0.407 & 1.536 \end{bmatrix} \text{ fF.}$$

The computation time is 87 s with a SUN SPARC 20. The corresponding capacitance matrix, derived by using SPICELINK from Ansoft (as described in [6]) is

$$[C] = \begin{bmatrix} 1.53 & -0.398 & -0.188 & -0.196 \\ -0.398 & 1.52 & -0.187 & -0.195 \\ -0.188 & -0.187 & 1.47 & -0.373 \\ -0.196 & -0.195 & -0.373 & 1.51 \end{bmatrix} \text{ fF}$$

and the computation time is 881 s.

The second test case considered was a crossover formed by two lines, an example of which appears in the Raphael Reference Manual RA 4.1 [7]. The width, thickness, and length of the conductors are 2, 0.5, and 30 μm, respectively. The lower conductor is located at a height of 4 μm above the ground plane and the upper conductor is 12 μm above the ground. The crossover is embedded in a two-layer of dielectric, and the thicknesses of the layers are 4 and 8 μm, while their relative dielectric constants are 4.3 and 3.9, respectively.

The capacitance matrix we obtained for this structure is

$$[C] = \begin{bmatrix} 3.207 & -0.358 \\ -0.373 & 1.5376 \end{bmatrix} \text{ fF.}$$

Since realistic interconnect structures are seldom totally symmetric, we chose to consider the entire computational domain that contained the crossover without invoking any symmetries that would have, if imposed, reduced its size by a factor of four. It took 70 s of CPU time on a Pentium PC 500 to derive this $[C]$ matrix.

For the sake of comparison, we then solved the same problem by using the Raphael software to obtain

$$[C] = \begin{bmatrix} 3.2197 & -0.4183 \\ -0.3872 & 1.6514 \end{bmatrix} \text{ fF.}$$

This latter computation required 80.3 s, even when we took advantage of the symmetry of the structure to reduce the size of the problem domain by a factor of four.

Next, to demonstrate the efficiency of the proposed approach when applied to the case of nonorthogonal crossovers, we divided the entire computational domain into two subdomains with an overlapping region, which ranged from the lower side of the lower line to the upper side of the upper line. We began by using the same FD mesh in the subdomains as we employed for the case of the orthogonal crossover.

To calculate the first row of the capacitance matrix, we set the potential of the lower line (line 1) to 1.0 V and grounded the upper line (line 2). As a first step of the iteration process, we solved the problem in subdomain-1 (see Fig. 4). Next, we went on to solve the problem in the companion domain, i.e., subdomain-2, while utilizing the values of the electric potential at the mesh points in Plane-1. If the crossover is not orthogonal, i.e., if the upper and lower lines form an angle α that is neither 90° or 0°, we rotate the coordinate system of the mesh in subdomain-2 with respect to the corresponding coordinate system of subdomain-1. Consequently, it is necessary to use an interpolation scheme to obtain the values of the potentials at the mesh points on the lower side of the subdomain-2 (Plane-1 in Fig. 4).

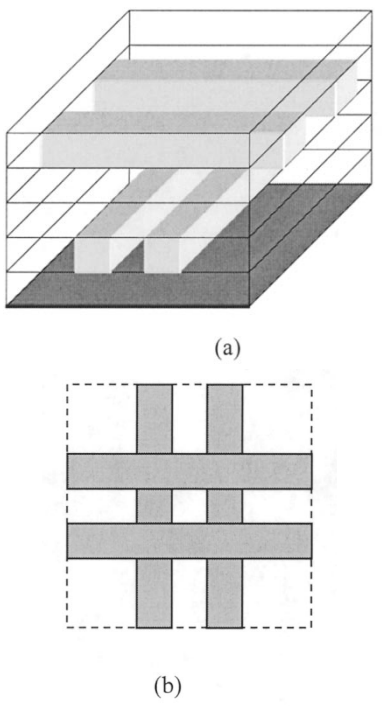

Fig. 3. Test example-1. (a) Two-by-two line crossover above a ground plane. (b) Top view of the crossover.

TABLE I
CAPACITANCE VALUES FOR DIFFERENT CROSSOVER ANGLES α

	α=90°	α=75°	α=60°	α=45°	α=30°	α=15°	α=0°
C_{11}	3.20	3.18	3.237	3.2426	3.26	3.265	3.288
C_{12}	-0.3579	-0.3741	-0.3811	-0.4155	-0.4516	-0.5314	-0.531

At the third step we resolved the problem in subdomain-1, by utilizing the values of the electric potential at the mesh points in Plane-2 and employing the interpolation scheme, if necessary.

The above iteration algorithm, which is based on the domain decomposition scheme, enables us to deal with crossovers with varying angles ranging from the limiting case of an orthogonal crossover (90°) to the other limit of two parallel lines (0°). The results of calculations of the capacitance versus the angle are presented in Table I.

The accuracy realized was better than 1%, and was achieved in just two to three iteration steps for all values of the orientation angle α.

V. ADDITIONAL NUMERICAL EXAMPLES

In this section, we present a few representative problems associated with realistic interconnect structures. For the first example we consider a test structure formed by four lines, whose widths and thicknesses are identical, viz., 0.5 μm and 0.25 μm, respectively (see Fig. 5). The two lines at the lower level are located at a height of 0.75 μm above the ground plane. The length of the straight line (line-1) is 6.0 μm. The distance between bends in the omega-shaped line is 3.0 μm. The lines at the upper level are located at a height of 1.5 μm above the ground plane. The structure is embedded in two dielectric layers. The first of these, just above the ground plane, is 0.75 μm thick, while the

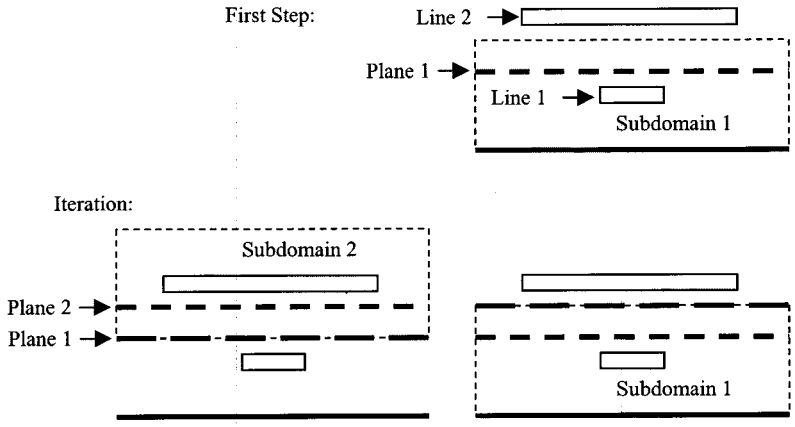

Fig. 4. Test example-2: crossover above the ground plane. Domain decomposition and the iterative scheme for the case of nonorthogonal interconnects.

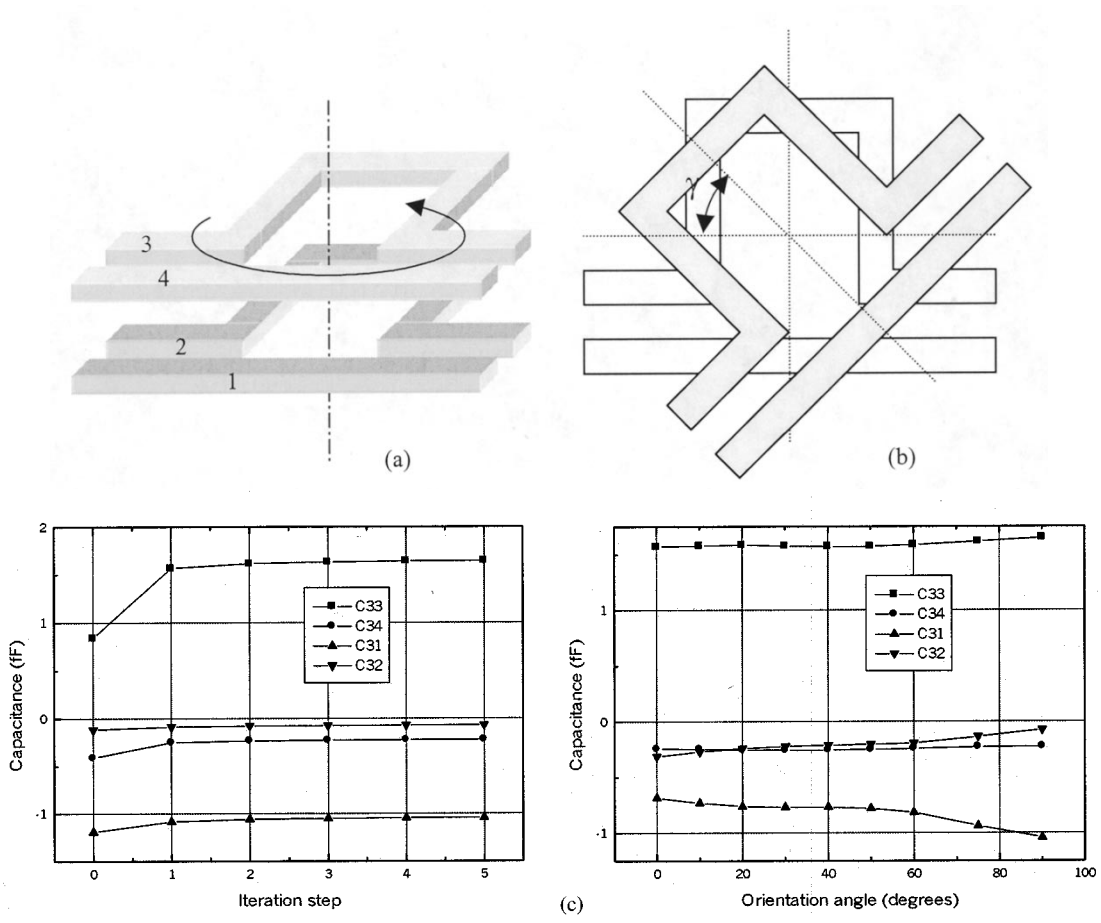

Fig. 5. (a) Four-line structure embedded in two dielectric layers above the ground plane (layers and the ground plane are not shown). (b) Top view of the modified structure. The upper lines are rotated by angle γ about the z axis, which is normal to the ground plane. (c) Capacitances of the four-line structure as functions of the iteration steps and as functions of the orientation angle γ.

second layer on its top is located between the heights of 0.75 μm and 1.75 μm.

If the angle of rotation $\gamma = 90^{\circ}$, and a 1-V potential is applied to line-3 while all the other lines are grounded, the computed capacitance values derived by using a single computational domain turn out to be $C_{33} = 1.6462, C_{34} = -0.2242, C_{32} = -1.0437, C_{31} = -0.0738$. The results of the domain decomposition approach, employing two subdomains with overlapping regions, are presented in Fig. 5(c). Note that the convergence of the iteration procedure is quite rapid.

For the next example, we analyze a via formed by two lines (width 0.5 μm and thickness 0.25 μm) with pads as shown in Fig. 6. The line at the lower level is located at a height of 0.75 μm above the ground plane. The lengths of the straight-line sections are 2.5 μm each. The patch width is 1.5 μm. The line at the upper level is located at a height of 1.5 μm above the ground plane.

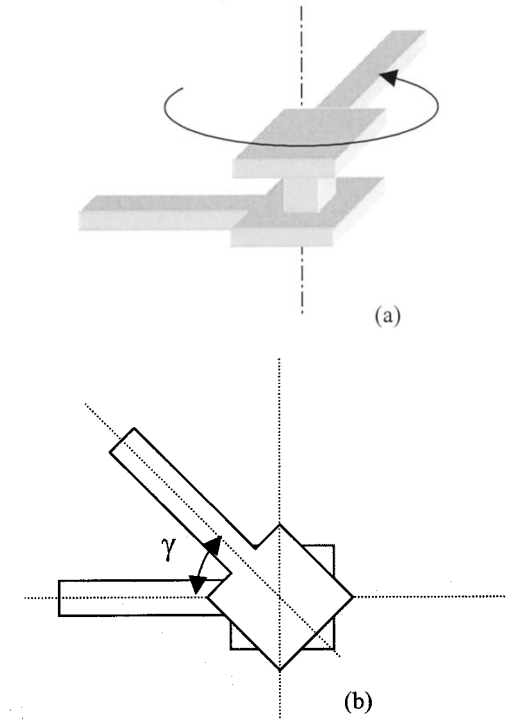

Fig. 6. (a) Via embedded in two dielectric layers above a ground plane (dielectric layers and the ground plane are not shown). (b) Top view of the via structure. The upper line is rotated about the z axis that is normal to the ground plane.

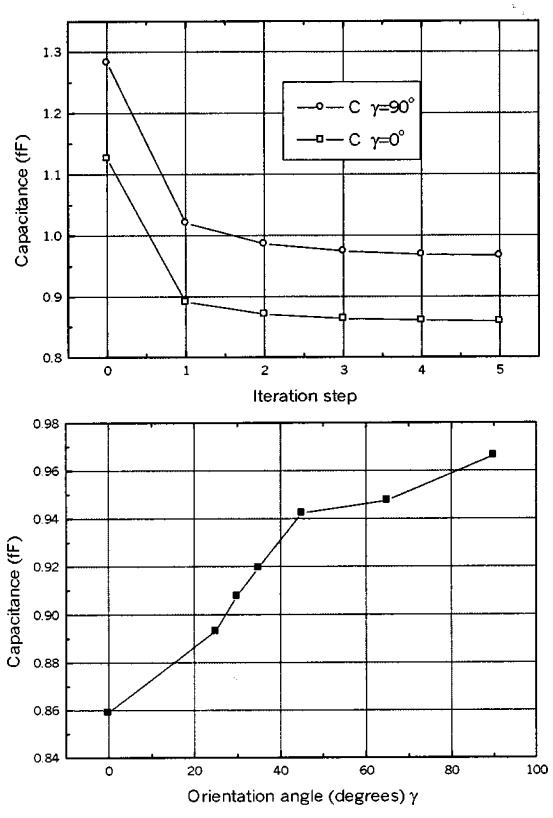

Fig. 7. Capacitance of the via, shown in Fig. 4(a) as a function of the orientation angle γ.

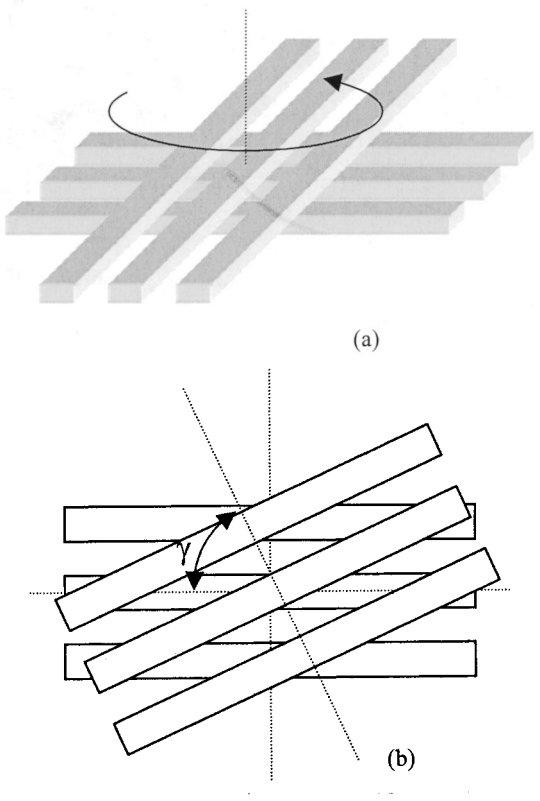

Fig. 8. (a) Three-by-three crossover embedded in two dielectric layers above the ground plane (layers and the ground plane are not depicted). (b) Top view of the crossover. The upper lines are turned around the axis that is normal to the ground plane.

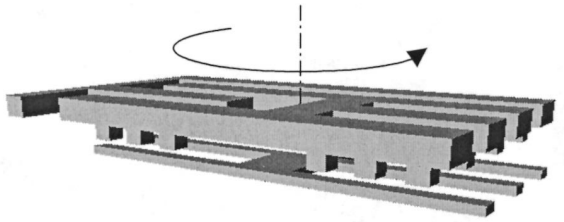

Fig. 9. Three-element interconnect structure. Two upper lines are rotated with respect to the lower traces. The structure is located above the ground plane and embedded in three dielectric layers, with $\varepsilon = 3.9$ (0.0 to 0.5 μm height) $\varepsilon = 5.7$ up a height of 1.4 μm, and $\varepsilon = 4.0$ to a height of 2.5 μm. The ground plane and dielectric layers are not shown in the figure.

The structure is embedded in the same two dielectric layers as those in the previous example.

The results of application of the domain decomposition with two subdomains and an overlapping region between them are presented in Fig. 7. Once again, rapid convergence is realized.

Next, we move on to a 3×3 crossover formed by three-by-three lines (width 0.5 μm and thickness 0.25 μm), as shown in Fig. 8. The lines at the lower level are located at a height of 0.75 μm above the ground plane, and they are both 6.5 μm long. The line at the upper level is located at a height of 1.5 μm above the ground plane. The structure is embedded in the same two dielectric layers as in the previous two examples.

If $\gamma = 25°$, we set the line-1 to a potential of 1 V, and ground all the other lines. For this case, we obtain the following values for the capacitances: $C_{11} = 1.376, C_{12} = -0.306, C_{13} = -0.0048, C_{14} = -0.0424, C_{15} = -0.1884, C_{14} = -0.3242$. The convergence of the iteration algorithm is again found to be swift.

For the last case example, we consider an interconnect structure formed by a set of connected lines (Net-1) at the lower level (0.5 μm above the ground plane) and two nets at the upper level (from 1.1 μm to 2.0 μm). The general view of the structure is shown in Fig. 9. Potential of Net-1 is set to 1 V and all traces from the Net-2 and Net-3 are grounded. For $\gamma = 90°$, we obtain the capacitance values $C_{11} = 3.2683, C_{11} = -0.5746, C_{11} = -1.0585$, and for $\gamma = 0°$, the corresponding values are $C_{11} = 3.0605, C_{11} = -0.5144, C_{11} = -0.7503$. These results agree well with the direct calculations that can be carried out without resorting to domain decomposition.

VI. Conclusion

This paper has presented a novel approach, based on the FD method and the domain decomposition scheme, for modeling interconnect structures that do not conform to a single Cartesian coordinate system, and are usually dealt with by using staircasing. We have shown that the approach can be efficiently applied to the problem of capacitance calculation of crossovers formed by traces at different levels that are parallel to the ground plane, but not necessarily parallel to each other. The proposed approach is efficient because it maintains the number of unknowns at the same level as in the simpler cases of parallel or orthogonal traces.

The domain decomposition scheme, presented herein, not only renders the problem manageable on a computer with a single CPU unit, but is also well suited for parallel processing.

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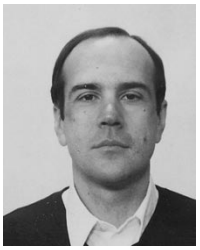

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