An Efficient CAD-Oriented Large-Signal MOSFET Model

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***Abstract*—An efficient computer-aided-design-oriented large-signal microwave model for silicon MOSFETs is presented based on the well-founded small-signal equivalent circuit including self-heating effect and charge conservation condition. The proposed new single continuously differentiable empirical equations for drain current and gate capacitance are simple and quite accurate. The model parameters in the equations are constructed in such a way that they can be easily and straightforwardly extracted from measured data. Temperature effect is predicted by simply adopting the linear temperature-dependent model parameters for threshold voltage, saturation current, capacitance, and series resistances. The presented model is a good compromise between the simplicity of numerical calculations and the accuracy of final results that is desired by circuit designers in nonlinear circuit simulation.**

***Index Terms*—Equivalent circuit, LDMOSFET, MOSFET RF modeling, Serenade, simulation.**

I. Introduction

PERSONAL wireless communication services have been driving intensive activities in silicon MOSFET worldwide for reliable low-cost and high-performance technology [1], [2]. For example, the LDMOS device structures have proven to be highly efficient, high gain, and linear for both high-power and low-voltage microwave and RF applications, including power amplifiers, low-noise amplifiers, mixers, and voltage-controlled oscillators [3]–[5]. In order to develop a low-cost silicon MOSFET for continued and demanded higher speed, higher frequency integrated circuits (ICs), and subsystems within shorter design time, it is necessary to have accurate device models for efficient intensive computer-aided design (CAD) simulation [6]. However, there is lack of such an efficient microwave MOSFET model. Reported popular physical models, such as the BSIM3v3 model, are too complex to be created correctly. Also, most of the models may not be accurate for RF IC simulation due to their derivative discontinuity with respect to the overall bias conditions. Moreover, microwave parasitic effects in silicon MOSFETs are not easy physically predictable. Table-based models, such as the HP Root model, are only accurate for the characterized structures and measurement conditions. An empirical modeling approach is a good compromise between physical and data-based models. It has been proven by excellent success in GaAs monolithic-microwave integrated-circuit (MMIC) development.

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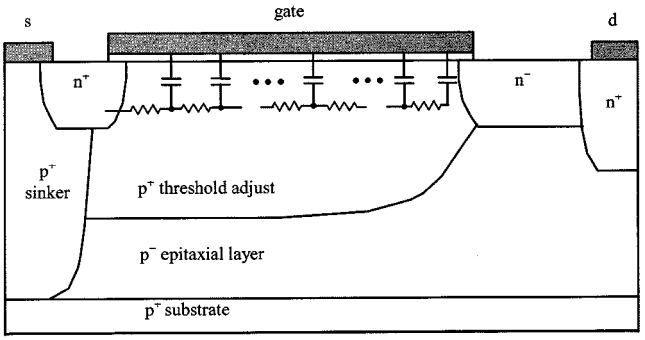

Fig. 1. Schematic representation of the MOSFET distributed channel structure.

In this paper, we report an empirical CAD nonlinear model for microwave silicon MOSFETs. Based on the well-founded small-signal MOSFET equivalent circuit, a new equation-based nonlinear model is empirically constructed from measured characteristics. Although the proposed empirical equations are simple, they describe the nonlinear behavior of the drain–current source and device intrinsic capacitances well. The realization of a single equation to cover wide operation bias conditions from subthreshold to deep inversion warrants the continuous derivatives and charge conservation. These requirements are necessary to predict the accurate third-order intermodulation distortion (IMD) in the harmonic-balanced simulation at large signal levels [7]. Moreover, the equations are constructed in such a way that the model parameter can be easily extracted in a straightforward way or small optimization with only few parameters. In the following sections, this will be described in detail.

II. Equivalent Circuit

In order to accurately describe the nonlinear properties of the large devices, such as LDMOSFETs, it is first necessary to take into account the distributed nature of the device structure along both its channel length and channel width. The distributed effect along the channel length can be modeled as a bias-dependent RC distributed transmission line when the channel charging resistance should be considered, as shown in Fig. 1 [8]. The channel charging resistance $R_{\rm ch}$ is a result of noninstantaneous respond to the changes of the gate–source voltage. In this case, under an assumption of gradual-channel approximation, the equivalent input impedance $Z_{\rm gs}$ seen from gate and source can be written as

$$Z_{\rm gs} = R_{\rm ch}\frac{\coth(\gamma L)}{\gamma L} \tag{1}$$

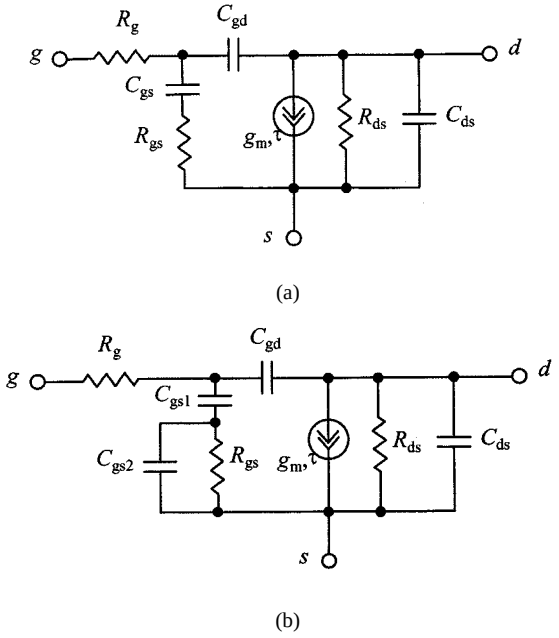

Fig. 2. Intrinsic MOSFET equivalent circuits corresponding to: (a) first- and (b) second-order channel approximation.

where L is the channel length, $\gamma = \sqrt{j\omega R'_{\rm ch} C'_g}$ is the propagation constant, and $R'_{\rm ch} = R_{\rm ch}/L$, $C'_g = C_g/L$, C_g is the total gate capacitance.

The first-order approximation of $Z_{\rm gs}$ obtained from a series expansion of (1) gives

$$Z_{\rm gs} = R_{\rm ch}\frac{\coth(\gamma L)}{\gamma L} \cong \frac{R_{\rm ch}}{\gamma L}\left(\frac{1}{\gamma L}+\frac{\gamma L}{3}\right) = \frac{R_{\rm ch}}{3}+\frac{1}{j\omega C_g}. \tag{2}$$

From (2), it follows that the MOSFET intrinsic gate–source channel circuit can be realized by a simple series circuit with the resistance $R_{\rm gs} = R_{\rm ch}/3$ and the capacitance $C_{\rm gs} = C_g$. Some improvement can be achieved as a result of the second-order approximation of $Z_{\rm gs}$, also derived from a series expansion of (1) as

$$\begin{aligned} Z_{\rm gs} &= R_{\rm ch}\frac{\coth(\gamma L)}{\gamma L} \cong \frac{R_{\rm ch}}{\gamma L}\left[\frac{1}{\gamma L}+\frac{\gamma L}{3}-\frac{(\gamma L)^2}{45}\right] \\ &= \frac{R_{\rm ch}}{3}\left(1-\frac{j\omega C_g R_{\rm ch}}{15}\right)+\frac{1}{j\omega C_g} \\ &\cong \frac{R_{\rm ch}}{3}\Bigg/\left(1+j\omega\frac{R_{\rm ch}}{3}\,\frac{C_g}{5}\right)+\frac{1}{j\omega C_g}. \end{aligned} \tag{3}$$

As a result, the second-order approximation of the channel structure can be realized by a series connection of the capacitance $C_{\rm gs1} = C_g$ and the parallel RC circuit, which consists of the resistance $R_{\rm gs} = R_{\rm ch}/3$ and the capacitance $C_{\rm gs2} = C_g/5$. The intrinsic transistor equivalent circuits corresponding to: 1) first-order approximation and 2) second-order approximation are shown in Fig. 2.

For a high-power MOSFET device, whose channel width is significantly larger than channel length, it is necessary to take into consideration the distributed character of the total gate resistance $R_t = R_{\rm sh}W/L$ across the width W of the device,

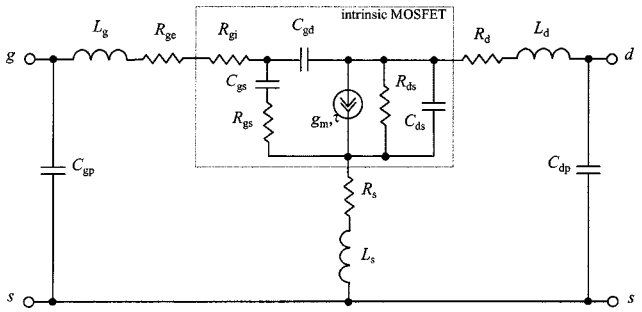

Fig. 3. Nonlinear MOSFET equivalent circuit with extrinsic linear elements.

where $R_{\rm sh}$ is the sheet resistance of the gate material. The silicon MOSFET can be decomposed into n devices, each with a width of W/n and a gate resistance of R_t/n. For $n \to \infty$, it will be viewed as an array of the small transistors distributed along the gate of the device. In a common case, it is necessary to consider a complicated two-dimensional power MOSFET distributed model because of its gate distributed character along both the channel length and channel width. However, due to the short channel size of the MOSFETs, a distributed gate effect along the channel length can be taken into account only in the frequency range close to the transition frequency f_T and higher. For the case when $\omega R_{\rm gs}C_{\rm gs} \ll 1$, the application of a transmission-line theory to analyze this distributed gate model along the channel width shows that all of the transistor Y-parameters should be modified by the term $\tanh(\gamma W)/\gamma W$ [9]. However, a linear series expansion of this term in the form of

$$\frac{\tanh(\gamma W)}{\gamma W} = 1 - j\omega C_g\frac{R_t}{3} \cong \frac{1}{1+j\omega C_g\dfrac{R_t}{3}} \tag{4}$$

leads, in essence, only to an additional use of a series lumped gate resistance $R_t/3$ that does not alter the structure of the transistor equivalent circuit. Consequently, the total gate resistance R_g should be divided in two series resistances as $R_g = R_{\rm ge} + R_{\rm gi}$, where $R_{\rm ge}$ is the extrinsic contact and ohmic gate electrode resistance and $R_{\rm gi} = R_t/3$ is the intrinsic voltage-dependent gate resistance due to the distributed gate structure of a power MOSFET.

In order to accurately describe the device behavior in hybrid or MMIC RF applications, the extrinsic linear elements can be added to the intrinsic nonlinear MOSFET model, as shown in Fig. 3. To evaluate the accuracy and verify the frequency limitation of a proposed small-signal model, three different power MOSFET test cells with the gate length $L = 1.25$ μm and the gatewidth $W = 1.44$ mm have been measured. They are the 28-V LDMOSFET (MOSFET1), 12.5-V LDMOSFET (MOSFET3), and 28-V LDMOSFET with reduced value of R_g (MOSFET2). To extract the small-signal MOSFET equivalent-circuit parameters, on-wafer S-parameter measurements were performed for each cell in the frequency range of 50 MHz up to 10 GHz with a subsequent optimization procedure to minimize the error function in the form of

$$\varepsilon_{ij} = \frac{1}{4}\sum_{i,j=1}^{2}\left(\frac{1}{N}\sum_{n=1}^{N}\frac{|{\rm meas}S_{ijn} - {\rm sim}S_{ijn}|}{{\rm meas}S_{ijn}}\right)\cdot 100\% \tag{5}$$

TABLE I
RELATIVE ERRORS OF S-PARAMETERS FOR MEASURED AND EXTRACTED PARAMETERS

Transistor	ε_{11}, %	ε_{12}, %	ε_{21}, %	ε_{22}, %
MOSFET1	0.76	0.25	1.35	0.73
MOSFET2	1.85	0.81	1.61	1.68
MOSFET3	1.24	2.87	1.26	1.91

where $\mathrm{meas}\, S_{ijn}$ are the measured S-parameter data, $\mathrm{sim}\, S_{ijn}$ are the simulated ones, N is the number of frequencies, and $i, j = 1, 2$. The results of the relative errors of the measured and simulated S-parameters for MOSFET cells are presented in Table I, which indicate a good accuracy for a proposed MOSFET equivalent-circuit model.

Thus, in order to characterize the transistor electrical properties, it is sufficient to use the grounded-source intrinsic Y-parameters, the two-port admittance matrix of which is as follows:

$$Y = \begin{bmatrix} \dfrac{j\omega C_{\rm gs}}{1+j\omega\tau_g} + j\omega C_{\rm gd} & -j\omega C_{\rm gd} \\ \dfrac{g_m \exp(-j\omega\tau)}{1+j\omega\tau_g} - j\omega C_{\rm gd} & G_{\rm ds} + j\omega(C_{\rm ds}+C_{\rm gd}) \end{bmatrix} \tag{6}$$

where $\tau_g = R_{\rm gs}C_{\rm gs}$, τ is the effective channel carrier transit time. As for the intrinsic gate resistance $R_{\rm gi}$, under numerical calculation, it can be considered as an external gate element.

III. MODEL DERIVATION

In many applications, it is necessary to take into consideration the MOSFET operation in the weak-inversion region when the gate-to-source voltage $V_{\rm gs}$ is smaller than the threshold voltage $V_{\rm th}$, e.g., to improve the conversion gain of a mixer or to reduce the IMD of a class-AB power amplifier when an active device is biased at a low-current level around the onset of the strong-inversion region from the weak-inversion region. Also, there is a great influence of input capacitance $C_{\rm gs}$ on the IMD level when the frequency increases in the microwave region [10]. Besides, the use of nonlinear capacitance $C_{\rm gs}$ can improve the simulated dc power consumption [11]. The drain current in the weak-inversion region is mainly dominated by the diffusion component that increases exponentially with the gate voltage [8]. On the other hand, in the strong-inversion saturation region, when the gate-to-source voltage is greater than the threshold voltage, the drain current is proportional to the square of $(V_{\rm gs}-V_{\rm th})$. Unfortunately, in the Berkeley short-channel IGFET model (BSIM) model, which is based on the device physics of a small-geometry MOSFET, the total drain current is modeled as the linear sum of a strong inversion component and a weak inversion component [12]. Such an approach results in a very sharp transition from weak-to-strong inversion regions.

A systematic approach for the extraction of the LDMOSFET model parameters is presented in [13]. The circuit model developed to emulate the nonlinear device current–voltage characteristic consists of a SPICE Level 1 MOSFET model, JFET model, and diode model as the basic elements. Practically the same approach with only the difference of using the special drift resistor to account for the quasi-saturation effect in the drift region is presented in [14]. As a result, a systematic parameter-extraction procedure is based on the knowledge of numerous physical device parameters and measured data. However, even such an approach with careful studying and understanding of the device physics does not allow one to provide a perfect conformity between the modeled and measured data since it was originally based on a simple MOSFET static model usually used to define the nonlinear current source $I_{\rm ds}$ for the devices with long and wide channels. Therefore, the difference between measured and modeled curves $I_{\rm ds}(V_{\rm gs}, V_{\rm ds})$ is more than 10% for both the large and small values of the gate–source voltage $V_{\rm gs}$ [13].

In order to provide a continuous behavior from a weak-inversion region to a strong-inversion region for the drain current and to achieve a compromise between accurate device modeling and ease of circuit analysis, a new simple equation-based empirical MOSFET model is developed.

A. Drain–Current Source

To propose a new empirical nonlinear model that accurately describes the drain–source current–voltage characteristic, two preliminary analytical premises were taken into consideration. First, for a quadratic character of the MOSFET transfer dependence in the strong-inversion region, the transfer drain–current function can be written as follows:

$$I_{\rm ds}(V_{\rm gs}) = A\Big\{\ln\left[1+\exp(B(V_{\rm gs}-V_{\rm th}))\right]\Big\}^2 \tag{7}$$

where A and B are the approximation parameters. As follows from (7), the drain current is effectively proportional to the square of $(V_{\rm gs}-V_{\rm th})$ when $V_{\rm gs}$ is larger than $V_{\rm th}$ and exponentially decreases with the gate voltage when $V_{\rm gs}$ is smaller than $V_{\rm th}$. The similar approximation, which is used in the Enz–Krummenacher–Vittoz (EKV) MOST model, has been successfully applied to low-voltage and low-current analog circuit design and simulation [15]. The approximation parameters A and B are defined from the following conditions:

$$I_{\rm ds}|_{V_{\rm gs}=V_{\rm th}} = I_{\rm th} \quad \left.\frac{\partial I_{\rm ds}}{\partial V_{\rm gs}}\right|_{V_{\rm gs}=V_{\rm th}} = S_{\rm th} \tag{8}$$

where $I_{\rm th}$ is the threshold drain current, as shown in Fig. 4(a), and $S_{\rm th}$ is a slope of the transfer current–voltage characteristic in the threshold point. Then

$$A = \frac{I_{\rm th}}{(\ln 2)^2} \quad B = \frac{S_{\rm th}}{I_{\rm th}}\ln 2. \tag{9}$$

Consequently, to define the transfer characteristic it is quite enough to be limited to two physical parameters $I_{\rm th}$ and $S_{\rm th}$, which are easily defined from the device measurements.

To link the linear and saturation regions by continuous analytical dependence, the following function to represent the current–voltage characteristic of the HEMT devices was used [7]:

$$I_{\rm ds}(V_{\rm gs}, V_{\rm ds}) = (I_{\rm max}^{-1} + I_{\rm dso}^{-1})^{-1} \tag{10}$$

where $I_{\rm dso}$ is an exponential function of $V_{\rm gs}$ and $V_{\rm ds}$, and $I_{\rm max}$ is maximum channel current expressed by

$$I_{\rm max}(V_{\rm ds}) = I_{\rm pk}(1+\lambda V_{\rm ds})\tanh(\alpha V_{\rm ds}). \tag{11}$$

$I_{\rm pk}$ is the drain current, which is corresponded to maximum slope of the $I_{\rm ds}$–$V_{\rm gs}$ curve, as shown in Fig. 4(b). Parameter α is

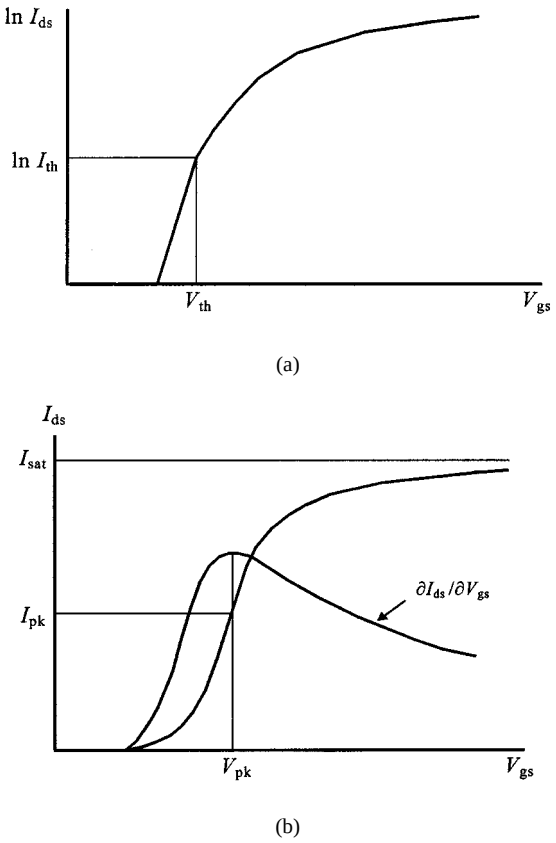

Fig. 4. Drain current $I_{\rm ds}$ versus gate–source voltage $V_{\rm gs}$.

the saturation voltage parameter, which has an effect on a slope of the $I_{\rm ds}$–$V_{\rm ds}$ curves in the linear region, whereas parameter λ determines a slope of the same curves in the saturation region. The use of a hyperbolic tangent function has been successfully applied to approximate with good accuracy the entire $I_{\rm ds}$–$V_{\rm ds}$ curves of the JFET, MESFET, and HEMT drain–current sources [16]–[18].

Then, in view of the quite sloping character of $I_{\rm ds}$–$V_{\rm ds}$ curves, and by taking into account two analytic preliminary premises presented by (7) and (10), the entire current–voltage characteristic of a MOSFET can be described as follows:

$$I_{\rm ds}(V_{\rm gs},V_{\rm ds}) = I_o \Bigg/ \left[1+\left(\frac{I_o}{I_{\max}}\right)^n\right]^{1/n} \tag{12}$$

where

$$I_o = \frac{I_{\rm th}}{(\ln 2)^2(1-\beta V_{\rm gs})} \cdot \left\{\ln\left[1+\exp\left(\frac{S_{\rm th}\ln 2}{I_{\rm th}}\,(V_{\rm gs}-V_{\rm th})\right)\right]\right\}^2$$

$$I_{\max} = I_{\rm sat}(1+\lambda V_{\rm ds})\tanh(\alpha V_{\rm ds})$$

$I_{\rm sat}$ is the saturated drain current, as shown in Fig. 4(b), $V_{\rm th} = V_{\rm tho} - \sigma V_{\rm ds}$, β is the fitting parameter, which determines a slope of $I_{\rm ds}$–$V_{\rm gs}$ curves under the large values of $V_{\rm gs}$, and σ is the parameter, which empirically expresses the dependence of the threshold voltage on $V_{\rm ds}$. Better accuracy can be achieved by using $I_{\rm sat}$ in the expression for $I_{\max}$ in (11) instead of $I_{\rm pk}$.

B. Capacitances

Attempting to calculate the gate–source capacitance $C_{\rm gs}$ or the gate–drain capacitance $C_{\rm gd}$ from the charges corresponding only to the accurate strong-inversion model results in a very complicated expression [8]. Therefore, in some cases of MOSFET modeling, the capacitances $C_{\rm gs}$ and $C_{\rm gd}$ can be modeled as the fixed capacitances measured at the quiescent bias voltage and p-n junction diode capacitance model can be applied to the capacitance $C_{\rm ds}$ [13]. In [14], only the drain–source capacitance $C_{\rm ds}$ and gate–drain capacitance $C_{\rm gd}$ are considered as the bias-dependent junction capacitances. With an increase in the bias voltage, a depletion region is formed under the oxide in the lightly doped drain region. Therefore, the capacitance $C_{\rm gd}$ can be considered as a junction capacitance, which strongly depends on the drain–source bias voltage $V_{\rm ds}$. According to the accurate charge model calculations in [8], $C_{\rm gd}$ has a strong dependence on $V_{\rm gs}$ only in the moderate-inversion region when $V_{\rm gs}-V_{\rm th} < 1$ V. For low-voltage MOSFET devices, the dependence of $C_{\rm gd}(V_{\rm gs},V_{\rm ds})$ can be quite accurately approximated by trigonometric hyperbolic functions [19], [20]. However, for high-voltage LDMOSFET devices, since the dependence of $C_{\rm gd}$ on $V_{\rm gs}$ is quite small, it seems sufficient to be limited to the dependence of $V_{\rm ds}$ only. As to the capacitance $C_{\rm ds}$, it is varied due to the change in the depletion region, which is mainly determined by the value of $V_{\rm ds}$.

To describe the behavior of the total gate–source capacitance $C_{\rm gs}$, it is necessary to separately consider an appropriate behavior of the intrinsic gate–source capacitance $C_{\rm gsi}$, including both the gate–source and source–substrate charge fluctuations, and the gate–substrate capacitance $C_{\rm gbi}$, the gate–source voltage dependence of which is essentially different [8]. The intrinsic gate–substrate capacitance $C_{\rm gbi}$ is constant in the accumulation region where it is equal to the total intrinsic oxide capacitance $C_{\rm ox}$, slightly decreases in the weak-inversion region, significantly reduces in the moderate-inversion region, and becomes practically constant in the strong-inversion or saturation regions. On the contrary, the intrinsic gate–source capacitance $C_{\rm gsi}$ rapidly grows in the moderate inversion region and becomes equal to $2C_{\rm ox}/3$ in the saturation region. The dependence of the total gate–source capacitance $C_{\rm gs}$ as a sum of its components $C_{\rm gsi}$ and $C_{\rm gbi}$ on $V_{\rm gs}$ is presented in Fig. 5.

In this case, it is convenient to use a hyperbolic tangent function for each of two parts of the dependence $C_{\rm gs}$ ($V_{\rm gs}$) where the gate–source capacitance as well as the MOS junction capacitance can be approximated by the following function:

$$C_{\rm gs} = C_{\rm gs\,min} + C_s\left\{1+\tanh\left[\frac{S}{C_s}\,(V_{\rm gs}-V_s)\right]\right\} \tag{13}$$

where $C_s = (C_{\rm gs\,max} - C_{\rm gs\,min})/2$, $C_{\rm gs\,max}$ is the maximum gate–source capacitance, $C_{\rm gs\,min}$ is the minimum gate–source capacitance, and $S = (S_1, S_2)$ is the slope of $C_{\rm gs}$ ($V_{\rm gs}$) at each bend point $V_{\rm gs} = V_s = (V_{s1}, V_{s2})$, as shown in Fig. 5

$$S_1 = \left.\frac{\partial C_{\rm gs}}{\partial V_{\rm gs}}\right|_{V_{\rm gs}=V_{s1}} \qquad S_2 = \left.\frac{\partial C_{\rm gs}}{\partial V_{\rm gs}}\right|_{V_{\rm gs}=V_{s2}}.$$

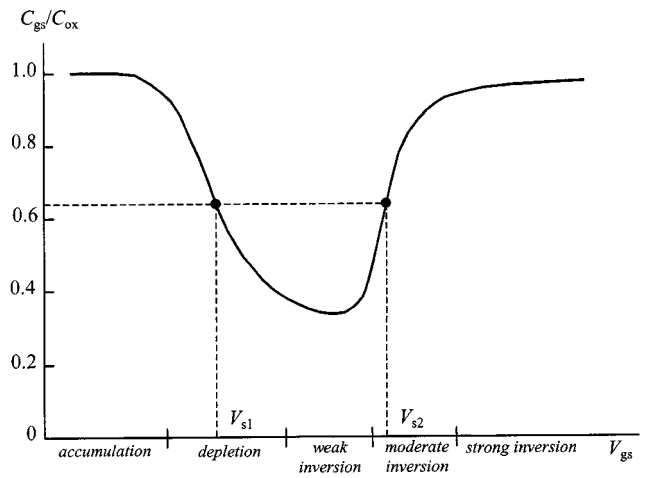

Fig. 5. Gate–source capacitance $C_{\rm gs}$ versus gate–source voltage $V_{\rm gs}$.

Then, the total gate–source capacitance $C_{\rm gs}$ as a function of $V_{\rm gs}$ can be described by

$$C_{\rm gs} = C_{\rm gs\,max} - C_{\rm gso}\left\{1+\tanh\left[\frac{S_1}{C_s}\,(V_{\rm gs}-V_{s1})\right]\right\} \times\left\{1+\tanh\left[\frac{S_2}{C_s}\,(V_{\rm gs}-V_{s2})\right]\right\} \quad (14)$$

where $C_{\rm gs\,max}=C_{\rm ox}$, $C_{\rm gso}$ is the model fitting parameter.

On the other hand, for high-voltage LDMOSFET devices, the dependencies of gate–drain capacitance $C_{\rm gd}$ and drain–source capacitance $C_{\rm ds}$ on $V_{\rm ds}$ can be accurately evaluated by means of the junction diode capacitance model as follows:

$$C_{\rm gd(ds)} = C_{\rm gdo(dso)}\left(\frac{\varphi+E_{\rm ds}}{\varphi+V_{\rm ds}}\right)^m \quad (15)$$

where m (m_1 for $C_{\rm gd}$ or m_2 for $C_{\rm ds}$) is the junction sensitivity, φ is the contact potential, a value of which depends on a doping profile ($m=1/3$ for the linearly graded junction, $m=1/2$ for the abrupt junction, $m>1/2$ for the hyperabrupt junction), and $C_{\rm gdo}$ and $C_{\rm dso}$ are the junction capacitances when $V_{\rm ds}=E_{\rm ds}$. For practical junction profiles, which are neither exactly abrupt nor exactly linearly graded, one often chooses the parameters m and φ so as to obtain the best matching between the theoretical model and measurements.

C. Charge Conservation

In order to correctly describe both small- and large-signal device models, it is necessary to satisfy a charge conservation condition. For a three-terminal MOSFET device, the matrix equation for a small-signal charging circuit in the frequency-domain representation can be given by

$$\begin{bmatrix} I_g \\ I_d \\ I_s \end{bmatrix} = j\omega \begin{bmatrix} C_{\rm gg} & -C_{\rm gd} & -C_{\rm gs} \\ -C_{\rm dg} & C_{\rm dd} & -C_{\rm ds} \\ -C_{\rm sg} & -C_{\rm sd} & C_{ss} \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_d \\ V_s \end{bmatrix} \quad (16)$$

where I_g, I_d, and I_s are the terminal current amplitudes, V_g, V_d, and V_s are the terminal voltage amplitudes, and the capacitance between any two device terminals (k,l) is described as $C_{kl}=\partial Q_k/\partial V_l$ [8]. To transform a three-terminal device into a two-port network with a common source terminal, the current and voltage terminal conditions of $I_g=I_{\rm gs}$, $I_d=I_{\rm ds}$, $I_s=-(I_{\rm gs}+I_{\rm ds})$, $V_g-V_s=V_{\rm gs}$, and $V_d-V_s=V_{\rm ds}$ should be taken into account. Besides, for three-terminal devices, the following relations between terminal capacitances are performed:

$$\begin{aligned} C_{\rm gg} &= C_{\rm gd}+C_{\rm gs}=C_{\rm dg}+C_{\rm sg} \\ C_{\rm dd} &= C_{\rm dg}+C_{\rm ds}=C_{\rm gd}+C_{\rm sd} \\ C_{ss} &= C_{\rm sg}+C_{\rm sd}=C_{\rm gs}+C_{\rm ds}. \end{aligned} \quad (17)$$

Then, the admittance Y_c-matrix for such a capacitive two-port network can be easily written as

$$Y_c = \begin{bmatrix} j\omega(C_{\rm gs}+C_{\rm gd}) & -j\omega C_{\rm gd} \\ -j\omega(C_{\rm gd}+C_m) & j\omega(C_{\rm ds}+C_m+C_{\rm gd}) \end{bmatrix} \quad (18)$$

where $C_m=C_{\rm dg}-C_{\rm gd}$ is the transcapacitance [8].

If it is taken into account that, for power MOSFET devices, the transcapacitance C_m is substantially less than $C_{\rm gs}$, it can be translated to an additional delay time τ_c in a frequency range up to f_T by combining with the transconductance g_m according to

$$\begin{aligned} g_m - j\omega C_m &= g_m\sqrt{1+\left(\frac{\omega}{\omega_T}\,\frac{C_m}{C_{\rm gs}}\right)^2} \\ &\quad\times\exp\left[-j\tan^{-1}\left(\frac{\omega}{\omega_T}\,\frac{C_m}{C_{\rm gs}}\right)\right] \\ &\cong g_m\exp(-j\omega\tau_c) \end{aligned} \quad (19)$$

where $\tau_c = C_m/\omega_T C_{\rm gs}$. As a result, to satisfy a charge conservation condition, the total delay time τ presented in the MOSFET equivalent circuit in Fig. 3 should contain both delay time due to the ideal transit time and delay time due to the transcapacitance. Also, the transcapacitance C_m can be easily added to the drain–source capacitance $C_{\rm ds}$ under a parameter-extraction procedure.

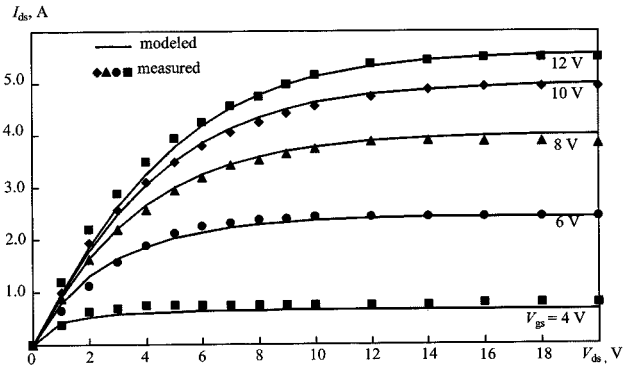

Fig. 6. Measured and modeled $I_{\rm ds}$–$V_{\rm ds}$ curves of a 28-V LDMOSFET.

D. Gate–Source Resistance

The gate–source resistance $R_{\rm gs}$, which is determined by the effect of the channel inertia in responding to rapid changes of the time varying gate–source voltage, varies in such a manner that the charging time τ_g remains approximately constant [21]. Thus, the increase of $R_{\rm gs}$ in the velocity saturation region when the channel conductivity decreases is partially compensated by the decrease of $C_{\rm gs}$ due to nonuniform channel charge distribution [22]. The effect of $R_{\rm gs}$ becomes significant at higher frequencies close to the transition frequency f_T of the MOSFET and cannot practically be taken into consideration for the RF

TABLE II
SIMULATED I–V MODEL PARAMETERS OF A HIGH-POWER LDMOSFET

Parameters	α, 1/V	β, 1/V	λ, 1/V	V_{th}, V	I_{th}, A	S_{th}, A/V	I_{sat}, A	n	σ
Values	0.15	0	0.0005	2.7	0.115	0.2	6.8	1.0	0

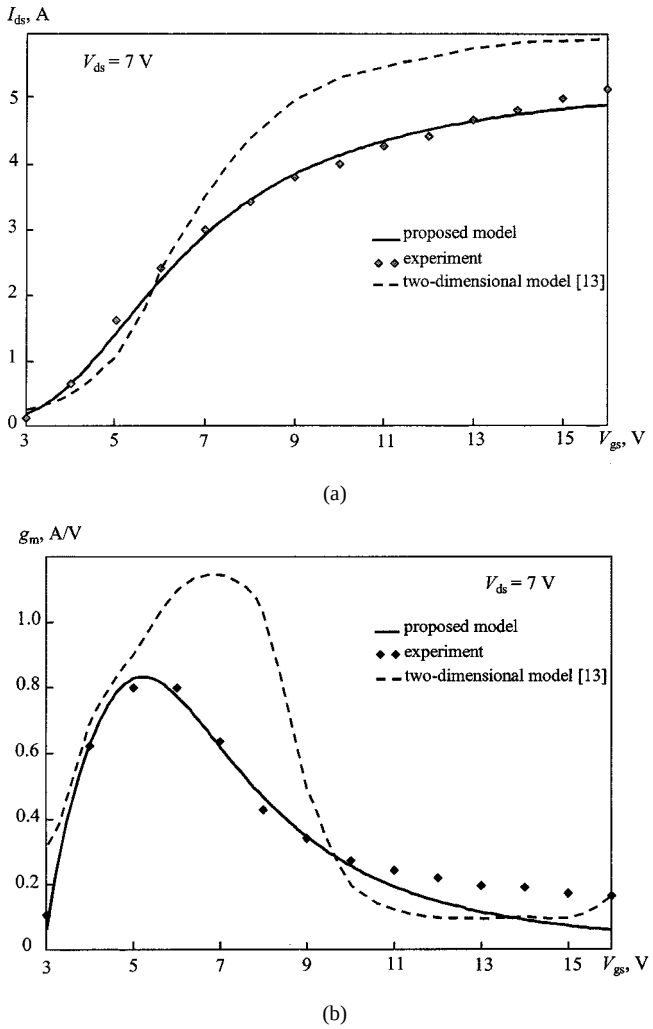

Fig. 7. Measured and modeled: (a) $I_{\rm ds}$–$V_{\rm gs}$ curves and (b) $g_m(V_{\rm gs})$ dependencies of a high-power LDMOSFET.

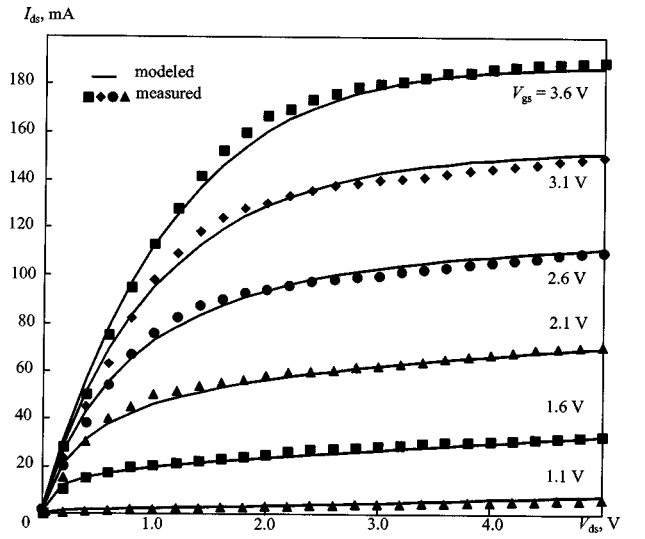

Fig. 8. Measured and modeled $I_{\rm ds}$–$V_{\rm ds}$ curves of a low-voltage MOSFET.

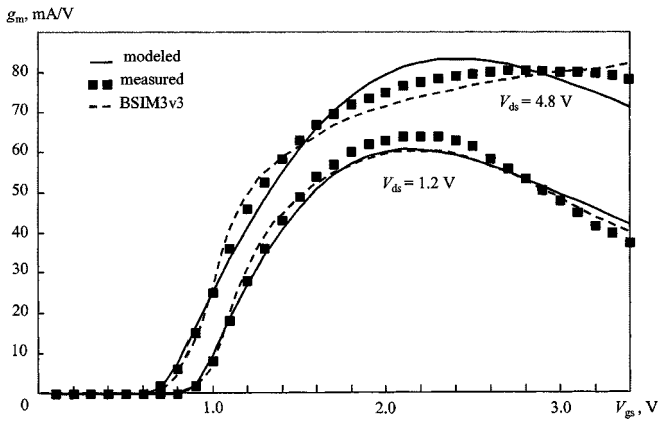

Fig. 9. Measured and modeled $g_m(V_{\rm gs})$ dependencies of a low-voltage MOSFET.

circuits operating below 2 GHz, which covers most of the commercial wireless applications [19], [23]. For example, for the MOSFET with the depletion region doping concentration value $N_A = 1700\ \mu\text{m}^{-3}$, the phase of the small-signal transconductance g_m near f_T reaches the value of only -15° [8].

E. Temperature Dependence

Silicon MOSFET devices are very sensitive to the operation temperature T and their characteristics are strongly temperature dependent [8]. The main parameters responsible for this are the effective carrier mobility μ and threshold voltage $V_{\rm th}$. The effect of these parameters on the transistor characteristics is such that a temperature increase leads to the increase of the drain current through $V_{\rm th}(T)$ and to the decrease of it through $\mu(T)$. Increasing temperature decreases the slope of the $I_{\rm ds}$–$V_{\rm gs}$ curves, and it can be found at a certain value of $V_{\rm gs}$, at which the drain current becomes practically temperature independent over a large temperature range. The change in the value of $V_{\rm th}$ with temperature in a wide range from -50 °C up to 200 °C represents a nonlinear function, which is slowly decreased with temperature [13], and can be approximated by the trinomial

$$V_{\rm th}(T) = V_{\rm th}(T_{\rm nom}) + V_{T1}\Delta t + V_{T2}\Delta t^2 \qquad (20)$$

where $\Delta t = T - T_{\rm nom}$, $T_{\rm nom} = 27$ °C (300 K), and V_{T1} and V_{T2} are the linear and quadratic temperature coefficients for threshold voltage.

The change the value of μ with temperature can be taken into account by introducing the appropriate temperature change of $I_{\rm sat}$ in (12). Thus, as the temperature change of $I_{\rm sat}$ represents

TABLE III
SIMULATED I–V MODEL PARAMETERS OF A LOW-VOLTAGE MOSFET

Parameters	α, 1/V	β, 1/V	λ, 1/V	V_{th}, V	I_{th}, mA	S_{th}, mA/V	I_{sat}, A	n	σ
Values	0.58	0.17	0	0.9	0.029	10.5	0.31	0.78	0.05

an almost straight line [13], which is decreased with temperature, the temperature dependence of $I_{\rm sat}(T)$ can be approximated by the linear function

$$I_{\rm sat}(T) = I_{\rm sat}(T_{\rm nom}) + I_T \Delta t \tag{21}$$

where I_T is the linear temperature coefficient for saturation current.

The temperature dependencies of the MOSFET capacitances and series resistances can be described by the following linear equations [12], [24]:

$$C(T) = C(T_{\rm nom}) + C_T \Delta t \tag{22}$$

$$R(T) = R(T_{\rm nom}) + R_T \Delta t \tag{23}$$

where $C = (C_{\rm gs}, C_{\rm ds}, C_{\rm gd})$, $R = (R_g, R_s, R_d)$, R_T, and C_T are the linear temperature coefficients for the capacitances and resistances, respectively.

F. Self-Heating

In order to correctly describe the behavior of the power MOSFET devices at all biasing conditions, it is necessary to take into account the self-heating effect. For example, at a highly dissipated power region, it leads to the negative output differential resistance due to the reduction of $I_{\rm ds}$ at high values of $V_{\rm gs}$. The effect of the negative conductance at high biasing can be taken into account if the nonlinear I–V model is rewritten in the following form:

$$I_{\rm ds}(T, p_T) = \frac{I_{\rm ds}(T)}{1 + p_T V_d I_{\rm ds}(T)} \tag{24}$$

where the drain–current source $I_{\rm ds}(T)$ is presented by (12), $V_d = V_{\rm ds}/\sqrt{1 + (\omega\tau_{\rm th})^2}$, p_T is self-heating temperature coefficient, $V_{\rm ds}$ is the drain–source supply voltage, $\tau_{\rm th} = R_{\rm th}C_{\rm th}$ is the thermal time constant, $R_{\rm th}$ is the thermal resistance, and $C_{\rm th}$ is the thermal capacitance. A thermal equivalent circuit can be added to the large-signal LDMOSFET model, as is shown in [25]. The thermal resistance $R_{\rm th}$ can be extracted from the temperature measurement of the dc characteristics. Since the slope of the dc measured $I_{\rm ds}$–$V_{\rm ds}$ curves changes its sign from positive to negative, the temperature coefficient p_T can be evaluated using the following condition:

$$\frac{dI_{\rm ds}(T, p_T)}{dV_{\rm ds}} = 0. \tag{25}$$

As a result,

$$p_T = \frac{1}{I_{\rm ds}^2(T)} \frac{dI_{\rm ds}(T)}{dV_{\rm ds}} \tag{26}$$

where $I_{\rm ds}$–$V_{\rm ds}$ curves are defined by pulsed measurement at ambient temperature T and a value of $I_{\rm ds}(T)$ is fixed the same as for a zero slope of $I_{\rm ds}(T, p_T)$.

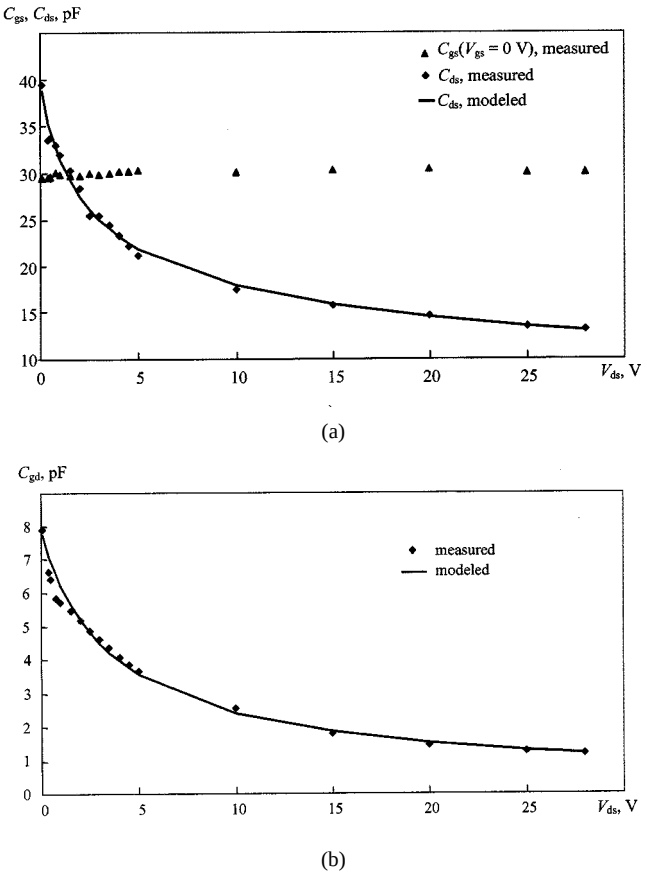

Fig. 10. Measured and modeled: (a) $C_{\rm gs}(V_{\rm ds})$, $C_{\rm ds}(V_{\rm ds})$ and (b) $C_{\rm gd}(V_{\rm ds})$ dependencies of a 28-V LDMOSFET.

TABLE IV
SIMULATED C–V JUNCTION MODEL PARAMETERS

Capacitance	$C_{\rm gd(ds)o}$, pF	m	φ, V
$C_{\rm gd}$	7.88	0.8	2.94
$C_{\rm ds}$	39.42	0.33	1.0

The thermal time constant $\tau_{\rm th}$ can be extracted by comparing pulsed $I_{\rm ds}$–$V_{\rm ds}$ curves calculated under a different pulsewidth and duty factors. A plot of $I_{\rm ds}$ as a function of pulsewidth under the fixed gate–source and drain–source biasing voltages gives an appropriate value of $\tau_{\rm th}$.

IV. MODEL SMALL-SIGNAL VERIFICATION

In order to verify the new empirical I–V model, a 28-V high-power LDMOSFET with gatewidth of $W = 4$ cm and gate length of $L = 1.1$ μm type LP801 from Polyfet RF devices was used. In Fig. 6, the theoretical and experimental (pulsed measurement) $I_{\rm ds}$–$V_{\rm ds}$ curves are presented. The

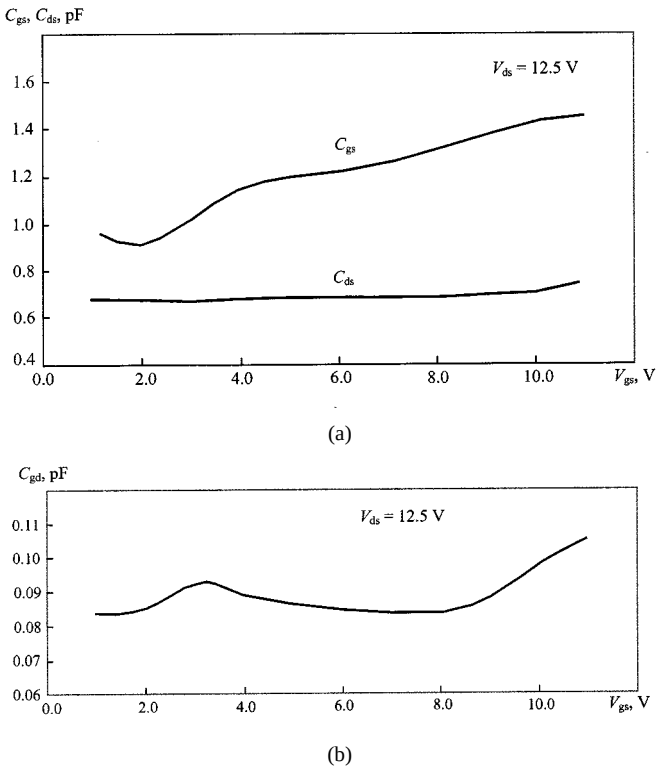

Fig. 11. Measured: (a) $C_{\rm gs}(V_{\rm gs})$, $C_{\rm ds}(V_{\rm gs})$, and (b) $C_{\rm gd}(V_{\rm gs})$ dependencies of a 12.5-V LDMOSFET cell.

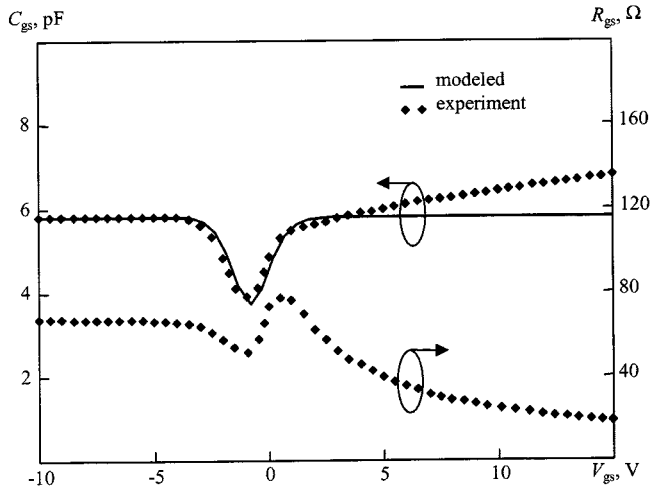

Fig. 12. Measured and modeled gate–source voltage dependencies of $C_{\rm gs}$ and $R_{\rm gs}$.

resulting current root-mean-square error of a family of the model $I_{\rm ds}$–$V_{\rm ds}$ curves is 0.5%. The values of simulated model parameters are indicated in Table II. As follows from Table II, the $I_{\rm ds}$–$V_{\rm ds}$ approximation is sufficiently simple and accurate in the case of a high-power LDMOSFET and requires only six fitting parameters, of which four of them are directly determined by the experimental curves.

Substantially better fitting for $I_{\rm ds}$–$V_{\rm gs}$ curve and $g_m(V_{\rm gs})$ dependence in comparison with the results obtained by extensive two-dimensional simulations [13] is realized (Fig. 7). The deviation of the average difference error of the model $I_{\rm ds}$–$V_{\rm gs}$ curve

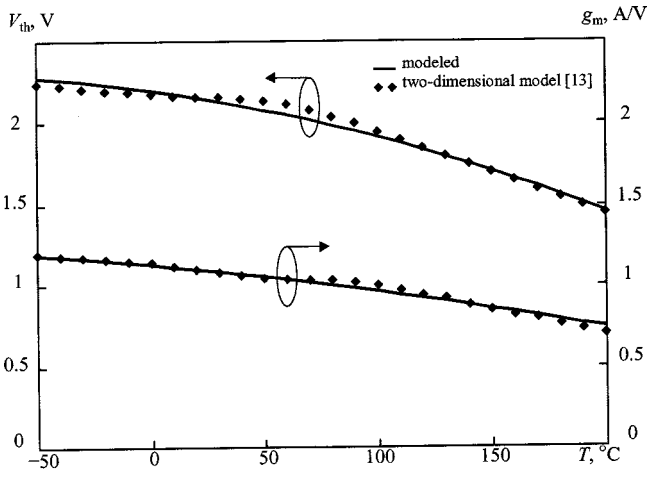

Fig. 13. Modeled temperature dependencies of $V_{\rm th}$ and g_m.

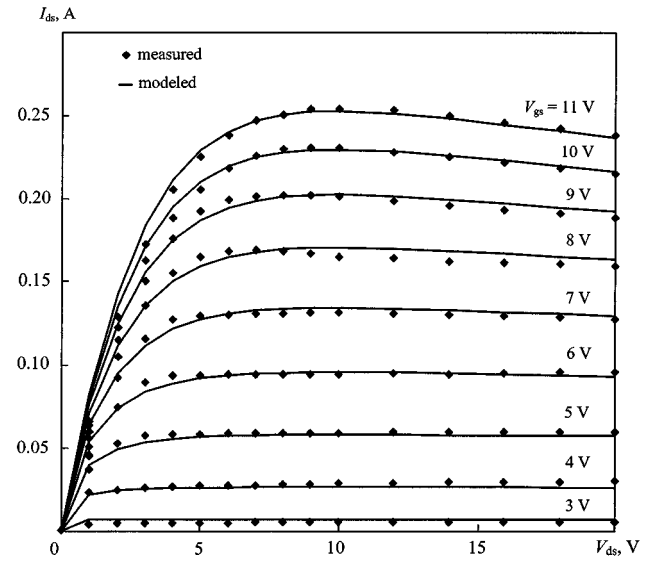

Fig. 14. Measured and modeled $I_{\rm ds}$–$V_{\rm ds}$ curves of a 12.5-V LDMOSFET cell.

from the experimental one is 4.4%. It can be seen that a proposed empirical model allows one to describe smoothly and sufficiently accurately the behavior of both $I_{\rm ds}$ and g_m as a function of $V_{\rm gs}$ in a weak-inversion region, as well as in the strong-inversion region of the LDMOSFET operation.

To verify an applicability of the proposed model to low-voltage MOSFET devices, the appropriate low-voltage RF power MOSFET with the gatewidth of $W = 2$ mm was chosen [23]. In Fig. 8, the modeled and experimental $I_{\rm ds}$–$V_{\rm ds}$ curves are presented. In this case, to improve the sensitivity of drain current $I_{\rm ds}$ under large values of $V_{\rm gs}$, the term $(1 - \beta V_{\rm gs})$ was introduced to the approximation function (12). The resulting root-mean-square error of a family of the $I_{\rm ds}$–$V_{\rm ds}$ curves is 0.42%. The values of $I_{\rm ds}$–$V_{\rm ds}$ model parameters are presented in Table III. The model $I_{\rm ds}$–$V_{\rm gs}$ curves were compared with the same characteristics calculated by means of the BSIM3v3 model developed for modeling of deep submicrometer device [23]. The results presented in Fig. 9 show a good agreement

TABLE V
SIMULATED C_{gs}–V_{gs} MODEL PARAMETERS

Capacitance	C_{gso}, pF	S_1, pF/V	S_2, pF/V	V_{s1}, V	V_{s2}, V	C_s, pF	C_{gsmax}, pF
C_{gs}	9.85	–0.8	1.2	–2.1	–0.84	0.94	5.83

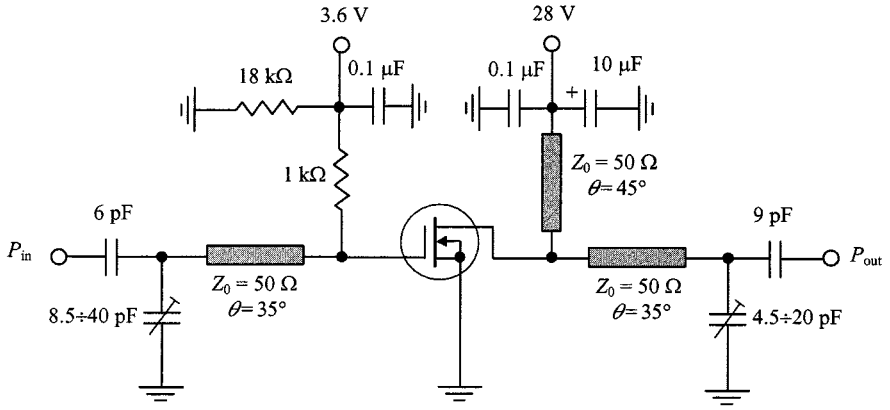

Fig. 15. Equivalent circuit of a 500-MHz 20-W LDMOSFET amplifier.

with the experimental curves and practically the same as in the case of the BSIM3v3 approximation.

The results of the approximation of C_{ds} and C_{gd} as the junction capacitances for LP801 device are given in Fig. 10(a) and (b), respectively. The fitting parameters of the approximation $C_{gd}(V_{ds})$ and $C_{ds}(V_{ds})$ curves are presented in Table IV. The resulting averaged differential deviation of model values from the measured ones for the gate–drain capacitance and drain–source capacitance is less than 5%.

In Fig. 11(a) and (b), the measured $C_{gs}(V_{gs})$, $C_{ds}(V_{gs})$ and $C_{gd}(V_{gs})$ curves for a 12.5-V LDMOSFET cell with a gate geometry of $L = 1.25$ μm and $W = 1.44$ mm are presented, respectively, which indicate practical independence of C_{gd} and C_{ds} on V_{gs}. A linear increase of all capacitances at high values of gate bias is provided with the increase of the dissipation power under dc measurement. The dependence $C_{gs}(V_{gs})$ has a predictable minimum near threshold voltage $V_{th} = 2.3$ V and can be readily approximated by hyperbolic tangent function. The behavior of C_{gd} as a function of V_{gs} with a small increase near V_{th} is typical for high-power silicon LDMOSFET devices [25].

Fig. 12 shows the measured and modeled gate–source voltage dependencies of $C_{gs}(V_{gs})$ and $R_{gs}(V_{gs})$ for a 28-V MOSFET with a horizontal channel of $L = 5$ μm. The fitting parameters of the approximation $C_{gs}(V_{gs})$ curve are given in Table V. Some growth of the experimental $C_{gs}(V_{gs})$ dependence at high values of V_{gs} is also the result of high power dissipation under dc measurement. As follows from Fig. 12, the gate–source capacitance C_{gs} increases with the increase of gate–source voltage V_{gs} in the strong-inversion region, whereas channel resistance R_{gs} decreases at the same changes of V_{gs} so that the charging time τ_g insignificantly reduces and can be approximated by a constant.

In Fig. 13, the modeled temperature dependencies of $V_{th}(T)$ and $g_m(T)$ for an LP801 device are presented. The results obtained by using the simple approximations (20) and (21) with the values of $V_{T1} = (2$ mV/°C, $V_{T2} = -8.55$ μV/°C)^2, and $I_T = -4.5$ mA/°C show a good prediction of the I–V curves in a wide temperature range.

Fig. 14 shows a comparison between the measured (dc measurement) and modeled I_{ds}–V_{ds} curves for a 12.5-V LDMOSFET sell with gate geometry of $L = 1.25$ μm and $W = 1.44$ mm. As follows from Fig. 14, the effect of self-heating is described quite accurately by (23) for the following model parameters: $p_T = 0.035$ 1/AV, $\alpha = 0.2$ 1/V, $\beta = \sigma = 0$, $S_{th} = 37$ mA/V, $I_{th} = 1.5$ mA, $V_{th} = 2.25$ V, $I_{sat} = 0.48$ A, $n = 1$, and $\lambda = 0.0005$ 1/V.

V. LARGE-SIGNAL APPLICATION

Using the Ansoft CAD simulator Serenade 8.5, linear circuit analysis and amplifier nonlinear simulation were performed for the LDMOSFET device with gate geometry of $L = 1.25$ μm and $W = 4$ cm at operating frequency of 500 MHz. Linear and nonlinear device model parameters were extracted from on-wafer measurements. The parameters of the matching circuit elements were chosen according to the results of the CAD simulation for the high-efficiency operating mode of the power amplifier. The experimental test structure of a single-stage 20-W LDMOSFET power amplifier is shown in Fig. 15. Two T-section transformers with series microstrip lines and parallel variable capacitors have been used as the input and output matching circuits. The matching circuits were fabricated on epoxy glass copper-clad laminate substrates and the characteristic impedances of all microstrip lines are equal to 50 Ω. In order to avoid low-frequency parasitic oscillations, the electrolytic capacitor of 10 μF was connected in parallel to the drain supply.

The measured (solid lines) and simulated (dotted lines) characteristics of the output power and power gain as a function of the input power are presented in Fig. 16. Maximum level of the

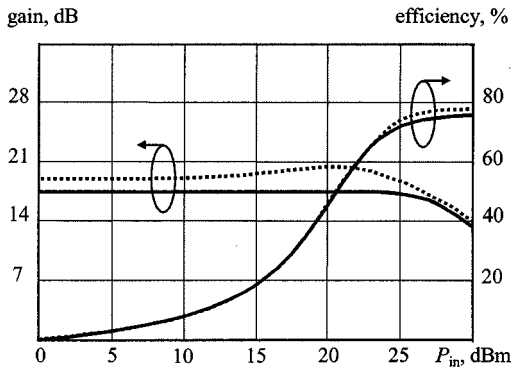

Fig. 16. Simulation (dotted line) and experimental (solid line) results of a 20-W LDMOSFET amplifier.

output power of 20 W with the drain efficiency of 76% and dc collector current of 0.94 A has been achieved. The difference between measured and modeled values of power-aided efficiency is practically negligible. The deviation of measured from simulated values of power gain of about 2–3 dB can be explained by sufficient gain sensitivity to the gate resistance, the exact value of which is difficult to calculate for the high-power device taking into account the distributed nature of the wide gate structure.

VI. Conclusions

In this paper, a new simple nonlinear model has been developed on the basis of the well-founded small-signal MOSFET equivalent circuit. The proposed model is based on new simple empirical equations, which completely describe the nonlinear behavior of the drain–current source and device intrinsic capacitances, and satisfies the charge conservation condition. The fitting parameters in these equations are easily determined by the measured results with subsequent small clarifications under the optimization procedure. To predict the variations of the current–voltage characteristic and equivalent-circuit elements with temperature and self-heating, simple equations have been proposed. The presented model is a good compromise between the simplicity of the numerical calculations and the accuracy of the final results, and can be easy inserted in any circuit simulators. By analytically combining the described linear external and nonlinear intrinsic elements, high-power and low-voltage silicon MOSFETs can be completely characterized and implemented in RF circuit design.

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