Three-Dimensional High-Frequency Distribution Networks—Part II: Packaging and Integration

Rashaunda M. Henderson, *Member, IEEE*, Katherine J. Herrick, *Member, IEEE*, Thomas M. Weller, *Member, IEEE*, S. V. Robertson, R. T. Kihm, and Linda P. B. Katehi, *Fellow, IEEE*

***Abstract*—This paper describes the implementation and packaging of the components, desribed in Part I of this paper, to realize a three-dimensional W-band distribution network.**

***Index Terms*—Coplanar transmission lines, micromachining, microwave circuits.**

I. Introduction

In order to develop high power at millimeter-wave frequencies using monolithic technology, a number of techniques have been proposed to combine the power generated by multiple solid-state devices. These techniques perform quasi-optical, spatial, and circuit power combining, and rely on circuit architectures that can handle complexity and provide high power-combining efficiency. The use of multiple devices along with imposed constraints for reduced coupling and high isolation between adjacent channels results in tradeoffs between size, loss, performance, and efficiency. Monolithic circuits that transmit moderate power at higher frequencies utilize a variety of architectures where power is generated and combined on-wafer via resistive or reactive circuit combiners [1] or in space by radiating the power via appropriately designed antennas [2]. An important characteristic of circuit and spatial combining techniques is the dependence of their power-combining efficiency on the loss of the integrated distribution network. Excessive loss found in the combining stages and performance sensitivity to matching networks are two of the most important factors that have led to designs using other quasi-optical techniques [3]. To make spatial combining a successful power-combining method, a circuit architecture is needed, where circuit miniaturization is accomplished with three-dimensional (3-D) integration and on-wafer conformal packaging. Appropriate integration techniques incorporated in the design of the circuit not only offer size reductions and added flexibility in system design, but also provide greater ability to obtain uniform amplitude and phase at each element [4], [5].

To allow for higher integration and better performance at higher operating frequencies, silicon (Si) micromachining has recently been identified as an enabling technology that can provide novel and cost-effective solutions. The mechanical, thermal, and electrical properties of high-resistivity Si compare well with the best ceramics, thus making it an appropriate substrate for this type of application. Si micromachining has been used to improve the performance of conventional transmission lines [6]–[9], and drastically reduce its size due to the capability to shield the circuits on-wafer. On-wafer packaging has been successfully demonstrated in simple circuits up to W-band [10], but herein is extended to fairly complex architectures. With recent advances in vertical wafer transition designs [11], the possibility to create multilayer high-density Si micromachined circuits is now becoming a reality.

This paper presents the development of a conformally packaged distribution network to be used in a W-band monolithic three-dimensional (3-D) transmit tile module (Fig. 1). The transmit module of Fig. 1 combines four electrical functions and distributes the circuits required for them on four different wafers. Specifically, the four electrical functions and corresponding wafers on which their circuits are printed on are: 1) distribution of the input power into four monolithic microwave integrated circuits (MMICs) (wafer #1); 2) distribution of the amplified power into 16 ports (wafer #2); 3) coupling of this power through slots to 16 radiating elements (wafer #3); and 4) effective radiation of the power into free space (wafer #4). The functions of each Si wafer and its metal layers are detailed in Table I.

In a transmit module architecture, such as the one presented in Fig. 1, design emphasis is placed on the circuits following the MMIC amplifier chips. Primary issues in design are the low loss of the output distribution network (wafer #2), effective coupling to the antennas (wafer #3), and high radiation efficiency (wafer #4). The circuit designs that have addressed the last two design issues have been recently presented elsewhere and will not be repeated here [12], [13]. The emphasis of this paper is in the development of the output distribution network with emphasis on minimizing parasitic mechanisms such as loss and electromagnetic coupling in order to optimize power efficiency, as well as power and phase balance between the radiating elements.

Manuscript received May 5, 1999. This work was supported by the Defense Advanced Research Projects Agency–Hughes under Contract FR-573 420-SR8 and under Contract ONR-N00014-95-1-0546.

R. M. Henderson was with the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA. She is now with the Materials and Structures Laboratories, Motorola Semiconductor Product Sector, Tempe, AZ 85284 USA.

K. J. Herrick and L. P. B. Katehi are with the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA.

T. M. Weller is with the Department of Electrical Engineering, University of South Florida, Tampa, FL 33620 USA.

S. V. Robertson was with the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA. He is now with the Wireless Technology Laboratory, Lucent Technologies, Whippany, NJ 07981 USA.

R. T. Kihm is with Electronics Systems, Microwave Center, Raytheon Company, El Segundo, CA 90245 USA.

Publisher Item Identifier S 0018-9480(00)08711-1.

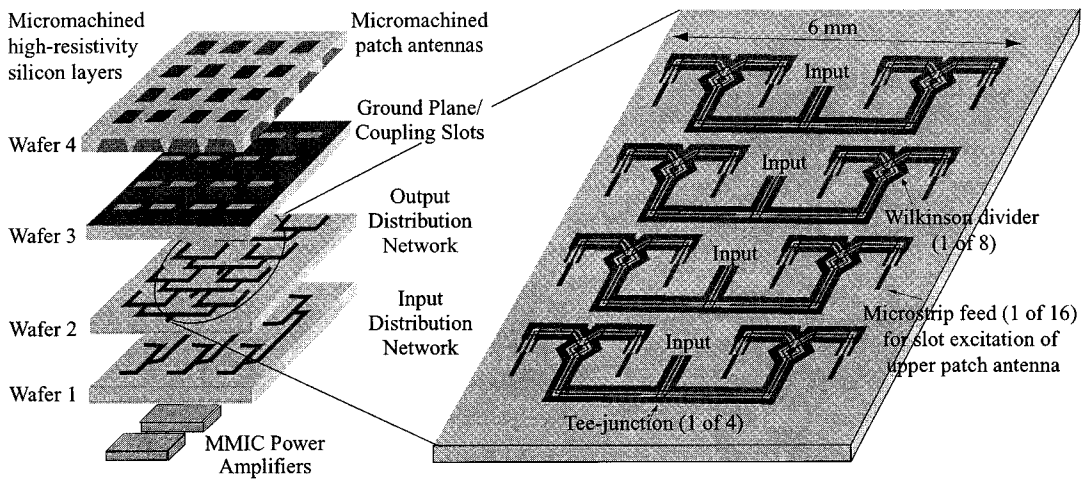


Fig. 1. Conceptual drawing of MMIC power cube with expanded view of distribution network layout.

TABLE I
FUNCTION OF 3-D MODULE LAYERS OF FIG. 1

Layer	Si	Metal
1	Heat sink/MMIC access	Input distribution network
2	Si micromachined layer On wafer packaging	Output distribution network
3	Si micromachined layer On wafer packaging	H-slot antenna feed
4	Si micromachined layer For surface wave reduction	Patch antenna

Fig. 1 shows a detailed schematic for the output distribution network printed on wafer #2. The total area available for distributing power to the antennas is 6 mm $\times$ 6 mm, thus imposing very strict requirements on high circuit density. The need to transition vertically, while at the same time provide high density, has lead to choosing the finite ground coplanar (FGC) waveguide as the primary interconnect geometry. Using FGC lines requires air bridges for the equalization of the ground plane potential and suppression of the slot line mode excited at line discontinuities. To preserve the integrity of the air bridges, when stacking and bonding the wafers, micromachined packages are monolithically developed along with the circuits.

The work presented in this paper focuses on the development of the distribution network, the choice of the interconnect technology, and the design of an appropriate package that reduces unwanted parasitics. The 3-D distribution network is made of circuit components presented in [14] of this series, which are optimized to suppress parasitic effects generated by the presence of multiple dielectric layers and the proximity of extended conducting planes. Using the presented circuit architecture, high density can be achieved by integrating wafers vertically and by utilizing both sides of the wafer for printing circuit components. To achieve on-wafer packaging while integrating multiple circuit functions, the same wafers carry the circuit components in addition to the monolithic fabricated cavities that provide shielding and good circuit isolation. In addition to packaging, the shielding cavities are utilized to reduce parasitic mechanisms generated by the stacking of the wafers and the close proximity of extended metallic planes.

The power distribution network is comprised of multiple bends, impedance steps, tee junctions, and Wilkinson dividers (as shown in Fig. 1). Individual component performance is critical to feed network efficiency and, for this reason, geometry optimization for lowest insertion and return loss has been effectively pursued.

The following sections present the basic design methodology, which utilizes high-resistivity Si micromachining and FGC interconnect technology to achieve optimal performance via 3-D circuit integration. In addition, theoretical and experimental results are presented confirming expected circuit performance.

II. INTERCONNECT GEOMETRY

In the vertical integration of high-frequency circuits, the ground conductors must follow the signal line as closely as possible in order to reduce parasitic radiation and prohibit the excitation of higher order modes. This need is exacerbated when the interconnects operating at high frequencies transition vertically into adjacent planes. FGC waveguide [see Fig. 2(a)] is a uniplanar line with the ground planes and signal conductors occupying the same wafer interface. The uniplanar structure of the line is responsible for the high field concentration at the wafer interface. As a result, line performance depends mostly on line geometry and is not sensitive to wafer thickness variations [8], [9]. The FGC line has the potential to minimize parasitic effects when transitioned vertically and, for this reason, was chosen for the distribution network described herein. The dimensions of this line were specified by the design rules established by [8] and [9]. These design rules specify a total linewidth (W_T) to provide single mode operation and eliminate parasitic radiation. To achieve high integration while keeping adjacent ground-plane separation to a minimum distance of 80 μm (as specified by module size requirements),

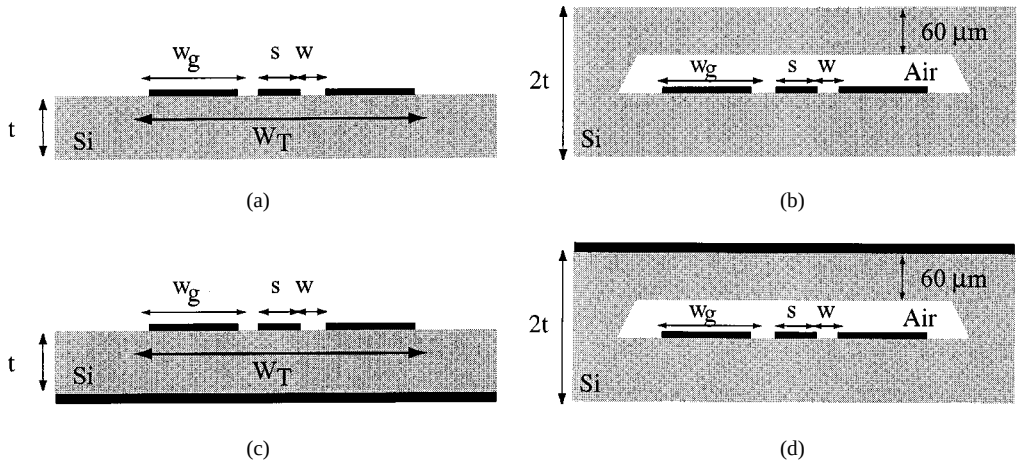


Fig. 2. 3-D environment geometries for the transmission lines. (a) Conventional FGC. (b) Packaged FGC. (c) Conductor-backed FGC. (d) Cavity-backed packaged FGC.

W_T is limited to 300 μm, while the aspect ratio necessary to realize 50 Ω is equal to 0.45, as shown by

$$\frac{s}{s+2w} = 0.45 \tag{1}$$

where s is the center conductor width and w is the aperture width. The dimensions chosen for the conventional line are $s = 40$ μm, $w = 24$ μm, ground-plane width $w_g = 106$ μm, and wafer thickness $t = 100$ μm. Extracting capacitance values using Ansoft's Maxwell 2D simulator, the characteristic impedance is calculated to be 49.98 Ω with an effective dielectric constant equal to 6.156.[1] In order not to excite higher order modes, W_T has to be less than $\lambda_g/2$, where λ_g corresponds to the guided wavelength of the maximum operating frequency according to

$$W_T = 2W_g + 2w + s < \lambda_g/2. \tag{2}$$

At the design frequency, $f_c = 94$ GHz, $\lambda_g/2$ is equal to 632 μm, a value much greater than the $W_t = 300$ μm, implying that the line operates free of higher order modes.

The design rules listed above apply to FGC lines printed on a single layer semiinfinite high-resistivity Si substrate ["conventional FGC" in Fig. 1(a)], and specify line geometries that demonstrate excellent performance at frequencies as high as W- and D-bands. In multilayered configurations, the vertical stacking of substrates and the close proximity of the various circuit components necessitates a thorough understanding of the propagating wave excited by the structure. Although the electromagnetic fields in coplanar waveguide (CPW) lines are fairly well confined to the aperture regions, it is important to further reduce interactions between adjacent circuits (laterally and vertically), in order to achieve the highest possible integration. Electromagnetic parasitic interactions, known as crosstalk, are due to substrate modes and/or proximity effects and result in degraded electrical performance. This parasitic coupling can be reduced or eliminated by appropriate shielding. Recent work has demonstrated that on-wafer packaging has the ability to effectively isolate circuits while preserving performance integrity and providing very small size and low-cost solutions. In the vertically integrated circuits studied in this paper, on-wafer packaging does not only isolate adjacent circuits, but provides mechanical protection to the air bridges.

The distribution network for the tile module is utilized in a 3-D environment with an extended metal plane placed above, to provide the ground for the micromachined antennas. The presence of this ground just 100 μm above the printed circuits introduces electromagnetics effects, the impact of which on line performance is discussed herein. When a conventional FGC line is backed by a metal plane [("conductor-backed FGC" in Fig. 2(c)], the characteristic impedance decreases to 46.73 Ω from 50 Ω and ε_{eff} increases to 6.428 from 6.156. This suggests that even though the field lines are concentrated in the aperture regions, the presence of the conductor plane attracts the fields slightly more into the substrate [12], a predictor of increased parasitic capacitance. To reduce this parasitic capacitance between the line and backing metal plane, an air cavity is micromachined ["cavity-backed packaged FGC" in Fig. 2(d)].

Similar air cavities are used in this paper to protect air bridges and reduce parasitic effects due to coupling to adjacent metal planes through the substrate. To understand the effects of these cavities on line characteristics, a static solver has been utilized to perform a parametric study of one of the most critical parameters, i.e., cavity height. The results have indicated that cavity heights greater than 40 μm are noninvasive and do not affect the line impedance. For this reason and for the ease in fabrication, a 40-μm cavity height has been chosen for the lines of Fig. 2(b) and (d).

As stated previously, the FGC line is printed on 100-μm-thick high-resistivity Si ($\varepsilon_r = 11.7$) with approximately 1-μm evaporated gold (Au). The conventional line shown in Fig. 2(a) is used as a reference. Its performance has been measured up to W-band and results in a characteristic impedance $Z_o = 52\,\Omega$, and effective dielectric constant $\varepsilon_{\text{eff}} = 6.3$. All experimental results have been obtained from on-wafer measurements using an HP 8510C vector network analyzer on an Alessi probe station with 100-μm-pitch GGB Picoprobes calibrated with the Na-

[1]Maxwell 2D, Ansoft Corporation, Pittsburgh, PA, 1994.

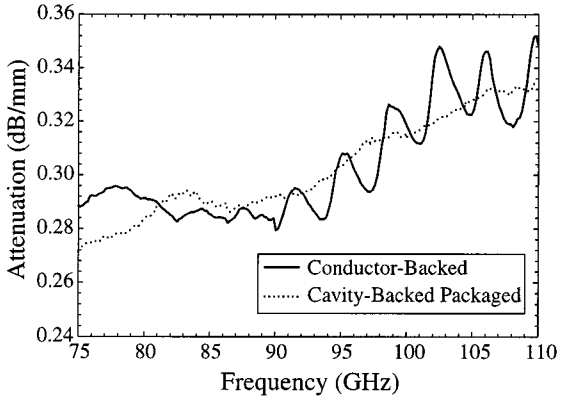


Fig. 3. Attenuation for line architectures of Figs. 2(c) and (d).

tional Institute of Standards (NIST) Multical program.[2] Measured propagation characteristics for the architectures shown in Fig. 2 indicate performance differences in conductor- and cavity-backed FGC lines. Specifically, the ε_{eff} for conductor- and cavity-backed packaged FGC lines is 6.4 and 6.3 at 94 GHz, respectively.

In Fig. 3, measured attenuation is presented for the two multilayer architectures and indicates a severe ripple in the conductor-backed FGC line caused by parasitic coupling to the ground plane. By placing the micromachined air cavity between the FGC line and the conductor plane, the effect is minimized as indicated by the loss data for the cavity-backed packaged line, indicating no oscillations.

In addition to studying a single transmission line in a multilayer environment, coupling effects between adjacent FGC lines have been examined. The coupling between two vertically integrated multilayer transmission lines has been computed using an integral-equation-based numerical solver.[3] For this simulation, two through lines with the same aspect ratios as all previous lines (40-μm center conductors, 24-μm apertures, and 106-μm ground planes) are used. In each case, the lateral spacing (s) between lines varies from 0 to 400 μm center to center and the vertical spacing is fixed at 100 μm. Cross coupling is estimated by measuring the insertion loss across ports 1 and 2 while leaving ports 3 and 4 open, as shown in Fig. 4. Due to the open conditions at ports 3 and 4, the measured coupling is 6 dB higher than the coupling observed between two ideally matched lines. Simulated results show a ripple in cross coupling (S_{21}) between lines separated by a uniform dielectric substrate (Fig. 5) due to parasitic substrate capacitance. The level of coupling for the lines laterally separated by 0 and 100 μm is as high as -10 dB between 90–95 GHz. By reorienting the air cavities to interrupt the uniformity of the substrate layer between the two lines, the ripple is eliminated completely and the coupling reduces by 8 dB to -18 dB over the entire frequency band (75–110 GHz), as seen in Fig. 6.

[2]R. B. Marks and D. F. Williams, Program MultiCal, Rev. 1.00, NIST, Boulder, CO, Aug. 1995.

[3]IE3D, Release 4, Zeland Software Inc., Fremont, CA, 1997.

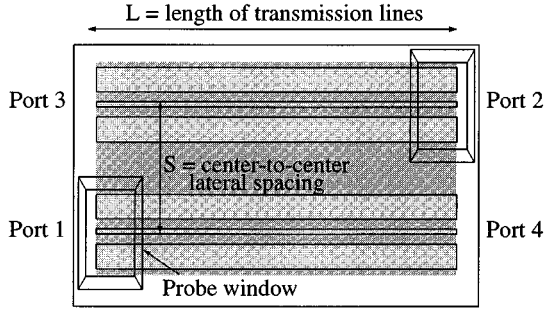


Fig. 4. Schematic for FGC-to-FGC coupling from ports 1 to 2.

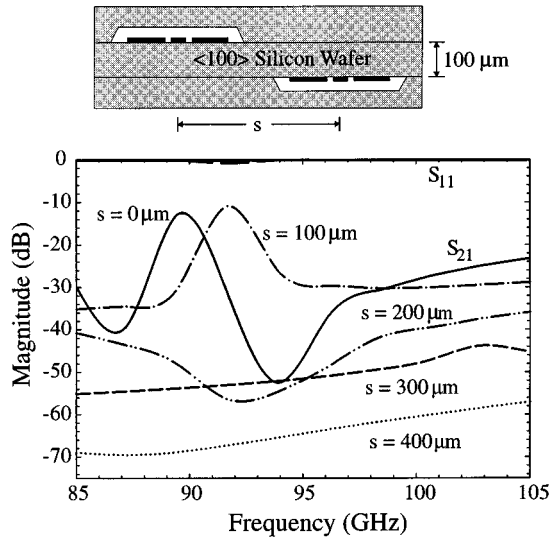


Fig. 5. FGC-to-FGC coupling through 100-μm Si wafer (s= center-to-center lateral spacing).

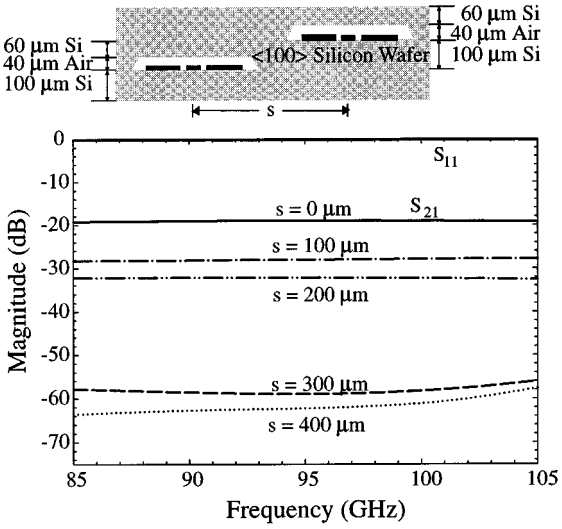


Fig. 6. FGC-to-FGC coupling through 60-μm Si 40-μm air cavity (s= center-to-center lateral spacing).

III. Vertically Integrated Distribution Network

As discussed previously, when the circuits are placed in a multilayer environment, there is a need to develop an air cavity

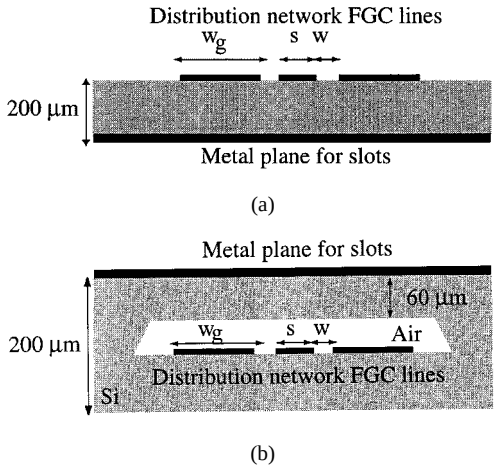


Fig. 7. Multilayer architectures for the 3-D distribution network. (a) Conductor-backed FGC. (b) Cavity-backed packaged FGC.

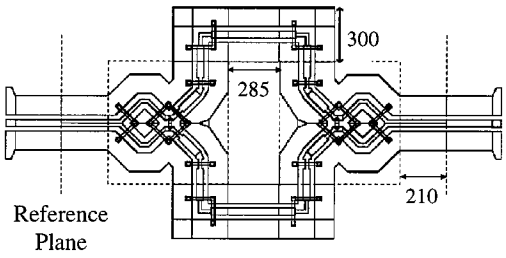


Fig. 8. Schematic of a back-to-back Wilkinson power divider.

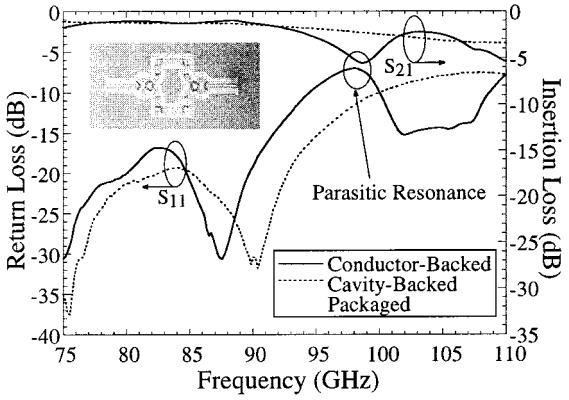


Fig. 9. Measured S-parameters of back-to-back divider for conductor- and cavity-backed packaged environments.

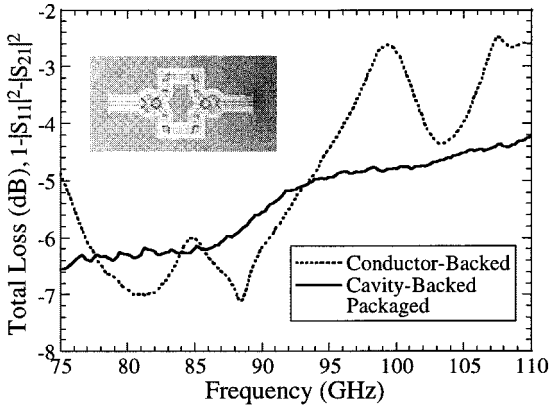


Fig. 10. Total loss of back-to-back divider for conductor- and cavity-backed packaged environments.

TABLE II
MEASURED LOSS OF INDIVIDUAL COMPONENTS FROM 85 TO 95 GHz (PEAK PERFORMANCE)

Component	Cavity-backed Packaged (dB)	Conductor-backed (dB)
Tee	-0.20	-0.4 to -0.6
Wilkinson	-0.40	-0.6 to -1
Right angle bend	-0.10	-0.2 to -0.4
Transmission line loss (1 mm)	-0.26	-0.28

appropriate for protection of the air bridges, in addition to provide electromagnetic shielding. The air cavity is designed to package the line, as shown in Fig. 2(d), and is fabricated on a 100-μm-thick Si substrate with 8500-Å SiO_2 masking layer. Probe access windows are etched into the substrate to allow for on-wafer measurements. The air cavity and access windows are defined using photolithography and anisotropically etched. The two wafers are aligned using a bonding station with 10 ± 5-μm accuracy.

In the following sections, the effects of the backing planes on the performance of the distribution network and the improvements obtained by use of the micromachined cavities will be discussed. To begin, the individual circuit components that comprise the distribution network will be presented and, finally, the section discussing the performance of the whole network will be presented.

A. Individual Components—Effects of Packaging

Among the various individual components, a back-to-back Wilkinson divider configuration is used to show the effects of adjacent metal planes on circuit performance and discuss performance improvements achieved by the use of micromachined cavities. This Wilkinson divider is a key component of the whole distribution network. It is the component mostly responsible for the loss of the network, as it will become obvious from the discussions presented in following sections. Comparisons are made between the performance of the conductor-backed [see Fig. 7(a)] and cavity-backed packaged circuits [see Fig. 7(b)] in terms of insertion loss and return loss. Fig. 8 shows the schematic of a back-to-back Wilkinson divider, while Fig. 9 gives the measured response. At 98 GHz, a parasitic resonance occurs in the conductor-backed circuit that increases the insertion loss to -5.6 dB and return loss to -7 dB indicating 2.6-dB total loss $(1 - S_{11}^2 - S_{21}^2)$ (Fig. 10). The cavity-backed packaged circuit, however, does not exhibit this resonance, but shows an insertion loss of less than -1.5 dB up to 97 GHz. This translates to an individual Wilkinson S_{21} of -0.40 dB after deembedding the feeding-line loss.

Similar performance comparisons between the individual components in conductor- and cavity-backed packaged arrangements are listed in Table II. These values represent the

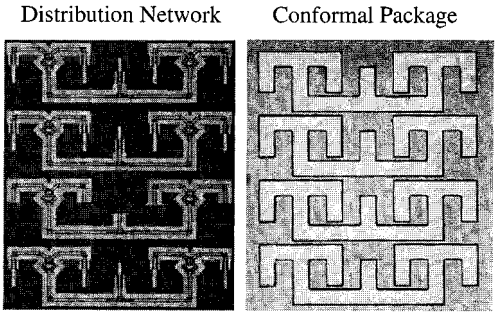


Fig. 11. Photograph of distribution network and conformal package. Ground-to-ground spacing between networks is 80 μm.

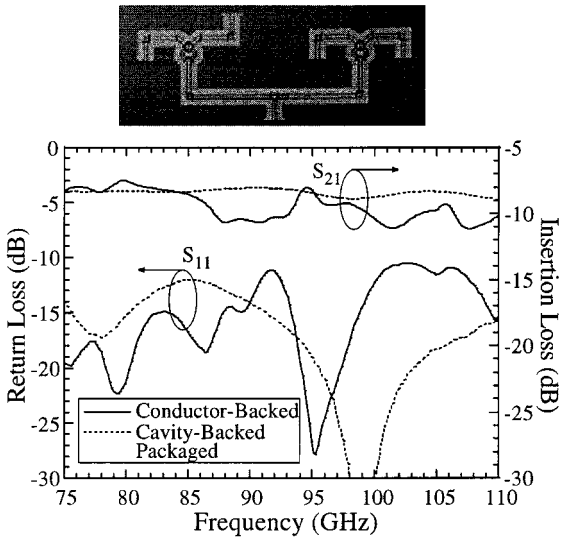


Fig. 12. Measured S-parameters of distribution network for conductor- and cavity-backed packaged environments from 75 to 110 GHz.

best performance insertion loss within the frequency range of 85–95 GHz. Results indicate that the performance of the cavity-backed packaged circuits is substantially better not only when compared to the conductor-backed, but also to the conventional ones. It is worth noting that conventional circuits demonstrate a variation by as much as ± 0.2 dB over the band due to parasitic effects caused by the proximity of the conductor planes, whereas performance variation in packaged circuits is on the order of ± 0.05 dB due to the reduced sensitivity of the circuit with regards to the conductor proximity.

B. Distribution Network—Effects of On-Wafer Packaging

Individual component performance is critical to feed network efficiency and warrants extensive measurements for different line architectures. Combining the individual components in the distribution network has led to a self-packaged architecture for the distribution network, as shown in Fig. 11. Measurements of the distribution network's performance in the four-divider network environment are shown in Fig. 12. The presented results indicate that individual component parasitics, in the case of conductor-backed circuit, combine to produce an insertion loss as high as 11 dB (layout 2, Fig. 13). On the contrary, the

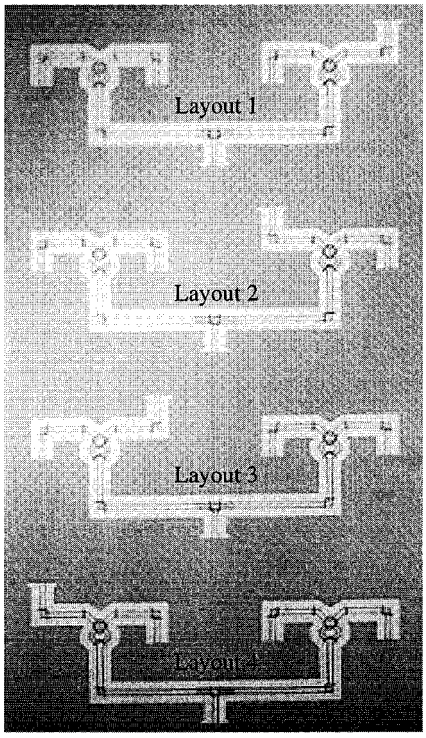
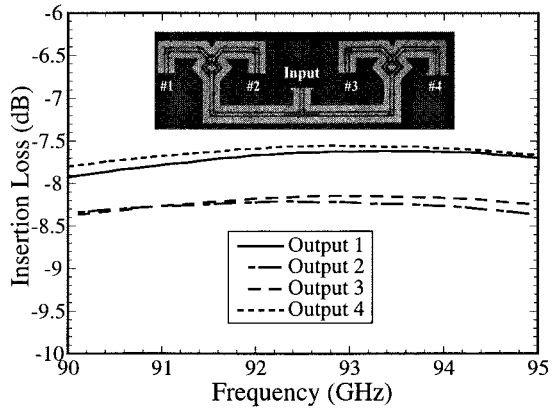
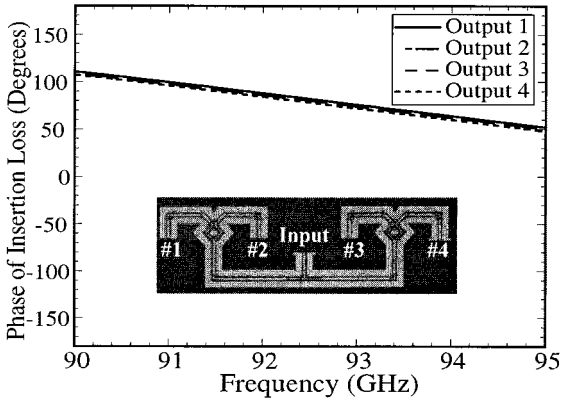


Fig. 13. Layout arrangements for the distribution networks.



(a)



(b)

Fig. 14. Insertion loss for four 1×4 distribution networks shown in insert. The loss for all four outputs varies by ± 0.5 dB and the phase varies by $\pm 2^{\circ}$. (a) Magnitude. (b) Phase.

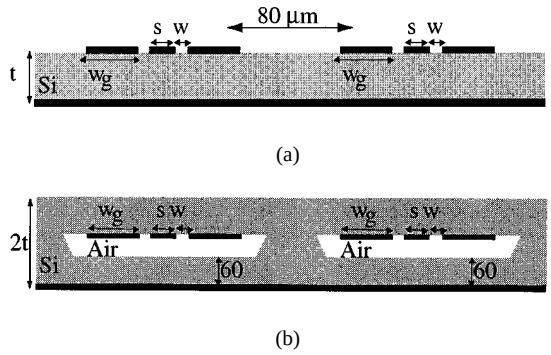


Fig. 15. Cross-sectional views for isolation measurements in two different line architectures. (a) Conductor-backed. (b) Cavity-backed packaged.

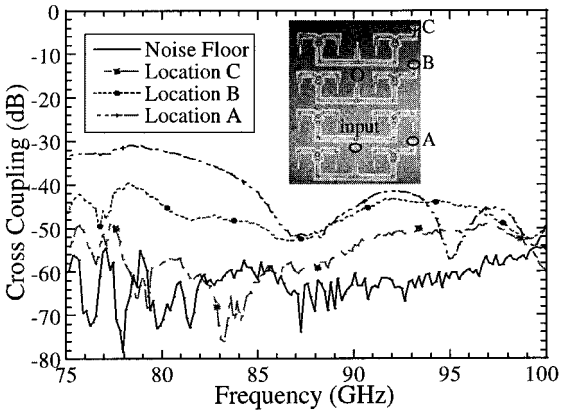


Fig. 16. Cross-coupling measurements of distribution networks with cavity-backed packaged architecture.

cavity-backed packaged distribution network exhibits a consistently excellent performance over the whole frequency range of interest. Representative results indicate an insertion loss of 1–1.4 dB above the nominal 6 dB (see Fig. 12).

In order to evenly distribute power to the 16 patch antennas, it is important that each of the four 1×4 networks have minimum amplitude and phase imbalance. To characterize this variation, four 1×4 distribution networks have been fabricated with three of the four output ports matched. That is, while the insertion loss of output 1 is being measured, outputs 2–4 are matched with 50-Ω terminations (see Fig. 14). Each output port has been measured in this manner and results indicate that the 1×4 dividers have 0.5-dB amplitude [see Fig. 14(a)] and a 2° phase imbalance [see Fig. 14(b)] from 90 to 95 GHz for conventional FGC.

To understand crosstalk effects in dense circuit topologies, cross coupling between four 1×4 distribution networks of Fig. 11 is measured using the arrangement shown in Fig. 15. In this circuit layout, all ports have been left open with the exception of the two ports connected to the probes of the on-wafer station. This way, due to the excited standing waves, on the interconnecting sections of the distribution networks, the measured coupling is higher than expected by 6 dB. S_{21} is measured between the input port O (see photo insert in Fig. 16), and the output ports at locations A, B, and C. Fig. 16 shows measurements of conductor-backed circuits [see Fig. 15(a)] and cavity-backed packaged circuits [see Fig. 15(b)]. The results confirm that the worst coupling between input port O and output port A in conventional FGC is always less than -30

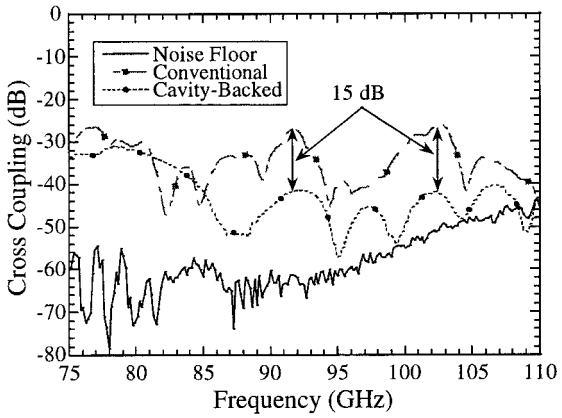


Fig. 17. Adjacent cross coupling for location A (80-μm ground-to-ground separation).

dB. With the use of conformal packaging in this dense circuit layout, the cross coupling is reduced by -15 dB to the noise level of the measurement equipment in the frequency range from 93 to 110 GHz.

To compare the coupling of conventional FGC circuits to a shielded arrangement, coupling between the input and location A has been measured for a conventional and cavity-backed distribution network. The measured crosstalk presented in Fig. 17 verifies that FGC lines have coupling effects that may be as low as -25 dB for conventional lines separated by as little as 80 μm.

IV. Summary and Conclusions

As indicated by the study presented in this paper, the presence of metal planes in a 3-D integrated circuit may cause the excitation of parasitic modes that result in unwanted resonances and increased losses. The presented results strongly demonstrate the capability to eliminate these parasitic effects by use of nonmetallized air cavities etched into the Si substrate. The use of nonmetallized cavities not only reduces parasitic loss and improves performance, but also improves isolation to levels very close to the noise of the measurement system. The presented micromachined technology realizes Wilkinson power dividers with insertion loss near 0.40 dB, and bends and tees with loss values of 0.1 and 0.2 dB, respectively. Finally, the 1×4 distribution network has demonstrated an insertion loss of about 1–1.4 dB near the design frequency, indicating an efficiency of 72%–80%. These results demonstrate the capability of this technology to provide superior integration in addition to excellent performance when compared to other conventional planar power-combining technologies.

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Rashaunda M. Henderson (S'91–M'99) received the B.S.E.E. degree from Tuskegee University Tuskegee, AL, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from The University of Michigan at Ann Arbor, in 1994 and 1999, respectively.

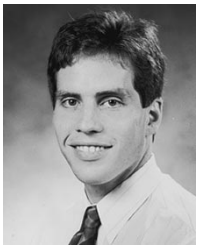
Her research involved developing and characterizing Si-based packages fabricated with standard integrated circuit (IC) and micromachining techniques for high-frequency applications. In February 1999, she joined the Materials and Structures Laboratories (a division within Digital DNA Laboratories), Motorola Semiconductor Product Sector, Tempe, AZ, where she is involved with characterization, simulation, and model development of on-chip and off-chip RF and microwave passive structures.

Dr. Henderson is a member of Eta Kappa Nu, the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the National Society of Black Engineers (NSBE), and the International Microelectronics and Packaging Society (IMAPS). She is treasurer of IEEE Waves and Devices Society, Phoenix Section.

Katherine J. Herrick (M'91) received B.S.E., M.S.E., and Ph.D. degrees from The University of Michigan at Ann Arbor, in 1993, 1995, and 2000, respectively, all in electrical engineering. Her doctoral work focused on integrated 3-D microwave circuits up to W-band utilizing silicon micromachining.

From January 1995 to December 1996, she was a NASA Graduate Fellow, where she was involved with electrooptic sampling and microwave circuits. She is currently conducting research as a Post-Doctoral Research Fellow in the areas of microelectromechanical systems (MEMS), filters, and multilayer silicon circuits at The University of Michigan at Ann Arbor.

Dr. Herrick received the First Place award at the Student Paper Competition at the 1997 IEEE International Microwave Theory and Techniques Society (IEEE MTT-S) Symposium. She also received the Third Place Award in the 2000 IEEE MTT-S Student Paper Competition.



Thomas M. Weller (S'85–M'86) received the B.S., M.S., and Ph.D. degrees in electrical engineering from The University of Michigan at Ann Arbor, in 1988, 1991, and 1995, respectively.

He is currently an Assistant Professor in the Electrical Engineering Department, University of South Florida, Tampa. He has authored or co-authored over 40 papers in his field. His research involves micromachining applications for microwave and millimeter-wave circuits, packaging, electromagnetic modeling, and millimeter-wave sensors.

Dr. Weller was the recipient of the 1996 Microwave Prize presented by the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).

S. V. Robertson received the B.S.E.E. degree from the University of Texas at Austin, in 1991, and the M.S.E. and Ph.D. degrees from The University of Michigan at Ann Arbor, in 1993 and 1997, respectively.

In 1991, he then joined the Radiation Laboratory, The University of Michigan at Ann Arbor, where he was involved with the application of silicon micromachining technology to millimeter-wave integrated circuits. He remained with the Radiation Laboratory until 1998, where he continued his involvement with novel millimeter-wave micromachined circuits and structures. In 1998, he joined the Wireless Technology Laboratory, Lucent Technologies, Whippany, NJ, where he is currently a member of the RF Technology Group.

R. T. Kihm received the B.S.E.E. degree from Case Western Reserve University, Cleveland, OH, in 1963, and the Ph.D. degree in electrophysics from the Polytechnic Institute of Brooklyn, Brooklyn, NY, in 1972.

In 1978, he joined the Raytheon Company (then Hughes Aircraft Company), El Segundo, CA, where he was involved with the design and development of MMW missile seekers, and is currently an Engineering Fellow with Electronic Systems, Microwave Center, involved with the development of a Ka-band imaging radar.

Linda P. B. Katehi (S'81–M'84–SM'89–F'95) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1977, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles, in 1981 and 1984 respectively.

In September 1984, she joined the faculty of the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, as an Assistant Professor, and then became an Associate Professor in 1989 and Professor in 1994. She has served in many administrative positions including, Director of Graduate Programs, College of Engineering (1995–1996), Elected Member of the College Executive Committee (1996–1998), Associate Dean for Graduate Education (1998–1999), and Associate Dean for Academic Affairs (since September 1999). She has authored or co-authored 410 papers published in referred journals and symposia proceedings and she holds four U.S. patents. She has also generated 20 Ph.D. students.

Dr. Katehi is a member of the Antennas and Propagation Society (IEEE AP-S), the IEEE Microwave Theory and Techniques Society (MTT-S), Sigma XI, Hybrid Microelectronics, and URSI Commission D. She was a member of the AP-S AdCom (1992–1995). She is an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION. She was the recipient of the 1984 IEEE IEEE AP-S W. P. King (Best Paper Award for a Young Engineer), the 1985 IEEE AP-S S. A. Schelkunoff Award (Best Paper Award), the 1987 National Science Foundation Presidential Young Investigator Award, the 1987 URSI Booker Award, the 1994 Humboldt Research Award, the 1994 University of Michigan Faculty Recognition Award, the 1996 IEEE IEEE MTT-S Microwave Prize, the 1997 International Microelectronics and Packaging Society (IMAPS) Best Paper Award, and the 2000 IEEE Third Millennium Medal.