Three-Dimensional High-Frequency Distribution Networks—Part I: Optimization of CPW Discontinuities

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Abstract—This paper describes a systematic study of coplanar waveguide discontinuities that are requisite components of high-frequency distribution networks. The specific geometries addressed are air bridges, right-angle bends, tee junctions, and Wilkinson dividers. Relative to typical monolithic-microwave integrated-circuit designs, the components studied herein are electrically large in order to minimize signal attenuation. The large size leads to pronounced parasitic effects, and the emphasis of this study was to optimize the electrical performance using simple compensation techniques. The optimization methods are developed using full-wave simulation and equivalent-circuit modeling, and are verified experimentally up to 60 GHz. Part II of this paper describes the implementation and packaging of the components to realize a three-dimensional W-band distribution network.

Index Terms—Coplanar transmission lines, microwave circuits, micromachining.

I. INTRODUCTION

BOTH THIS paper and [1] address the development of advanced high-frequency distribution networks for planar arrays operating at 94 GHz. The contributions of this paper relate to the simultaneous realization of low-loss and high-isolation channels, in a package with an extremely small footprint. Silicon micromachining is the enabling technology that was used to create the compact network architecture, which features a three-dimensional packaging configuration and multilayer interconnects. The use of multiple layers was also exploited in improving the inter-channel crosstalk and distortion performance. In order to minimize the distribution loss, finite-

ground coplanar-waveguide (CPW) geometries with cross sections approaching one-tenth of a guided wavelength were used. In this paper, design techniques for optimizing the performance of the CPW discontinuities that comprise the distribution network are described. The implementation and packaging of the components is presented then in [1].

This study on CPW discontinuities was motivated by the present shortage of mature equivalent-circuit models, such as are available for the microstrip line. Geometries such as stubs, bends, and tee junctions have been studied extensively using experimental and full-wave analysis methods, e.g., in [2]–[9]. However, while some studies have described equivalent-circuit model development (e.g., [10]–[14]), there have been few that focus on systematic design and optimization techniques. One reason for this is that CPW provides considerable design versatility in terms of line geometry (signal line, slot, and ground-plane width) and the size and location of often needed air bridges. As described in [1], micro-packaging techniques introduce additional electromagnetic effects that are also critical to the performance of the components.

Specifically addressed in this paper are methods for optimizing the performance of CPW air bridges, right-angle bends, tee junctions, and Wilkinson dividers. A common thread in each case is the compensation of excess capacitance introduced by air bridges, using sections of high-impedance line (step-compensation sections). Aside from packaging effects, it will be shown that the air-bridge capacitance can be considered as the dominant performance-limiting factor at millimeter-wave frequencies. This topic is discussed with respect to CPW 90° bends in [6], in which it is shown that the impact of air-bridge capacitance outweighs that of the parasitics inherent to the bend itself. By compensating for the excess capacitance, improvements in the return loss on the order of 15–20 dB can be achieved. The designs of the step-compensation sections are determined through a combination of analytical techniques, full-wave simulation, and equivalent-circuit modeling. The theoretical predictions are verified experimentally over the frequency range from 20 to 60 GHz, and for linewidths ($S + 2W$, see Fig. 1) of 130 and 260 μm.

The theoretical and experimental results presented in this paper are based on circuits supported on high-resistivity (>2000 Ω-cm) 450-μm-thick silicon wafers. Referring to Fig. 1, the line dimensions are either $S + 2W = 260$ μm and $W_g = 230$ μm or $S + 2W = 130$ μm and $W_g = 120$ μm. For the fabricated circuits, the gold traces were electroplated to a

Fig. 1.   CPW air bridge with step compensation.

Fig. 2.   Ratio of effective air-bridge capacitance to the parallel-plate approximation versus CPW aspect ratio. Curves are shown for three CPW 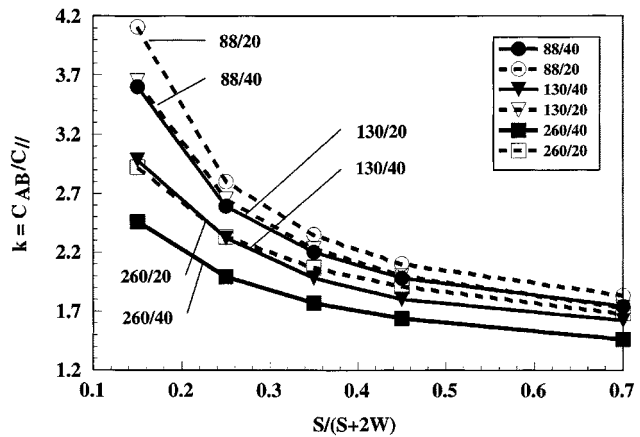linewidths ($S + 2W = 88, 130, 260, \mu$m) and two air-bridge widths (20, 40 μm). The air-bridge height is 3 μm.

thickness of 2.5 μm and the air-bridge height was 3 μm. The measurements were taken using a Wiltron 360B vector network analyzer (VNA), GGB 150-μm-pitch GSG probes, and a Jmicro probe station. Instrument calibration was performed using the National Institute of Standards (NIST) Multical thru-reflection line (TRL) software [15]. All full-wave simulations referenced within were performed using HP EESof's Momentum.

II. CPW AIR BRIDGES

An air bridge in CPW introduces a shunt capacitance to ground due to the coupling between the CPW center conductor and air-bridge span. Thus, while it is a widely used structure for equalizing CPW ground-plane potential, the air bridge will introduce parasitic effects that degrade circuit performance. The approach described herein for compensating for the excess capacitance is to introduce a short length of high-impedance line on either side of the air bridge, as illustrated in Fig. 1.

In order to derive a closed-form expression for determining the parameters of the step-compensation section, the excess capacitance presented by the air bridge must be known. In [16], selected microstrip crossover geometries were investigated, which present a parasitic capacitance similar to that of the CPW air bridge. It was found that the capacitance was around 1.5 times the value predicted by a simple parallel-plate approximation. (For a CPW configuration, the dimensions of the parallel plate are defined by the overlap of the center conductor width and the air-bridge width.) In order to investigate the CPW case thoroughly, a parametric study versus line geometry was performed using full-wave method-of-moments (MoM) simulations. From the full-wave results, the air-bridge capacitance was extracted via optimization (HP Series IV) using a simple equivalent circuit consisting of an ideal shunt capacitor. The CPW lines were uniform, i.e., no step-compensation sections were included, in order to simplify the extraction process.

The results of this study are summarized in Fig. 2, which shows the ratio (k) of effective air-bridge capacitance (C_{AB}) to the parallel-plate capacitance ($C_{\parallel}$) versus line aspect ratio. The modeling of the narrower lines ($S+2W = 88$ and $130\,\mu$m) was performed from 20 to 110 GHz and an excellent fit between the simple circuit model and the full-wave results was found. For the wider lines ($S + 2W = 260\,\mu$m), the modeling was performed from 20 to 60 GHz, again with an excellent match. As indicated in Fig. 2, the ratio decreases as the aspect ratio, or center conductor width, increases since the fringing capacitance becomes a lesser contributor to the overall capacitance value.

The same trend holds versus air-bridge width, with the value for k being consistently larger for the 20-μm-wide air bridges than for the 40-μm-wide geometries. As a point of reference, an aspect ratio of approximately 0.45 produces a 50-Ω line on silicon (in the absence of an air bridge), and the k value in this case is around 1.8.

As mentioned above, the required compensation for the air-bridge capacitance can be realized by reducing the width of the CPW line beneath the air bridge (Fig. 1). In [3], this technique was considered from the viewpoint of increasing the effective characteristic impedance of the line, in order to offset the decrease in Z_o affected by the air bridge. A limitation of this perspective is that a localized narrowing of the center conductor may not provide enough compensation. The alternative approach taken here is to use the lumped-capacitor equivalent-circuit model and add a section of high-impedance line on either side. Using ideal transmission-line theory, the following equation is derived for the length of the high-Z line that yields an impedance match

$$L_{\text{ideal}} = \frac{c}{\sqrt{\epsilon_{re}}} \frac{Z_h Z_o^2 C_{AB}}{Z_h^2 - Z_o^2} \qquad (1)$$

where Z_o is the nominal CPW impedance outside the step section, Z_h is the impedance in the high-Z section, C_{AB} is the air-bridge capacitance, c is the speed of light, and ϵ_{re} is the effective dielectric constant in the high-Z section. Equation (1) is valid assuming

$$\tan\left(\frac{\theta}{2}\right) \approx \frac{\theta}{2}$$
$$Z_h \omega C_{AB} \left(\frac{\theta}{2}\right) \ll 1 \qquad (2)$$

where θ is the electrical length of the step-compensation section. The choice of Z_h affects L_{ideal} directly through (1) and indirectly through its effect on C_{AB}.

The expression for L_{ideal}, being derived from ideal transmission-line theory, is based only on the air-bridge capacitance and does not account for its physical size. From the full-wave simulation results and related circuit optimization, it was found that
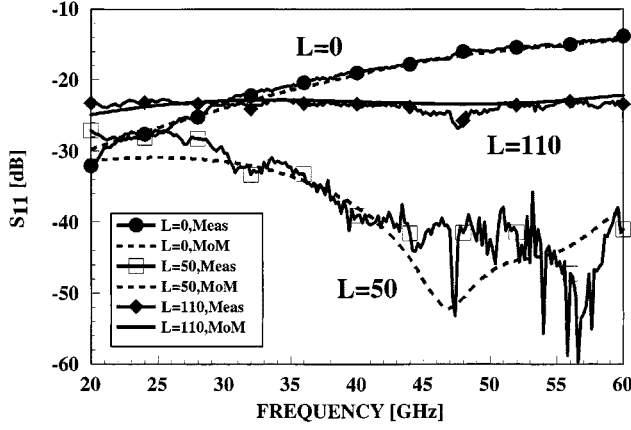
Fig. 3. Measured and simulated (MoM) S_{11} for air-bridge geometries with varying step-compensation lengths (in micrometers μm). The CPW linewidth is $S + 2W = 260$ μm and the air-bridge width is 40 μm.

Fig. 4. CPW right-angle bend with step compensation.

Fig. 5. Equivalent circuit used to model the CPW right-angle bend.

by treating the air bridge as a lumped capacitance, the effective reference planes lie within the physical boundaries of the air bridge. On average, the distance from the outer edges of the air bridge to the reference planes occupies 70% of the air-bridge width. In order to correct for this effect and define the step-compensation length as an extension beyond the air-bridge boundary (as indicated in Fig. 1), the following equation is used:

$$L = L_{\text{ideal}} - 0.7W_{\text{AB}} \tag{3}$$

where W_{AB} is the air-bridge width.

A comparison between full-wave simulation results and measured data, for linewidths $(S + 2W)$ of 260 μm and air-bridge widths of 40 μm, is given in Fig. 3. The curves labeled $L = 0$ correspond to a geometry with no step compensation; in this case, the line aspect ratio is 0.45 and the effective air-bridge capacitance is around 23 fF. The sets of curves labeled $L = 50$ and 110 correspond to geometries using high-Z sections with a characteristic impedance of 80 Ω. The aspect ratio in the step sections is 0.15, leading to an air-bridge capacitance of approximately 11 fF. As the effective dielectric constant is around 6.2, the predicted optimum step length from (3) is 42 μm (using a Z_o of 50 Ω). This value is verified by the results in Fig. 3, which indicate an improvement in the return loss of more than 20 dB for the $L = 50$ design, at frequencies above 40 GHz. The standing wave effect seen in Fig. 3 is partially a result of the characteristic impedance of the feed lines being 2 Ω higher than the 50-Ω reference impedance used to generate the results. The impedance of the fabricated circuits was higher than anticipated because the oxide layer present between the silicon substrate and the CPW metal was not initially taken into account.

Full-wave simulation results for linewidths of 130 μm and air-bridge widths of 40 μm were generated to examine the effects of air bridges on narrower lines. In comparison to the 260-μm-wide lines, the air-bridge capacitance is smaller, resulting in less degradation in the return loss. Still, relative to the noncompensated geometry, an improvement in the return loss of greater than 10 dB is obtained above 45 GHz using the step-compensation predicted from (3).
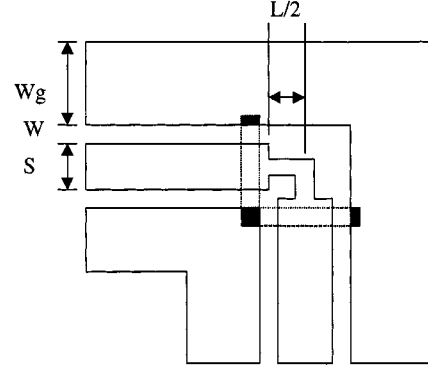
III. CPW 90° BENDS

An approach based on step compensation was also developed to improve the millimeter-wave performance of 90° CPW bends. The use of air bridges to suppress the excitation of the coupled slot-line mode in laterally asymmetric geometries such as a bend is a common practice [4], [5]. However, the combined effects of the bend and air-bridge parasitics can lead to extremely poor return loss; as will be shown, the return loss is less than 10 dB at 50 GHz for a CPW linewidth of 260 μm if no compensation is used. In [7], a method to improve the bend performance is described, which involves chamfering the outside corner of the signal conductor. A design methodology is not presented, however, as the focus is placed on optimization using full-wave analysis. Another alternative to improving the performance of a bend is to introduce dielectric overlays at the interior corner [17], but this approach is not suitable for monolithic-microwave integrated-circuit (MMIC) applications.

A step-compensated right-angle bend and the equivalent circuit used for modeling purposes are illustrated in Figs. 4 and 5, respectively. The capacitors C_{AB} represent the effective air-bridge capacitance, while the transmission line is a simple approximation to the CPW line extending between the two air bridges. Using transmission-line theory, it is found that the length of the transmission line that minimizes the reflection coefficient is given by

$$L = \frac{c}{\sqrt{\epsilon_{re}}} \frac{2Z_h Z_o^2 C_{\text{AB}}}{Z_h^2 - Z_o^2} \tag{4}$$

where the variables are the same as those described above for (3) and the same assumptions are taken as stated in (2). This equation also assumes that the high-Z step-compensation section is uniform and extends up to the edge of each air bridge, and it does not account for parasitics, which are inherent to the bend itself.
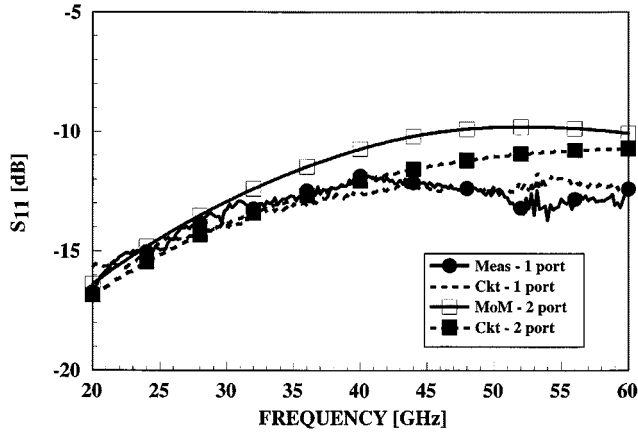
Fig. 6. S_{11} for a right-angle CPW bend with an input linewidth of $S + 2W = 260 \, \mu$m and no step compensation. The curves include measured one-port data, the optimized one-port equivalent-circuit model, the two-port version of the equivalent-circuit model, and simulated (MoM) results for the two-port version.

Fig. 7. S_{11} for a right-angle CPW bend with an input linewidth of $S + 2W = 260 \, \mu$m and a step-compensation length of 220 μm. The curves include measured one-port data, the optimized one-port equivalent-circuit model, the two-port version of the equivalent-circuit model, and simulated (MoM) results for the two-port version.

Experimental verification of the theoretical predictions was performed by fitting an equivalent-circuit model to measured data, and then comparing the model to full-wave simulation results. This approach was taken because two-port measurements of a bend require the use of a VNA calibration technique such as short-open-load-reciprocal (SOLR) thru, which allows a calibration to be performed with the microwave probes positioned in an orthogonal orientation. In this paper, only the TRL calibration method was used and, thus, a direct two-port comparison to full-wave results was not possible.

As an example of the comparison approach, the reflection coefficient of a 260-μm-wide bend with 40-μm-wide air bridges and no step compensation is shown in Fig. 6. The curve labeled Meas-1 Port is the measured response of a single bend that is terminated in a thin-film resistive load. The curve labeled Ckt-1 Port is the response of the optimized equivalent circuit, which has the same topology as that given in Fig. 5, but is terminated using measured data for the resistive load. The only free variable in the circuit model was the capacitance used to represent the air bridges, all other parameters corresponding directly to the physical geometry. As the optimized value for this capacitance was higher than the predicted value (30 versus 23 fF), it was concluded that simplifications in the model, e.g., ignoring bend-related parasitics, were taken up in this parameter. The curve labeled Ckt-2 Port corresponds to the optimized equivalent-circuit model with the resistive load data removed from the output port. As seen in this figure, the two-port circuit model compares to within 1.5 dB of the two-port full-wave analysis results.

Similar results for the same bend, modified with a step-compensation section, are given in Fig. 7. The optimum length for the high-Z section, as calculated from (4), is 247 μm (assuming $Z_h = 80 \, \Omega$ and $C_{AB} = 20$ fF), whereas the fabricated circuit had a step length of 220 μm. The two-port equivalent-circuit model and the full-wave simulation results differ by approximately 5 dB near the low end of the band, but show close agreement overall. In order to keep a consistent circuit model, the only change made with respect to the optimized model for the no-compensation case (Fig. 6) was to increase the characteristic impedance of the line between the air bridges from 50 to 80 Ω.
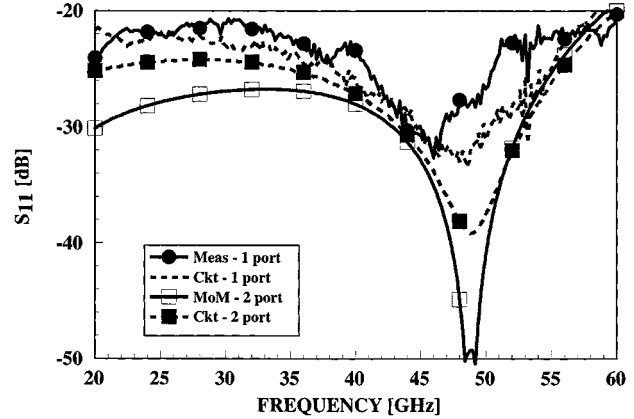

Fig. 8. S_{11} for a right-angle CPW bend with an input linewidth of $S + 2W = 130 \, \mu$m and no step compensation. The curves include measured one-port data, the optimized one-port equivalent-circuit model, the two-port version of the equivalent-circuit model, and simulated (MoM) results for the two-port version.
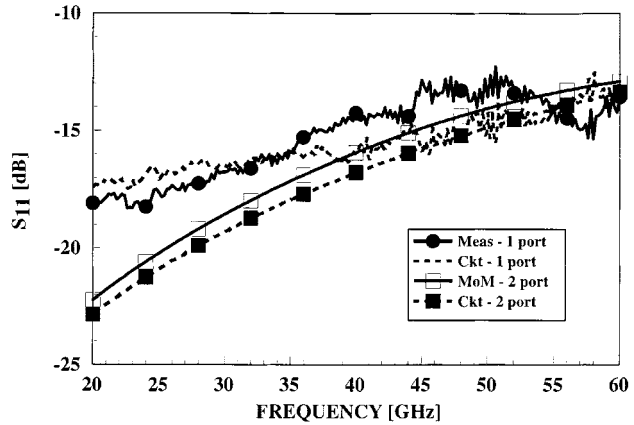
The results demonstrate that the step compensation provides an improvement of 10–15 dB above 40 GHz. Full-wave simulations on several bend geometries verified that the optimum taper length was between 240–280 μm.

The performance of right-angle bends in 130-μm-wide lines, also using 40-μm-wide air bridges, is shown in Figs. 8 (uncompensated) and 9 (compensated). For the uncompensated design, the circuit model and full-wave simulation results agree to within 1 dB over the frequency band. As with the wider line comparison described above, the optimized value for the air-bridge capacitance was higher than the predicted value (15 versus 12 fF). With the compensated design, the circuit model was modified only to reflect a change in the characteristic impedance of the high-Z section, and the resulting two-port version agreed with the full-wave simulation results to within 4 dB; this version of the circuit model corresponds to the curve labeled Ckt-2 port (a). The sensitivity of the model to the high-Z line length is indicated by the curve labeled Ckt-2 port (b), which corresponds to a circuit model in which the length was increased by 20 μm. A comparison between Figs. 8 and 10
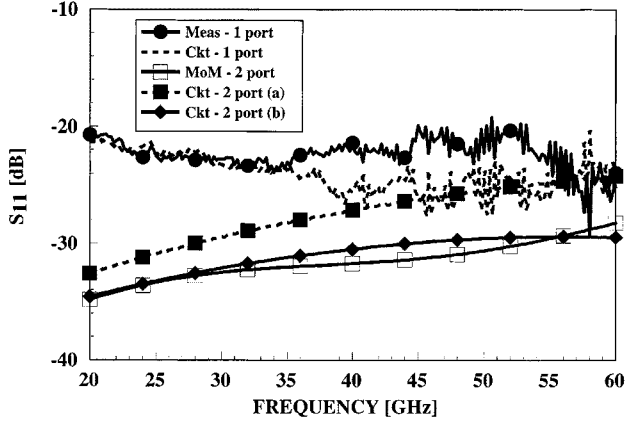
Fig. 9. S_{11} for a right-angle CPW bend with an input linewidth of $S + 2W = 130$ μm and a step-compensation length of 120 μm. The curves include measured one-port data, the optimized one-port equivalent circuit model, the two-port version of the equivalent-circuit model, and simulated (MoM) results for the two-port version with: (a) 120-μm and (b) 140-μm step lengths.
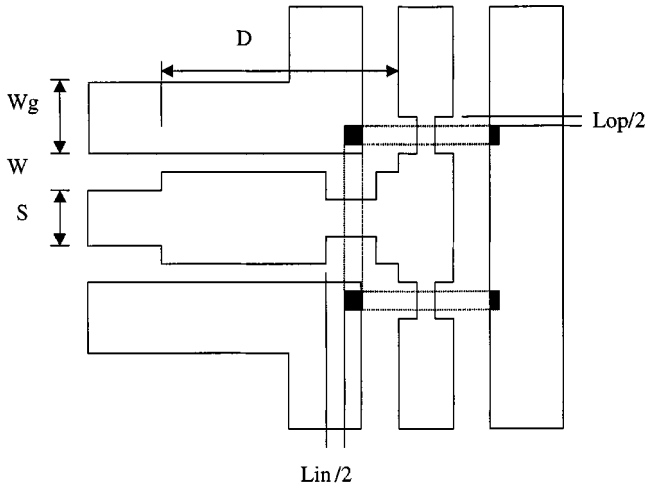

Fig. 10. CPW tee junction with a quarter-wave impedance transformer at port 1.

indicates that the compensation provides an improvement in the return loss of approximately 15 dB above 40 GHz.

IV. CPW TEE JUNCTIONS

An illustration of a generalized CPW tee junction is given in Fig. 10. In this configuration, a quarter-wavelength impedance transformer is included at the input (on the left-hand side of this figure) in order to obtain an impedance match with an equal impedance presented at all three ports. The figure also indicates a possible means of introducing step compensation at each of the air-bridge locations [18]. Although not addressed herein, this approach for compensation could be used in conjunction with alternative ground-equalization methods, such as the one described in [8] and [9].

The parasitic effects of the tee junction can be studied using the equivalent-circuit model shown in Fig. 11. As an example, a full-wave simulation was performed on a geometry comprised of 260-μm-wide lines, with 40-μm-wide air bridges and no step compensation. The reference impedance at each port was 50 Ω
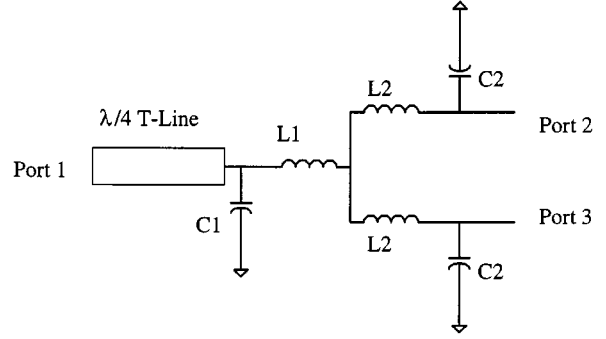

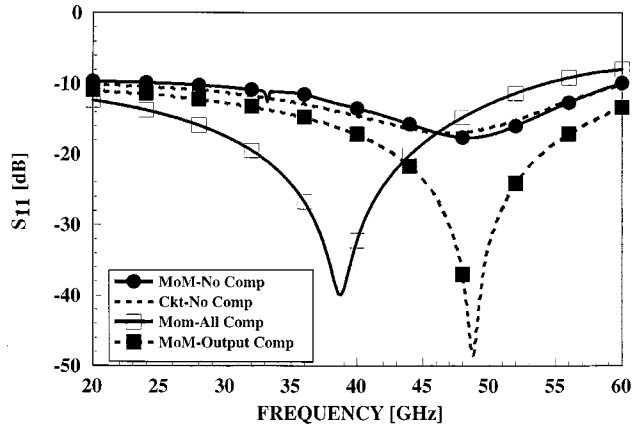Fig. 11. Equivalent circuit used to model the CPW tee junction.

Fig. 12. S_{11} for CPW tee junctions with linewidths of $S + 2W = 260$ μm. The curves include simulated (MoM) and equivalent-circuit results for a geometry with no step compensation, as well as simulated results for geometries with compensation on all air bridges and on just the output air bridges (at ports 2 and 3).

and the $\lambda_g/4$ section was 35 Ω (aspect ratio of 0.78). The optimized equivalent-circuit model, in which only the lumped elements were allowed to vary, provided an excellent match to the full-wave simulation results for all S-parameters; a comparison of S_{11} is shown in Fig. 12. The resulting circuit model parameters show that the effective input capacitance (C_1) is close to the predicted air-bridge capacitance (29 versus 31 fF). However, the output capacitance (C_2) is significantly higher than that due to the air bridge alone (40 versus 23 fF) indicating that fringing capacitance associated with the tee junction itself is taken up in the C_2 parameter.

The circuit model can be used to determine the impact of introducing step compensation to modify the capacitance *due to the air bridges*. As shown by the full-wave simulation results in Fig. 12, steps at the output air bridges improve the return loss by 10–15 dB in the 45–50-GHz band without shifting the center frequency, whereas the response shifts down in frequency when the input air bridge is also compensated (all step lengths were 20 μm, as defined in Fig. 10). These effects were predicted accurately using the equivalent-circuit model. The theoretical predictions were also verified experimentally, as shown in Fig. 13. In this figure, the full-wave simulation results were terminated at the output ports using measured data for the resistive load, to replicate the measurement conditions. The characteristics of compensated tee junctions developed
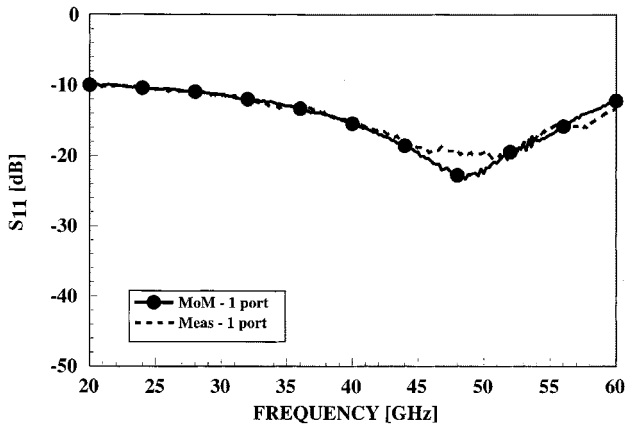
Fig. 13.   Measured and simulated (MoM) S_{11} for a one-port version of the CPW tee junction with linewidths of $S+2W = 260\,\mu$m and step compensation on the output air bridges. The three-port simulation data was terminated at ports 2 and 3 with measured data for the load.
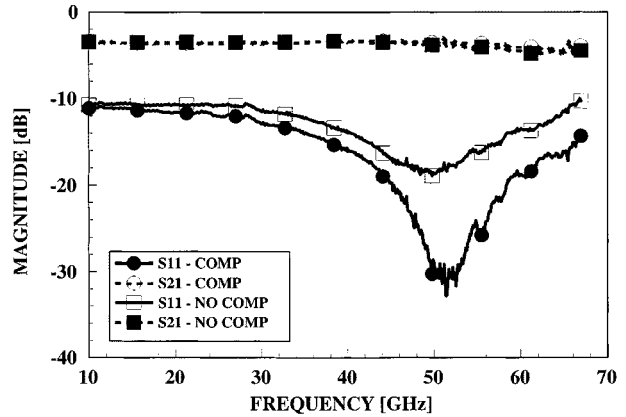

Fig. 15.   Measured S_{11} and S_{21} for an ACPS Wilkinson divider with and without the air-bridge compensation indicated in Fig. 14.
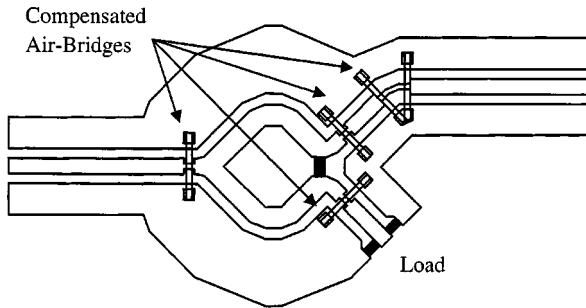

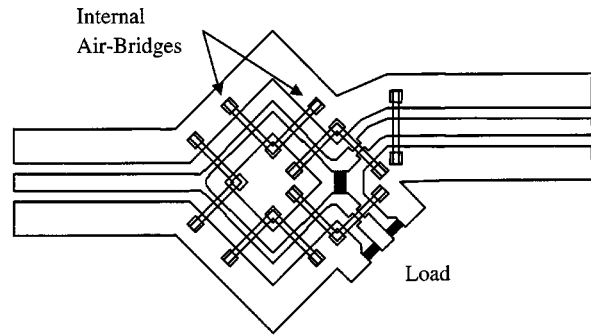Fig. 14.   ACPS Wilkinson divider with output port (3) terminated.

Fig. 16.   CPW Wilkinson divider with output port (3) terminated.

around 130-μm-wide lines proved to be essentially the same as those of the wider lines.

V. WILKINSON POWER DIVIDERS

As demonstrated for the right-angle bend and tee-junction geometries, compensation of air-bridge capacitance is also an important factor in the design of Wilkinson dividers. In this paper, both CPW and asymmetric coplanar strip (ACPS) configurations were examined, as potential candidates for the 94-GHz distribution network described in [1]. An advantage of the ACPS approach [19] is that higher characteristic impedances can be realized compared to CPW. An ACPS Wilkinson design also requires fewer air bridges than a CPW design. While previous authors have presented millimeter-wave Wilkinson dividers (e.g., [20], [21]), this is the first paper to address the aspect of air-bridge compensation.

An ACPS divider, designed to operate in the 45–50-GHz range, is illustrated in Fig. 14. The input/output CPW feedlines are 130-μm wide, while in the ACPS lines, the strip width is 80 μm, the slot width is 40 μm, and the ground width is 250 μm. The divider requires three air bridges, and two additional air bridges are used at the 45° bend at the output port 2.

The measured S_{11} and S_{21} for the ACPS configuration, with and without air-bridge compensation, are given in Fig. 15. In

Fig. 17.   Measured S_{11} and S_{21} for a CPW Wilkinson divider, with and without the internal air bridges indicated in Fig. 16.

each case, the insertion loss is approximately 3.4 dB. However, the return loss is improved by as much as 14 dB when the short high-Z sections are integrated around each air-bridge location. Another noticeable effect was that the minimum in S_{22} was 20 GHz below the S_{11} minimum in the uncompensated circuit (see [22]). It can be verified using circuit-level modeling that this results from excess capacitance at the input and output ports of the divider.

A CPW Wilkinson divider is shown in Fig. 16. This design has 130-μm-wide CPW lines at the input and output ports, and in the divider section itself. As illustrated in this figure, air bridges are required along the quarter-wavelength 70-Ω lines; at a minimum, air bridges must be used at each end of the divider, but might also be placed at the 90° bends in the center. The step-compensation method is difficult to implement for all these air bridges, however, since the highest characteristic impedance that can be practically realized is around 80 Ω. Referring to (3) or (4), the difference between Z_h and Z_o is only 10 Ω, leading to step-compensation line lengths that cannot be accommodated within the boundaries of the divider.

A solution to the step-compensation problem is to remove the air bridges from the internal 90° bends of the CPW divider. As shown in Fig. 17, the return loss for a divider, which includes all the air bridges, even when compensated to the extent possible, is only 15 dB. The removal of the internal air bridges results in a 13-dB improvement in the return loss without affecting the insertion loss. A similar improvement in S_{22} as described for the ACPS design was also observed.

VI. SUMMARY

This paper has presented high-frequency design techniques for several CPW geometries that are printed on high-resistivity silicon. The theoretical and experimental results demonstrate that the methods are effective for lines with electrically large cross sections, i.e., approaching 0.1 λ_g. The use of lines with wide cross sections is necessary to maximize the efficiency of monolithic distribution networks, which may be several wavelengths long.

The dominant parasitic effect in the geometries that were studied is the shunt capacitance presented by air bridges. On a 50-Ω line with a cross section $(S+2W)$ of 260 μm, an air bridge with typical dimensions will introduce approximately 23 fF of capacitance, which translates into a $-j140\ \Omega$ shunt reactance at 50 GHz. By properly compensating for this reactance, the return loss from CPW geometries such as air bridges, right-angle bends, tee junctions, and Wilkinson dividers can be improved by 15–20 dB. Without this level of improvement, the cumulative effect of input mismatch at the various elements comprising a complex distribution network will easily diminish the advantages gained by the use of large linewidth geometries.

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