Optimization of Distributed MEMS Transmission-Line Phase Shifters—U-Band and W-Band Designs

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***Abstract*—The design and optimization of distributed micromechanical system (MEMS) transmission-line phase shifters at both U- and W-band is presented in this paper. The phase shifters are fabricated on 500-μm quartz with a center conductor thickness of 8000 Å of gold. The U-band design results in 70°/dB at 40 GHz and 90°/dB at 60 GHz with a 17% change in the MEMS bridge capacitance. The W-band design results in 70°/dB from 75 to 110 GHz with a 15% change in the MEMS bridge capacitance. The W-band phase-shifter performance is limited by the series resistance of the MEMS bridge, which is estimated to be 0.15 Ω. Calculations demonstrate that the performance of the distributed MEMS phase shifter can be greatly increased if the change in the MEMS bridge capacitance can be increased to 30% or 50%. To our knowledge, these results present the best published performance at 60 and 75–110 GHz of any nonwaveguide-based phase shifter.**

***Index Terms*—MEMS, microwave, millimeter-wave, phase shifter, true-time delay.**

I. Introduction

THE development of electronically variable phase shifters has been driven primarily by their usefulness in phased-array radars, although they are now used in a wide range of systems including communications and measurement instrumentation [1]. Most phase shifters currently being used can be divided into either ferrite phase shifters or semiconductor device phase shifters [2]–[4]. Semiconductor-device-based phase shifters have been used up to 100 GHz with switching times well under 1 μs [5]. These devices are either hybrid or monolithic with switching powers on the order of milliwatts. The hybrid devices (p-i-n or varactor diodes) can handle up to 1 kW of RF power at microwave frequencies (1–10 GHz), however, the monolithic devices can only handle RF power on the order of milliwatts to 1 W [1].

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There are many different designs for the semiconductor-device-based phase shifters. Some of the more prominent designs are switched-line phase shifters [6], loaded-line phase shifters [7], [8], branch-line phase shifters [9], [10], and high-pass/low-pass phase shifters [11]. The switched-line phase shifter is a true-time delay (TTD) device with the bandwidth limited by the high-frequency operation of the switches. Typical figures-of-merit for the semiconductor-device-based phase shifters are 144°/dB at 1 GHz [11], 211°/dB at 12 GHz [12], 86°/dB from 16 to 18 GHz [10], 60°/dB at 60 GHz [9], and 41°/dB at 94 GHz [5]. Also, Goldsmith *et al.* have shown 3- and 4-bit switched line phase shifters using microelectromechanical system (MEMS) switches with 279°/dB at 10 GHz and 138°/dB at 35 GHz [13].

Recently, another type of true-time-delay phase shifter, known as the distributed phase shifter, has been investigated by Nagra *et al.* [14], [15] using GaAs Schottky diodes. This phase shifter is very similar to the distributed MEMS transmission line (DMTL), but uses varactor diodes rather than MEMS bridges for the variable capacitance. The distributed Schottky-diode phase shifters have shown good performance with 86°/dB insertion loss at 20 GHz, or 4.2-dB insertion loss for 360° phase shift and are capable of faster switching times than the MEMS-based phase shifters. However, the millimeter-wave performance of these devices is limited by the series resistance of the diodes, which is typically 2–6 Ω.

II. Basics of Periodically Loaded Lines

Distributed circuits have been used in many devices including filters [16], traveling-wave amplifiers [17], phase shifters [15], and nonlinear transmission lines [17]. The concept is very useful because the parasitics of the discrete components, such as the gate-to-source capacitance of transistors in traveling-wave amplifiers or the capacitance of Schottky diodes in nonlinear transmission lines are included as part of the periodic transmission line, thereby resulting in very wide-band operation. The transmission-line dimensions can also be designed such that the resulting periodic transmission line will have a 50-Ω characteristic impedance.

The DMTL consists of a high-impedance line (>50 Ω) capacitively loaded by the periodic placement of MEMS bridges

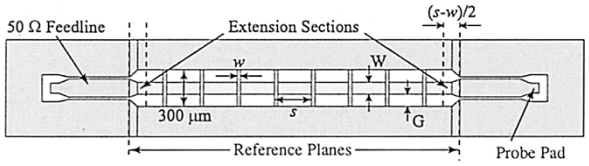

Fig. 1. Layout of a DMTL constructed of a CPW line with center conductor width W and total CPW width $W + 2G$, and MEMS bridges with width w and spacing s. The DMTL is connected to 50-Ω feed lines and probe pads for testing.

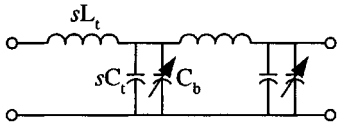

Fig. 2. Lumped-element transmission-line model of the DMTL assuming the MEMS bridge can be represented by a capacitor C_b. L_t and C_t are the per unit length inductance and capacitance, respectively, of the unloaded transmission line, and s is the spacing between the MEMS bridges.

[18]. This can be done with many different types of transmission lines, however, it is most easily implemented using coplanar waveguide (CPW) transmission lines. Fig. 1 shows the top view of a typical DMTL used in this paper. The MEMS bridges have a width w, a length $l = W + 2G$, and a thickness t. The periodic spacing between the bridges, i.e., s, and the number of bridges vary depending upon the application. The DMTL is connected to probe pads via 50-Ω CPW feed lines for the purpose of testing.

A. Bragg Frequency

A result of creating a periodic structure is the existence of a cutoff frequency or Bragg frequency f_B near the point where the guided wavelength approaches the periodic spacing of the discrete components [19]. In many of the distributed circuits mentioned, this cutoff frequency can be designed such that it will not limit the device performance since the discrete components will have a comparable maximum frequency [17]. However, in the case of the DMTLs, the self-resonant frequency of the MEMS bridges is around 200 GHz [20] and, thus, the operation is limited by the Bragg frequency of the line.

For the DMTL, the MEMS bridge can be modeled as a shunt capacitor, resulting in a loaded-line model, as shown in Fig. 2. Using this model, the resulting characteristic impedance is given by [17]

$$Z_l = \sqrt{\frac{sL_t}{sC_t + C_b}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \tag{1}$$

where ω_B is the Bragg frequency and is given by

$$\omega_B = \frac{2}{\sqrt{sL_t(sC_t + C_b)}}. \tag{2}$$

It can be seen that well below the Bragg frequency, the impedance of the line is given by $\sqrt{L/C}$, where $L = sL_t$ and $C = sC_t + C_b$.

The MEMS bridge cannot be entirely modeled by a single capacitor due to the presence of some inductance and resistance in the bridge. In the circuit modeling of measured DMTLs, it has been found that the inductance is large enough to have a noticeable effect on the device performance, while the effect of the resistance is almost negligible.

TABLE I
BRAGG FREQUENCY CALCULATIONS FROM (2) AND (5)

L_b (pH)	f_B (GHz)
0	137.9
10	123.3
20	111.9
30	102.9

$Z_o = 100\ \Omega$, $\epsilon_{eff} = 2.5$, $s = 200\ \mu$m, $C_b = 40$ fF.

When an inductance L_b is included in series with the bridge capacitance, the shunt admittance is

$$Y_p = j\omega sC_t + \frac{j\omega C_b}{1 - \omega^2 L_b C_b} \tag{3}$$

and the equation for the characteristic impedance becomes

$$Z_l = \sqrt{\frac{sL_t}{sC_t + \dfrac{C_b}{1 - \omega^2 L_b C_b}}} \cdot \sqrt{1 - \frac{\omega^2 s^2 L_t C_t}{4} - \frac{\omega^2 s L_t C_b}{4(1 - \omega^2 L_b C_b)}}. \tag{4}$$

Setting this equation to zero and solving for ω, the resulting Bragg frequency is found to be

$$\omega_B = \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}}, \qquad a = s^2 L_t C_t L_b C_b$$
$$b = s^2 L_t C_t + s L_t C_b + 4 L_b C_b, \qquad c = 4 \tag{5}$$

For most of the DMTLs designed in this paper, the inductance in the bridge has been found to be 10–30 pH based on curve fitting a circuit model to measured data. Table I shows the calculated Bragg frequencies versus several values of bridge inductance for a line with an unloaded impedance Z_o of 100 Ω, an unloaded effective dielectric constant of 2.5, a periodic spacing of 200 μm, and a bridge capacitance of 40 fF. As can be seen, including the series inductance of the bridge has a significant effect on the position of the Bragg frequency.

B. Phase Velocity

The phase velocity of the loaded line can be determined by assuming a lossless line and using the model in Fig. 2 [17]

$$v = \frac{s}{\sqrt{sL_t(sC_t + C_b)}\left(1 + \dfrac{\omega^2}{6\omega_B^2} + \cdots\right)} \tag{6}$$

where τ is the time delay *per section*. At frequencies well below the Bragg frequency, the phase velocity can be approximated as $s/\sqrt{LC}$. From (6), it is seen that by varying the MEMS bridge

capacitance C_b, the phase velocity of the transmission line can be varied resulting in a variable delay line or TTD phase shifter.

C. Line Loss

When a transmission line is loaded such that the impedance is changed, the loss of the line is also changed due to a change in the amount of current on the line for the same amount of power. The transmission loss can be included in the model of the DMTL (Fig. 2) by including a resistance R_s in series with the line inductance sL_t. The effect of a series resistance in the bridge can also be taken into account by placing a resistor R_b in series with the bridge capacitance. Combining this loss with the transmission-line loss, the total loss *per section* for a distributed transmission line is [17]

$$\alpha = \frac{R_s}{2Z_l} + \frac{R_b Z_l C_b^2 \omega^2}{2} \tag{7}$$

where Z_l is the *loaded* line impedance. For a line with an unloaded impedance of 100 Ω, an unloaded effective dielectric constant of 2.5, a periodic spacing of 200 μm, a bridge capacitance of 40 fF, a loss of 0.6 dB/cm at 20 GHz for the unloaded line ($R_s = 0.28\ \Omega$/period), and a MEMS bridge resistance of 0.1 Ω at 30 GHz, the loss from the transmission line is 1.6 and 2.5 dB/cm at 30 and 60 GHz, respectively, while the loss from the MEMS bridge resistance is 0.05 and 0.28 dB/cm at 30 and 60 GHz. Thus, for these typical CPW parameters on quartz, the loss is dominated by the transmission-line loss. In addition, as the effective dielectric constant is increased, the transmission line will dominate even more due to the higher loss of the transmission line, which results from the reduced dimensions.

Although the analytic model provides a good general understanding of distributed lines, it is not accurate at frequencies approaching the Bragg frequency. The model begins to break down due to approximating the transmission-line sections as lumped elements. However, it has been shown that a very accurate model can be obtained using a circuit simulator (such as HP EESof's Libra[1]) where the line is modeled using transmission-line segments instead of lumped elements [18].

III. Design and Optimization of a U-Band DMTL Phase Shifter

A. Design

The design of a DMTL phase shifter requires the specification of the bandwidth or Bragg frequency, substrate or dielectric constant, unloaded impedance, and loaded impedance. From these specifications, the zero-bias bridge capacitance C_{bo} and spacing s can be determined from (1) and (2) and are given by

$$s = \frac{Z_{lu}}{\pi f_B \sqrt{L_t(C_r L_t - (C_r - 1)C_t Z_{lu}^2)}} \tag{8}$$

$$C_{bo} = s\left(\frac{L_t}{Z_{lu}^2} - C_t\right) \tag{9}$$

[1]HP EES of Communications Design Suite v6.0, Hewlett–Packard Company, Santa Clara, CA, 1995.

where, in (2), the bridge capacitance and inductance have been set to $C_b = C_r \cdot C_{bo}$ and $L_b = 0$, respectively, Z_{lu} is the DMTL characteristic impedance for the low capacitance state, and C_r is the ratio of maximum to minimum (or zero-bias) bridge capacitance. The per unit length inductance and capacitance L_t and C_t are given by [16]

$$C_t = \frac{\sqrt{\epsilon_{r,\text{eff}}}}{cZ_o} \quad \text{and} \quad L_t = C_t Z_o^2 \tag{10}$$

in which $\epsilon_{r,\text{eff}}$ is the effective dielectric constant of the unloaded transmission line and c is the free-space velocity. For the case where the DMTL is constructed using a CPW line, Z_o and $\epsilon_{r,\text{eff}}$ can be related to the physical CPW line parameters by a conformal mapping [21]

$$Z_o = \frac{\eta_o K(k')}{4\sqrt{\epsilon_{r,\text{eff}}} \cdot K(k)} \tag{11}$$

$$\begin{aligned} \epsilon_{r,\text{eff}} &= \frac{\epsilon_r + 1}{2} \\ k &= W/S \\ k' &= \sqrt{1 - k^2} \end{aligned} \tag{12}$$

where W and S are the center conductor width and total width of the CPW line, respectively, η_o is the free-space impedance, and $K(k)$ is the complete elliptic integral of the first kind. Using these equations, the DMTL phase shifter can be designed to a set of specifications. This initial design is then simulated using the Libra circuit model given in [18]. The Libra circuit model does include the MEMS bridge inductance and will result in a more accurate value of the Bragg frequency from which the design can be fine tuned, using iterative methods, to the desired specifications.

B. Optimization

The optimization method used in this section is based on the work of Rodwell *et al.* [22], [17], which presented the analysis of loss in distributed nonlinear CPW lines. The distributed line analysis was significantly extended to optimize for best phase shift by Nagra *et al.* [15]. In this paper, we apply an optimization method similar to Nagra to the case of MEMS bridges to obtain the maximum amount of phase shift for the minimum amount of insertion loss in distributed MEMS phase shifters. In order to carry out this optimization, analytic expressions for both the phase shift per unit length and the insertion loss per unit length must be found. In addition, a set of design constraints must be specified, which, for this optimization, are listed in Table II. The substrate is chosen to be quartz ($\epsilon_r = 3.8$) due to its low-loss properties at microwave frequencies. The Bragg frequency in Table II is set to 120 GHz in order to limit the return loss to -10 dB up to 60 GHz [18], while the capacitance ratio was determined to be 1.2 from previous DMTL measurements. The optimization analysis is carried out with the total width of the CPW, i.e., S, chosen to be approximately $\lambda_d/8$ at the maximum operating frequency of 60 GHz. The loaded line impedance Z_{lu} is chosen to be 48 Ω in order to maximize the effect that a change in the MEMS bridge capacitance has on the transmission-line

TABLE II
DMTL PHASE-SHIFTER SPECIFICATIONS

ϵ_r	3.8
Z_{lu}	48 Ω
f_B	120 GHz
C_r	1.2

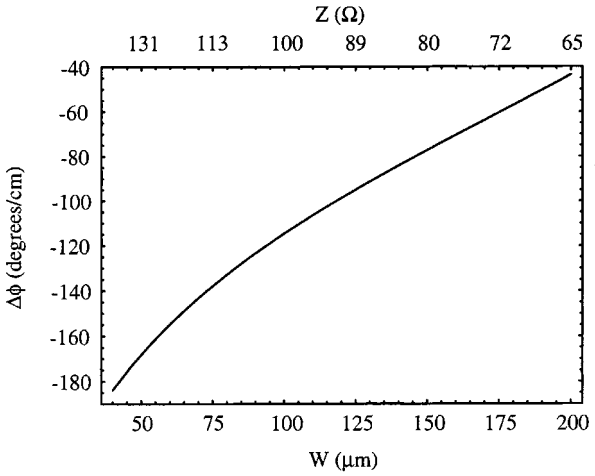

Fig. 3. Calculated phase shift per centimeter versus the CPW center conductor width at 40 GHz for a loaded line impedance of 48 Ω, a Bragg frequency of 120 GHz, and a total CPW linewidth of 300 μm.

velocity while maintaining a −10 dB or better return loss (see Section III-B.1).

1) Phase Shift: The phase shift per unit length is found from the change in the phase constant given by

$$\Delta\phi = \beta_1 - \beta_2 \quad = \omega\left(\frac{1}{v_1} - \frac{1}{v_2}\right). \tag{13}$$

Using the capacitance ratio C_r and (6) for the phase velocity, the phase shift is found to be

$$\begin{aligned}\Delta\phi &= \omega\sqrt{L_t C_t}\left(\sqrt{1+\frac{C_{bo}}{sC_t}} - \sqrt{1+\frac{C_r C_{bo}}{sC_t}}\right)\\ &= \frac{\omega Z_o\sqrt{\epsilon_{r,\text{eff}}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right)\text{rad/m}\end{aligned} \tag{14}$$

where Z_{lu} and Z_{ld} are the DMTL characteristic impedances for the low and high bridge capacitance states, respectively. Using this equation and (8)–(12), the phase shift per centimeter versus the center conductor width is calculated for DMTLs at 40 GHz for the specifications listed in Table II. As can be seen in Fig. 3, the phase shift is much larger for narrow center conductor widths (high impedance). This is due to the larger loading capacitance per unit length C_{bo}/s needed to load the line to 48 Ω and, therefore, the change in bridge capacitance (from C_{bo} to $1.2 \cdot C_{bo}$) has a larger effect on the phase velocity.

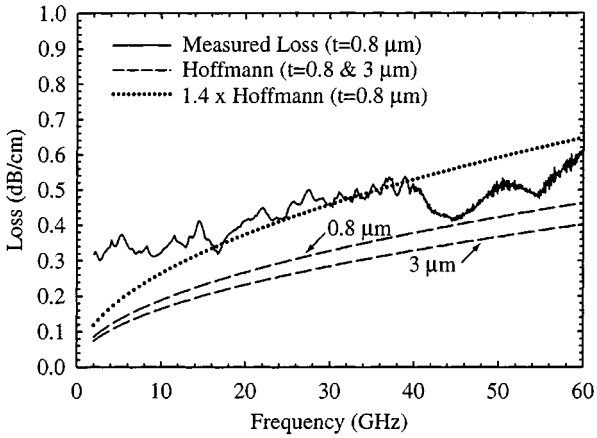

Fig. 4. Measured and calculated loss versus frequency for a 300-μm total width unloaded CPW line on quartz with a 100-μm-wide center conductor ($Z_o = 100\ \Omega$).

2) Loss: The transmission-line loss for the unloaded CPW line is found from a conformal mapping technique, and is given by Hoffmann [21]

$$\begin{aligned}\alpha = &\frac{8.686\cdot 10^{-2} R_s\sqrt{\epsilon_{r,eff}}}{4\eta_o S K(k)K(k')(1-k^2)}\\ &\cdot\left[\frac{2S}{W}\left\{\pi + \ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right\}\right.\\ &\left.+2\left\{\pi + \ln\left(\frac{4\pi S(1-k)}{t(1+k)}\right)\right\}\right]\text{dB/cm}\end{aligned} \tag{15}$$

where t is the metal thickness, R_s is the surface resistance given by $R_s = \sqrt{\pi f \mu_o/\sigma}$, and σ is the conductivity of the metal. It should be noted that this equation significantly underestimates the measured loss of the CPW line on quartz. Fig. 4 shows the measured loss (from a thru-reflection line (TRL) calibration) and calculated loss versus frequency for a 300-μm total width CPW line on quartz with a 100-μm-wide center conductor ($Z_o = 100\ \Omega$). The CPW line is 8000 Å of gold with a conductivity of approximately $3.3 \cdot 10^{-7}$ S/m. Significantly less loss can be obtained, particularly at low frequencies, if a 3-μm-thick center conductor is used.

The line loss calculated from (15) is for a metal thickness of 0.8 μm which, at 40 GHz, is 1.8 skin depths. However, according to (15) and Fig. 4, if the metal thickness is increased to 3 μm, the loss would decrease by a factor of 1.15 *independent* of frequency. This is known to be incorrect since the loss depends on the skin depth, and once the metal thickness reaches several skin depths, it will cease to decrease with increased thickness. Thus, (15) should not be used to predict the loss performance of the line, but more as a guide to predict the *trend of loss* versus center conductor width.

As can be seen, the equation from Hoffmann must be increased by a factor of 1.4, in this case, in order to match the measured results. Notice that above 40 GHz, the unloaded CPW line is starting to radiate and this results in an adverse effect on the calibration standards and loss estimation using the TRL technique.

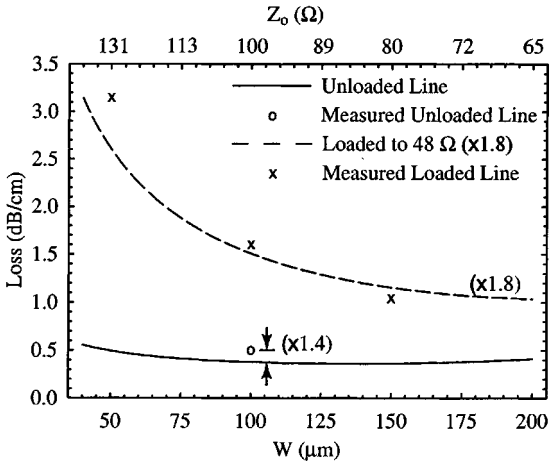

Fig. 5. Unloaded (—) and loaded (- - -) line loss at 40 GHz. The calculated loaded line loss has been increased by a factor of 1.8, which fits the measured loss best. The impedances for the labeled widths are included for reference.

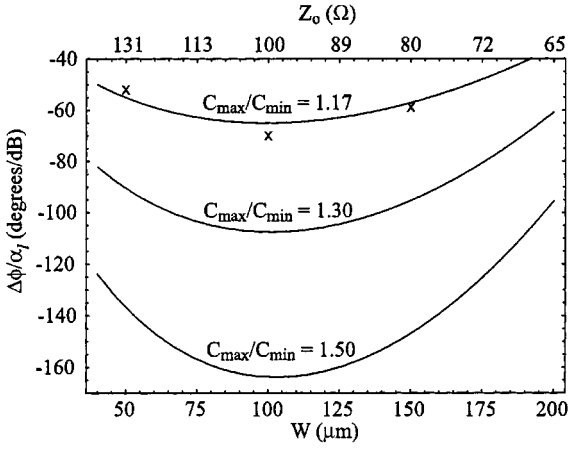

Fig. 6. Calculated phase shift per decibel loss at 40 GHz with capacitance ratios of 1.17, 1.3, and 1.5. Measured data points (x) are included for CPW center conductor widths of 50, 100, and 150 μm.

The loaded line loss is calculated by multiplying α by the ratio of the unloaded impedance Z_o to the loaded impedance Z_l given in (1). The loaded impedance in the high capacitance state Z_{ld} is used since this gives the maximum loss due to the fact that it is the lowest impedance state. There is not a large change in the line loss between Z_{lu} and Z_{ld} since the line impedance is only changing by 3–4 Ω for a MEMS capacitance ratio of $C_r = 1.2$. If the capacitance ratio is increased to 1.5, then the impedance change is 7–8 Ω. In this case, the DMTL, which starts at a loaded impedance of 48 Ω at 0-V bias, will change to a loaded impedance of 40–41 Ω when bias is applied to the MEMS bridge. This results in a -13- to -14-dB reflection loss, which is still within the design constraint of -10 dB. However, it may be desirable to reduce the reflection loss by changing the zero-bias loaded impedance to 52 Ω so that the 7–8-Ω impedance change will not adversely effect the phase-shifter performance.

Fig. 5 shows the calculated loaded and unloaded loss at 40 GHz, as well as the measured data points for three lines with different unloaded line impedances (131, 100, 80 Ω). The measured *unloaded* line loss is approximately a factor of 1.4 higher than the loss calculated from (15), as seen in Fig. 4. However, as seen in Fig. 5, the calculated *loaded* line loss, using the same factor of 1.4, does not match the measured *loaded* line loss. Instead, a factor of 1.8 matches the measured results. The difference could be due to additional loading effects, such as a change in the current distribution on the transmission line, which are not accounted for in the formulation of the loaded line loss.

3) Optimization: The optimal center conductor width (and unloaded impedance) is found by dividing the phase shift per centimeter (shown in Fig. 3) by the loaded line loss per centimeter (shown in Fig. 5) to find the phase shift per decibel loss. The result is plotted in Fig. 6, from which it is seen that the optimal center conductor width is 100 μm.

C. Experiment

In order to verify the position of the optimal center conductor width, three DMTL designs, with the specifications listed in Table II, were fabricated on quartz with center conductor widths of 50, 100, and 150 μm ($Z_u = 131, 100, 80\ \Omega$). Using the design equations (8)–(12), the bridge capacitances and spacings for the three cases are calculated and are shown in Table III. When using the design equations, the bridge inductance is first neglected. However, in order to account for its effect, the Bragg frequency, with $L_b = 0$, is set to 140 GHz rather than the specified value of 120 GHz, and (8) is used to calculate the spacing s. The Bragg frequency is then calculated using (5) and including a bridge inductance of 20 pH. As can be seen in Table III, the Bragg frequency is close to 120 GHz for all three cases. A constant bridge inductance is used, regardless of the bridge width, due to the fact that the bridge inductance is a weak function of the bridge width [20]. The bridge height for these designs is 1.2 μm and the bridge widths are determined using the static-field solver Maxwell 3D, with the results given in Table III. It should also be mentioned that Muldavin *et al.* have shown that the bridge resistance does not vary much with bridge width and, thus, a constant bridge resistance of 0.15 Ω at 30 GHz is used for all three cases in Table III [20].

TABLE III
DIMENSIONS OF THE DMTLS USED TO VERIFY THE OPTIMIZATION. THE BRAGG FREQUENCY IS CALCULATED USING $L_b = 20$ pH. $R_b = 0.15\ \Omega$ AT 30 GHz

$W(\mu\text{m})$	50	100	150
$Z_u(\Omega)$	131	100	80
C_{bo}(fF)	37.9	33.8	28.6
$s(\mu\text{m})$	150	197	249
$w(\mu\text{m})$	80	35	17
f_B(GHz)	119	122	127

Fig. 6 shows the calculated phase shift per decibel loss for capacitance ratios of 1.17, 1.3, and 1.5 at 40 GHz. The results of the measured DMTLs, with a capacitance ratio of 1.17, agree

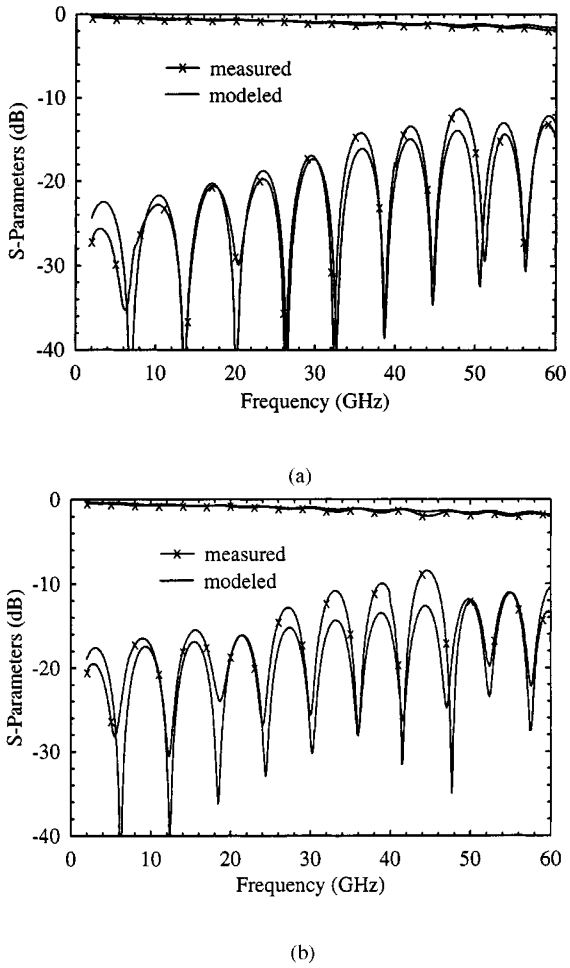

Fig. 7. Measured and modeled S-parameters of the $W = 100$ μm DMTL with 38 bridges (total length $= 7.6$ mm) at: (a) 0 V and (b) a maximum applied bias of 13 V.

well with calculations, and the phase shift per decibels for the optimal line ($W = 100$ μm) is measured to be -70°/dB at 40 GHz. The calculated phase shift per decibel loss, based on the *measured* CPW line loss, for capacitance ratios of 1.3 and 1.5, show that the performance of the DMTL can be increased to -108°/dB and -164°/dB, respectively, which is the equivalent of 3.3- and 2.2-dB insertion loss for 360° phase shift at 40 GHz.

Fig. 7 shows the measured and modeled S-parameters, at 0 V and the MEMS bridge maximum bias voltage of 13 V, for the optimal DMTL phase shifter with a 100-μm center conductor. The parameters used in the circuit model are listed in Table IV where A is the unloaded CPW line loss at 20 GHz and varies with frequency as $\sqrt{f}$. As can be seen, the zero-bias bridge capacitance C_{bo} is very close to the designed value of 33.8 fF and the return loss rises up to -10 dB at 60 GHz, when the maximum bias is applied, as desired. The discrepancies between the measured and modeled data seen in the return loss are most likely due to small variations in the bridge height among the 38 bridges used in this DMTL.

The measured and modeled phase shift are shown in Fig. 8 with excellent agreement between the two data. The maximum measured phase shift is 148° at 60 GHz, which corresponds to a time delay of 6.8 ps. Dividing the measured phase shift by

TABLE IV
CIRCUIT MODEL PARAMETERS FOR THE OPTIMAL DMTL ($W = 100$ μm)

C_{bo}(0 V) (fF)	34.6
C_{bo}(13 V) (fF)	40.6
L_b (pH)	11
A @ 20 GHz (dB/cm)	0.46
Z_{lu} (Ω)	47
Z_{ld} (Ω)	45

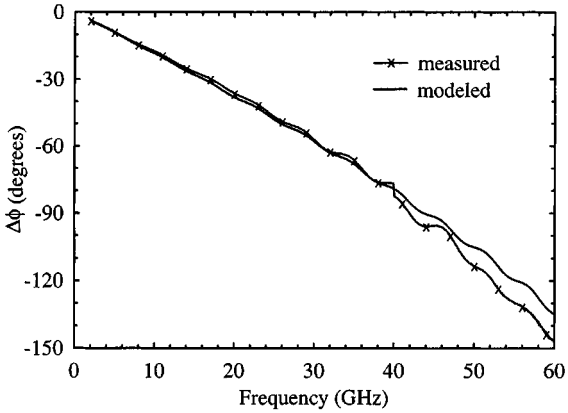

Fig. 8. Measured and modeled phase shift of the $W = 100$ μm DMTL at 13 V.

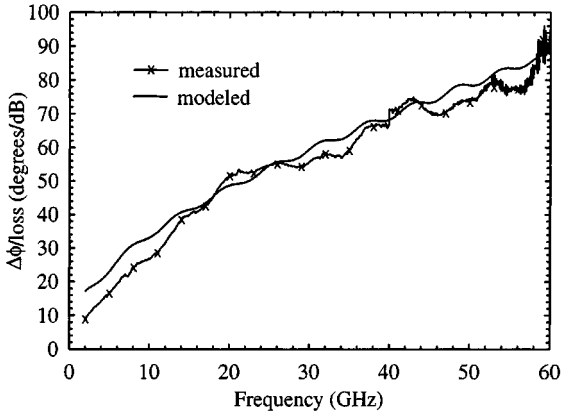

Fig. 9. Measured and modeled phase shift per decibel loss for the $W = 100$ μm DMTL showing 90°/dB at 60 GHz or 4 dB loss for 360° phase shift.

the measured insertion loss, with the reflection loss removed, results in Fig. 9, where the modeled data is again shown to be in good agreement with measurement. It is seen that 70°/dB at 40 GHz and 90°/dB at 60 GHz are achieved with this line. Thus, this DMTL is capable of giving 360° phase shift at 40 GHz with 5.1-dB loss and at 60 GHz with 4.0-dB loss.

The phase shift per decibel increases with frequency as $\sqrt{f}$, which is in agreement with theory since the loss increases as

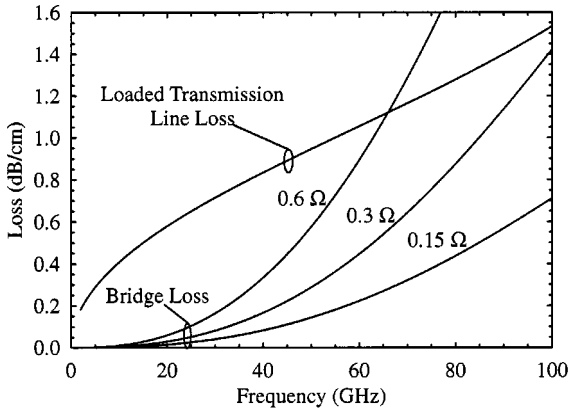

Fig. 10. Loaded transmission-line loss and loss due to bridge resistance versus frequency. The line loss is calculated from Hoffmann's equation for a 300-μm total width CPW line with a 100-μm-width center conductor ($f_B = 180$ GHz, $s = 110$ μm, and $C_b = 20.7$ fF).

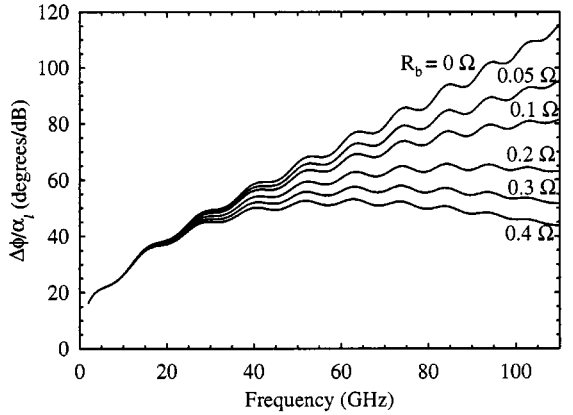

Fig. 11. Phase shift per decibel loss calculated from a Libra circuit simulation of a 32-bridge DMTL on quartz with a capacitance ratio of 1.17 and different bridge resistances specified at 30 GHz and varying as $\sqrt{f}$.

$\sqrt{f}$ and the phase shift increases as f. However, this only holds true as long as the loss due to the bridge resistance remains small compared to the transmission-line loss. The U-band phase shifter was designed to operate up to 60 GHz ($S = 300$ μm, $W = 100$ μm, $t = 8000$ Å, $f_B = 120$ GHz) and, therefore, at 10 or 20 GHz, does not give optimal phase-shifter performance. If the DMTL is redesigned to operate up to 20 GHz, a much higher phase shift per decibel loss could be achieved at 10–20 GHz since the design would dictate a wider CPW total width and a much thicker metal, resulting in a reduced unloaded line loss. Also, the capacitive loading would be increased such that the Bragg frequency would be 40 GHz rather than 120 GHz as it is for the 60-GHz design.

IV. Optimized W-Band DMTL Phase Shifter

The design procedure for a W-band phase shifter is identical to that given in the previous section; however, there are some additional effects that must be taken into consideration at higher frequencies. One such effect is loss due to the bridge resistance, which becomes significant at W-band frequencies (Figs. 10 and 11). This loss is shown in Fig. 10 for bridge resistances of 0.15, 0.3, and 0.6 Ω (specified at 30 GHz and increasing with frequency as $\sqrt{f}$). The calculation is for a 300-μm total width CPW line with a 100-μm center conductor width ($Z_o = 100$ Ω) loaded to 48 Ω and a Bragg frequency of 180 GHz. The loaded line loss is derived using Hoffmann's equations for the unloaded line loss multiplied by 100 Ω/48 Ω (notice that the 1.4 or 1.8 correction factor is not used here). It is seen that the distributed phase shifter is line-loss limited up to 100 GHz for MEMS bridge resistances of 0.15 and 0.3 Ω, whereas for a 0.6-Ω resistance, the bridge loss starts to dominate above 65 GHz. In Fig. 11, a Libra circuit simulation has been carried out for a 32-bridge DMTL with an unloaded impedance of 96 Ω, an effective dielectric constant of 2.37, a loaded impedance of 48 Ω, a capacitance ratio of 1.17, and different bridge resistances R_b specified at 30 GHz and varying as $\sqrt{f}$. It is seen that as the bridge resistance increases, the phase shift per decibel loss starts to level off and can even decrease with frequency for the higher resistances. The phase shift per decibel loss drops from 115°/dB at 110 GHz for no bridge resistance, to 52°/dB for a 0.3-Ω bridge resistance.

TABLE V
Calculated Design of an Optimized W-Band DMTL Phase Shifter on Quartz

$W(\mu\text{m})$	100
$S(\mu\text{m})$	300
C_{bo}(fF)	19
$s(\mu\text{m})$	110
f_B(GHz)	192
($L_b = 20$ pH)	

Using (8)–(12), a DMTL on quartz is designed for operation up to 100 GHz with a total CPW width of 300 μm and a zero-bias loaded impedance of 48 Ω. The resulting values for C_{bo} and s are given in Table V where the effect of neglecting the bridge inductance has been offset by increasing the Bragg frequency used in (8) to 250 GHz. As seen in Table V, the calculated Bragg frequency [using (5)] with a 20-pH bridge inductance is 192 GHz. Using the static-field solver Maxwell 3D, a bridge width of 25 μm at a height of 1.5 μm is found to give a bridge capacitance of 20.7 fF, and this value is used in the measured circuit (with $f_B = 186$ GHz), as seen in Table VI.

The W-band DMTL is measured using an HP8510C for 2–40 GHz and an HP8510C with W-band millimeter-wave test set for 75–110 GHz calibrated using on-wafer TRL standards. The measured and modeled results of a 48-bridge DMTL are shown in Fig. 12 with the circuit model parameters listed in Table VII. The S-parameters are shown for 0 V and the maximum applied bias of 26 V, and show very good agreement with the design. The pull-down voltage of this line is just over 26 V with a corresponding capacitance ratio of 1.15. This capacitance ratio is lower than previously observed and is believed to be due to higher levels of compressive stress within the bridges and increased nonuniformity across the wafer. This

TABLE VI
DIMENSIONS FOR THE OPTIMIZED W-BAND DMTL PHASE SHIFTER

$W(\mu\text{m})$	100
$S(\mu\text{m})$	300
$C_{bo}(\text{fF})$	20.7
$s(\mu\text{m})$	110
$w(\mu\text{m})$	25
$f_B(\text{GHz})$ ($L_b = 20$ pH)	186

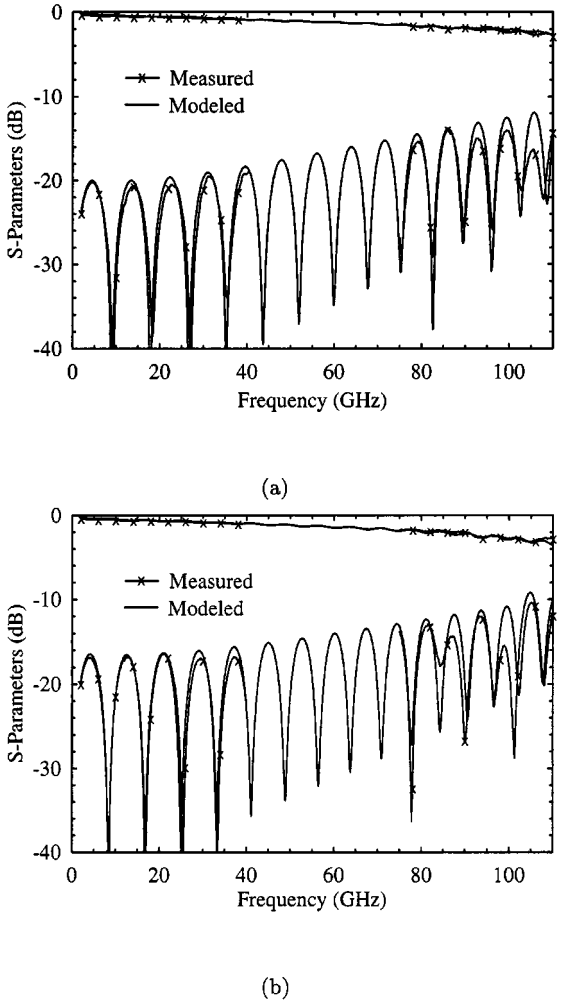

Fig. 12. Measured (2–40 and 75–110 GHz) and modeled S-parameters at: (a) 0-V bias and (b) a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table VI and the circuit parameters are listed in Table VII.

also explains why the pull-down voltage is twice as large for only a 25% increase in the bridge height from 1.2 to 1.5 μm. The measured phase shift per decibel loss is found by dividing the measured phase shift (Fig. 13) by the insertion loss and is shown in Fig. 14. As can be seen, there is a fairly constant level

TABLE VII
CIRCUIT MODEL PARAMETERS FOR THE W-BAND DMTL PHASE SHIFTER

C_{bo}(0 V) (fF)	20.7
C_{bo}(26 V) (fF)	23.7
L_b (pH)	22
A @ 20 GHz (dB/cm)	0.5
R_b @ 30 GHz (Ω)	0.15

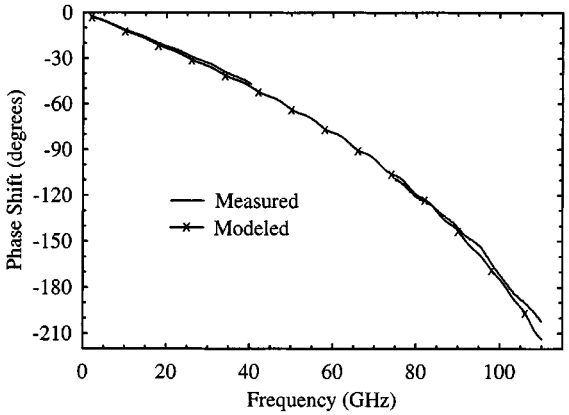

Fig. 13. Measured and modeled phase shift of the W-band DMTL at 26 V.

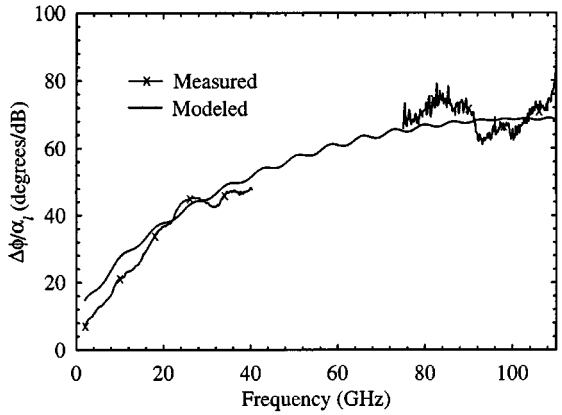

Fig. 14. Measured and modeled phase shift per decibel loss at a maximum bias of 26 V for a W-band DMTL phase shifter. The dimensions are listed in Table VI and the circuit parameters are listed in Table VII.

of nearly 70°/dB from 75 to 110 GHz, or 5-dB loss for 360° phase shift at W-band. The modeled data shows good agreement using a bridge resistance of 0.15 Ω at 30 GHz, which scales as $\sqrt{f}$.

Fig. 15 shows the calculated phase shift per decibel loss for capacitance ratios of 1.15, 1.3, and 1.5 at 100 GHz and a bridge resistance of 0.15 Ω at 30 GHz. The calculated unloaded-line loss from (15) is increased by a factor of $1.8\times(Z_{ld}/Z_o)$ in order for the calculated results to match measurements, as discussed in Section III-B.2. The result of the measured DMTL, with a

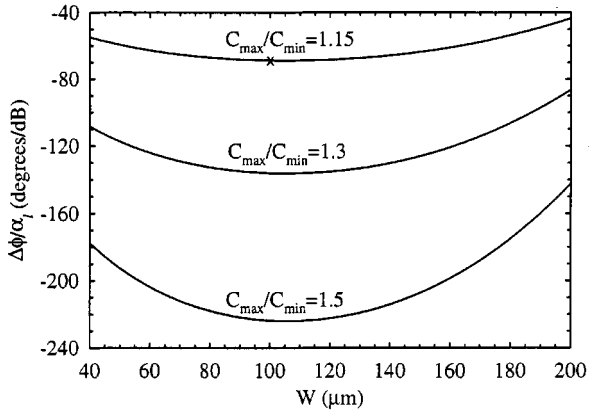

Fig. 15. Calculated phase shift per decibel loss at 100 GHz with a capacitance ratio of 1.15, 1.3, and 1.5. The measured data point is shown for a center conductor width of 100 μm.

capacitance ratio of 1.15, is in agreement with the adjusted calculated value. The calculated phase shift per decibel loss for a MEMS capacitance ratio of 1.3 and 1.5 show that the performance of the W-band DMTL can be increased to $-136°$/dB and $-224°$/dB, respectively, which is the equivalent of 2.6- and 1.6-dB insertion loss for 360° phase shift at 100 GHz.

V. Conclusion

This paper has presented the design and optimization of distributed CPW-based MEMS transmission-line phase shifters. An analytic model is used to find the optimum design for a given set of specifications. Optimized U- and W-band phase shifters were designed, fabricated, and tested at The University of Michigan at Ann Arbor. The U-band design results in 70°/dB at 40 GHz and 90°/dB at 60 GHz with a change in the loading capacitance of only 17% (and a center conductor thickness of only 8000 Å of gold). The W-band design results in 70°/dB from 75 to 110 GHz with a change in the loading capacitance of only 15%. The series resistance of the MEMS bridge was estimated to be 0.15 Ω at 30 GHz based on the W-band measurements, and limited the performance of the phase shifter above 80 GHz.

In addition, it has been shown that the performance of the distributed MEMS phase shifter can be greatly increased if the change in the MEMS bridge capacitance can be increased to 30% or 50%. This can be achieved by abandoning the analog control and using the MEMS bridge capacitance in the up or down state. Normally, this would yield a very large capacitance ratio ($\sim$20–80), which would cause a large change in the loaded impedance. However, if the MEMS bridge capacitance is placed in series with a fixed metal–insulator–metal capacitor, then the resulting capacitance ratio can be limited to 1.5–2. This research is currently being done at The University of Michigan at Ann Arbor [23], [24].

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