High-Power Time-Domain Measurement System with Active Harmonic Load–Pull for High-Efficiency Base-Station Amplifier Design

Johannes Benedikt, Roberto Gaddi, Paul J. Tasker, and Martin Goss

***Abstract*—A measurement system combining vector corrected waveform measurements with active harmonic load–pull extends, for the first time, real-time experimental waveform engineering up to the 30-W power level. The vector correction procedure is presented in this paper. A novel harmonic load–pull approach based on the real-time measurement capability of the system is demonstrated on a 4-W LDMOS device. A 20% increase in maximum output power to 4.7 W without degrading gain and efficiency is realized. Waveform analysis at various drive and load conditions directly identifies nonlinear capacitance effects being a key design issue for the design of highly efficient power amplifier.**

***Index Terms*—Active load–pull, calibration, microwave measurements, microwave power amplifier, modeling, MOSFETs, nonlinearities, time-domain measurements.**

I. Introduction

AT THE present time, a key design challenge is the realization of high-efficiency and high-power amplifiers for the next generation of mobile communication base stations. It is the theoretical analysis of terminal voltage and current waveforms that provides a clear understanding of amplifier modes of operation required for high efficiency, linearity, and power [1], [2]. Hence, the experimental measurement and analysis of waveforms including RF load lines should be the method of choice when optimizing (tuning) amplifier performance. High-power measurement systems used for characterizing devices generally do not provide this information. However, in the last decade, time-domain measurement systems have emerged [3], [4]. Initially, these time-domain measurement systems were used to provide experimental insight into active devices' nonlinear behavior [5]. More recently, their integration with harmonic tuning at the input and output has shown how large-signal device/circuit interactions can be experimentally investigated [6]. However, the power capabilities of such systems have thus far been inadequate to the requirements of the emerging telecommunication market.

In this paper, we illustrate a measurement system that overcomes these limitations, allowing both vector-corrected time-domain waveform measurements and active harmonic load–pull at power levels up to 30 W. The vector-correction technique implemented for absolute power and relative phase measurements of the signal harmonics is presented. Real-time waveform engineering on a commercially available packaged 4-W LDMOS transistor is performed to demonstrate how the combination of harmonic load–pull with waveform measurements is most advantageous during real-world device performance optimization (tuning) with respect to power and efficiency. Furthermore, through the analysis of the waveforms the nonlinear capacitance effects are identified to be a key design issue, which has to be addressed to further improve the performance of a power amplifier, based on LDMOS devices.

Manuscript received March 6, 2000; revised August 25, 2000. This work was supported by a Grant from Nokia Networks.

J. Benedikt, R. Gaddi, and P. J. Tasker are with the School of Engineering, Cardiff University, Cardiff CF24 3TF, U.K. (e-mail: benedikt@cf.ac.uk).

M. Goss is with Nokia Networks, Camberley GU15 3BW, U.K.

Publisher Item Identifier S 0018-9480(00)10737-9.

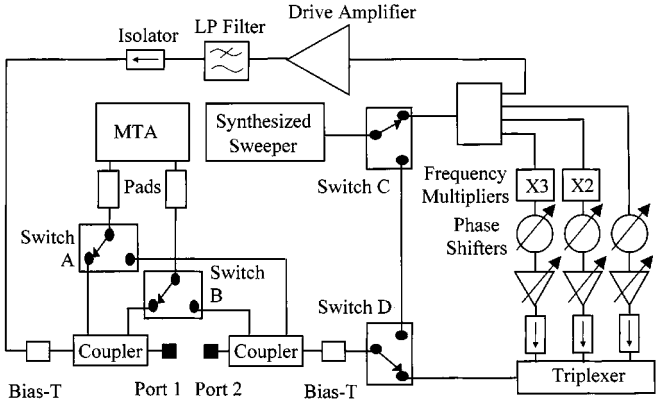

Fig. 1. Schematic of the two-port time-domain load–pull system.

II. System Description

Fig. 1 depicts the block diagram of the developed high-power system for the measurement of in-fixture devices. Time-domain high-power testing capabilities and active load–pull involving three harmonics are integrated in the same test bench.

The system is based on a two-channel sampling oscilloscope and test set, with a similar structure to that presented in [7]. The synthesized sweeper source signal is directed to port 1 or port 2 by the two switches C and D. The directional couplers sense the incident and reflected waves at each side of the device-under-test (DUT). Two of the four coupled waveforms are forwarded to the microwave transition analyzer (MTA) input channels by the switches A and B. Attenuators are inserted in front

of each channel avoiding saturation of the MTA. For the characterization of high-power devices, a 200-W solid-state drive amplifier, with a frequency bandwidth of 1.8–2.0 GHz, can be inserted. A low-pass filter is inserted to suppress any harmonic content generated by the drive amplifier. Isolation at the fundamental frequency between the drive amplifier and port 1 is provided by an additional isolator.

The MTA measures the voltage values of the coupled signals in the time domain through a sampler-based broad-band down-conversion technique followed by digitalization of the signal [8]. The measured incident and reflected voltage waveforms V^i and V^r are directly related to the a- and b-traveling waves

$$\vec{a} = \frac{\vec{V}^i}{\sqrt{Z_0}} \tag{1}$$

$$\vec{b} = \frac{\vec{V}^r}{\sqrt{Z_0}} \tag{2}$$

from which the terminal current and voltage waveforms can be calculated. By taking the ratio of only the fundamental components of the a- and b-waves, s-parameters can also be computed.

The test set allows for the measurement of signals ranging from 0.5 to 12.5 GHz of packaged devices mounted on a microstrip-based fixture. For high-power device characterizations, a high power bias T with a bandwidth of 1.3 to 9 GHz has also been developed. This bias T has been thus far successfully tested up to a continuous wave power of 30 W and a dc current of 10 A and its limits of operation are still to be determined.

For vector corrected s-parameters, a thru-reflect-line (TRL) calibration is used to shift the reference plane to the package leads. Vector correction of time-domain voltage and current waveforms is achieved by a developed absolute calibration technique. System calibration and vector correction are implemented in the PC-based HP-Basic control software. Real-time data analysis allows for an immediate reaction to the measured data in terms of measurement setup, e.g., bias point, drive power level, or device load. Additionally, a deembedding procedure for lumped-element device parasitic networks is implemented, which enables the shift of measurements to the device intrinsic reference planes.

The active harmonic load–pull has a feed-forward architecture [9]. A four-way power splitter provides three fundamental frequency signals of which one is used directly to actively load–pull the DUT at the fundamental frequency. A frequency doubler and tripler provide a second and third harmonic signal components for the active harmonic load–pull. All three signal components can be changed individually in phase and magnitude allowing to set all three harmonic loads anywhere on the Smith chart. The maximum output powers of the solid-state amplifiers included within each load–pull determine the maximum magnitude of the load–pull signals. At present, these powers are 200 W at the fundamental frequency and 40 W at the second and third harmonic frequencies. All amplifiers are followed by an isolator in order to prevent them from any effects due to signals coming from the DUT. The active load–pull system is placed after the sensing couplers at port 2, allowing for the direct measurement of the synthesized load with no extra load–pull calibration required.

With this system configuration, packaged devices have been tested and load–pull measurement performed up to a 30-W output power level.

III. System Absolute Calibration

All microwave s-parameter measurement systems do not instantly provide accurate data, unless a necessary calibration step has been performed using standards that can be traced to international standards [10]. System calibration procedures for s-parameter measurements using full two-port measurement systems have been developed since the beginning of automated network analysis in the late 1960's [11]. Well-established calibration procedures that allow different level of accuracy depending on the desired application are now available. These calibrations fulfill two main requirements: 1) to improve accuracy and 2) to create a well-defined measurement reference plane. The limitation inherent with these calibration procedures is that they operate on s-parameters, which are defined as traveling-wave ratios. As a consequence, only relative measurements are calibrated and absolute power and phase information of incoming and outgoing waves remain undetermined. This restriction needs to be overcome in order to achieve accurate measurements of magnitude and phase of the traveling waves at the measurement reference plane and, consequently, reconstruct voltage and current waveforms at the DUT terminals.

In the first reported magnitude and phase nonlinear measurement setup [12], system calibration relies on the use of a reference diode. Accurate knowledge of nonlinearities of the diode is assumed and used to fully characterize the system. Two other approaches [13], [3] were relying on a vector network analyzer for test-set characterization, and careful modeling of the data acquisition setup. A more recently proposed measurement system [14] is built around two synchronized MTAs, with calibration based on the availability of a multitone reference generator. A reference generator is a multitone generator with accurately known output impedance, where the absolute amplitudes and relative phases of all frequency components are stable and accurately specified. The generator is characterized by a broad-band accurate signal analyzer, tracing the calibration accuracy to a "nose-to-nose" procedure [15].

The system calibration presented in what follows is based on a reformulation of the conventional 12-term directional error model of a four-sampler measurement system for s-parameter measurements depicted in Fig. 2. Two analogous error models are associated to the forward and reverse measurement states. The need for these two sets of error coefficients is related to source switching issues inherent with nonideal reflectometers [16]. Both forward and reverse error models are scaled by an arbitrary factor, giving the two unity frequency response terms. This is due to the fact that frequency response terms always appear as products within the traveling-wave ratio equations that define s-parameters.

An error model that can be extended to absolute vector corrected waveform measurements must fulfill two main requirements: 1) it must be nondirectional and independent from system terminations and 2) correction at both ports at

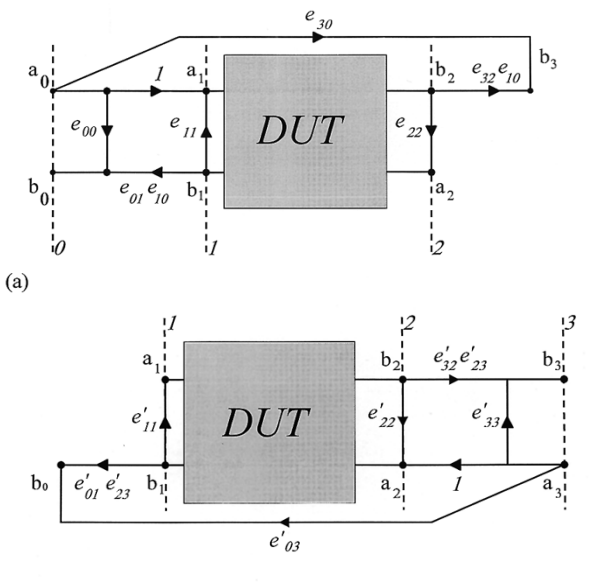

Fig. 2. Traditional 12-coefficient directional error model. (a) Forward. (b) Reverse.

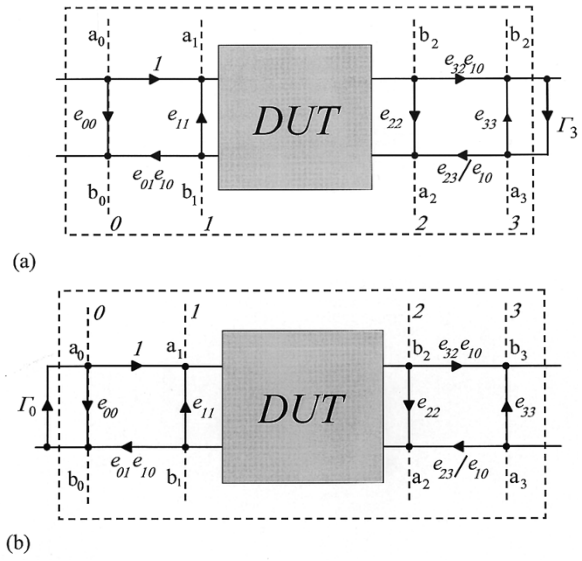

Fig. 3. Modified error model used for the measurement system calibration. (a) Forward. (b) Reverse.

the same time must be possible; namely, all four reference planes must be present in the model. The modified error model depicted in Fig. 3, in which isolation terms have been omitted for simplicity, achieves both conditions. In this formulation, the system error model, which is indicated by the dashed box, does not depend on measurement direction or terminations. Since the MTA system is a reconfigured two-sampler system, special care has been taken in the design in order to allow sampler reconfiguration issues to be ignored. The remaining source switch nonidealities have been brought outside the model by means of the two match error terms Γ_0 and Γ_3, which can be simply measured during calibration by configuring the system source switch to run the directional couplers "backward." For example, during the standard through line forward measurement, inverse s_{22}, obtained by measuring $1/s_{22}$ while sourcing

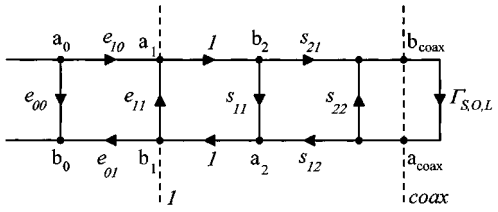

Fig. 4. Modified error model after insertion of the coaxial cable for power calibration.

from port 1, gives the ratio a_3/b_3, which is the wanted source switch match Γ_3. The adopted error model configuration is the same as that used for thru-reflect-line (TRL) calibration, which has been implemented in the controlling HP-Basic software of the system together with other traditional procedures such as short-open-load-through (SOLT) and thru-match-reflect (TMR) [11], [16], [17]. For the particular case of microstrip test environment presented in this paper, TRL calibration was the method of choice [18].

The resulting error model after s-parameter calibration can simply be extended for absolute magnitude and phase correction of the traveling waves, through a further calibration step, which will be referred to as "power calibration," which determines the scaling parameter e_{10}. The response coefficient e_{10} could be directly measured as the ratio a_1/a_0 (see Fig. 3) if we could access the port-1 reference plane with a traveling-wave magnitude and phase measurement system, such as one of the two channels of the MTA. In general though, it is not possible to directly connect a measurement reference port into the coaxial input port of the MTA, e.g., if the reference planes are in microstrip environment or wafer probes. The solution to this problem is to shift reference plane 1 to the end of a coaxial cable suitable for connection to the MTA measurement channel. After inserting a through line between the two measurement ports, a cable is connected at the end of the port 1 directional coupler, or at the load switch D, shown in the system schematic in Fig. 1. By performing a one port short-open-load calibration at the end of the cable, it is then possible to transform wave measurements done at the coaxial reference plane back to the port-1 reference plane. Fig. 4 depicts the flow graph of the modified system after insertion of the coaxial cable, being the s-parameters (s_{11}, s_{21}, s_{12}, s_{22}) associated to the network between port 1 and the coaxial cable reference plane. Symmetry of the response behavior of this network is assumed, hence, the response parameter s_{21} can be calculated.

At this stage, connecting the coaxial cable into the b traveling-wave measuring channel of the MTA changes the system topology, allowing for the through measurement of the ratio $\Gamma_T = b_{\text{coax}}/a_0$. The response error coefficient e_{10} can finally be calculated as follows:

$$e_{10} = \frac{\Gamma_T(1 - e_{11}s_{11})}{s_{21}}. \tag{3}$$

After the coefficient e_{10} has been extracted, since this is the error model scaling factor, the remaining transmission coefficients can be calculated as follows:

$$\begin{aligned} e_{32} &= e_{10}e_{32}/e_{10} \\ e_{01} &= e_{10}e_{01}/e_{10} \\ e_{23} &= (e_{23}/e_{10}) \cdot e_{10}. \end{aligned} \tag{4}$$

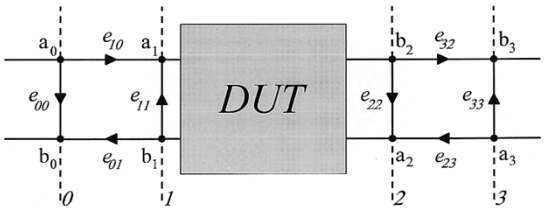

Fig. 5. Complete system error model for waveform vector correction.

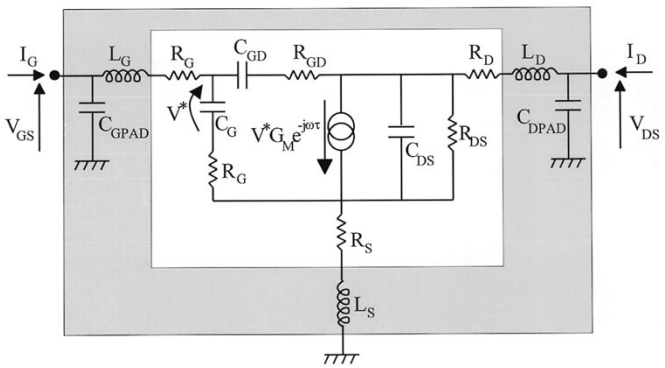

Fig. 6. Small-signal model topology adopted for the LDMOS device (the grey area being the package).

The completely extracted error model as depicted in Fig. 5 allows absolute magnitude and phase of the traveling waves at the DUT reference planes to be simply deembedded from the raw measured waves

$$\begin{cases} b_1 = \dfrac{b_0 - e_{00}a_0}{e_{01}} \\ a_1 = a_0 e_{10} + b_1 e_{11} \end{cases} \qquad \begin{cases} b_2 = \dfrac{b_3 - e_{33}a_3}{e_{32}} \\ a_2 = a_3 e_{23} + b_2 e_{22}. \end{cases} \tag{5}$$

Voltage and current time-domain waveforms are finally obtained, through inverse fast Fourier transform (FFT), from all the relevant frequency components of the calibrated traveling waves. The presented calibration procedure does not account for nonidealities of the MTA input channels, such as mismatch and asymmetry between the two channels. Further calibration steps have been developed to compensate for those effects, but are too extensive for the scope of this paper.

IV. Small-Signal Device Model

Initially, measured time-domain data have immediately shown that, for a meaningful interpretation of the results, all reactive elements need to be characterized and deembedded. The s-parameter data of the device, obtained from the same measurement system, allows for the extraction of a simple small-signal model, which includes parasitic effects [19]. Fig. 6 shows the adopted model, with the device surrounded by the parasitics associated to the package. This model topology achieves reasonable fit of the s-parameter data at various bias points across the region of operation. The values for package reactances and device capacitances, which will be utilized in the following data analysis, are extracted from s-parameters at the self-biasing point of large-signal operation ($V_{\mathrm{DS},Q} = 26$ V $I_{\mathrm{DS},Q} = 260$ mA). Fig. 7 shows the measured s-parameters compared with the model results, while a listing of the extracted parameter values is shown in Table I. The reactive parasitic elements can now be deembedded from measured waveforms; hence, shifting the measurement reference planes. The time-domain output current and voltage data presented in this paper is shifted to the output current generator plane, providing a better understanding of the device intrinsic behavior.

V. Waveform Measurement System Validation

Before further proceeding, the measurement results obtained from the system were validated. First, small-signal s-parameters obtained from the waveform measurement system were compared with measurements performed using an HP8510C. The agreement between the two systems was better than -45 dB, verifying the waveform measurement system capability to measure accurate s-parameters.

Furthermore, the developed small-signal model for the LDMOS device was utilized for investigation on the convergence of large-signal waveform measurements toward small signal. For this purpose, an arbitrary load with a high reflection coefficient was attached to the DUT and the device input reflection coefficient determined from the measured waveforms at the small-signal power level. This measured reflection coefficient was compared with the one simulated using the small-signal model terminated into the same load. The agreement between the two was better than -30 dB in magnitude and 3° in phase, demonstrating that the s-parameters obtained from waveform measurements at small-signal power level are correct. Additionally, from the small-signal model, the time delay occurring between the output generator current and the intrinsic input voltage is predicted: $\mathrm{Total\ Delay} = Cgs \cdot Rgs + \mathrm{Tau}$, giving 40 ps (see Table I). From deembedded waveforms measured at the small-signal power level, the time delay between the output current and input voltage waveforms is found to be 43 ps, which is consistent with the small-signal model prediction. These investigations strongly indicate the correctness of both s-parameter and waveform measurement capabilities of the system.

VI. Fundamental Load–Pull Measurement

A comprehensive fundamental-frequency load–pull investigation has been performed on the device, biased at pinchoff with drain voltage $V_{\mathrm{DS}} = 26$ V. Fig. 8 shows the resulting load–pull contours of drain efficiency, both at the extrinsic package leads plane and after deembedding at the current generator plane. For the measurement of the load–pull contours, the second and third harmonic load were 50 Ω at the package leads. Contours generated for output power and power gain show similar behavior and give similar optimum loads. The optimum output reflection coefficient $\Gamma_{\mathrm{OPT}} = (0.78@156°)$ at the package lead plane, resulting in an optimum admittance $Y_{\mathrm{OPT}} = (15.8 - j5.2)$ mS at the current generator plane, gave a maximum drain efficiency $\eta = 59.5\%$, output power $P_{\mathrm{OUT}} = 3.91$ W, power gain $G = 13.6$ dB, and a -1 dB compression point of $P_{\mathrm{IN}} = 22.4$ dBm. A swept input power measurement was performed on the device into this optimum fundamental load. Figs. 9 and 10 show the RF dynamic load lines, as well as the output harmonic power content at increasing output power levels. It can be readily

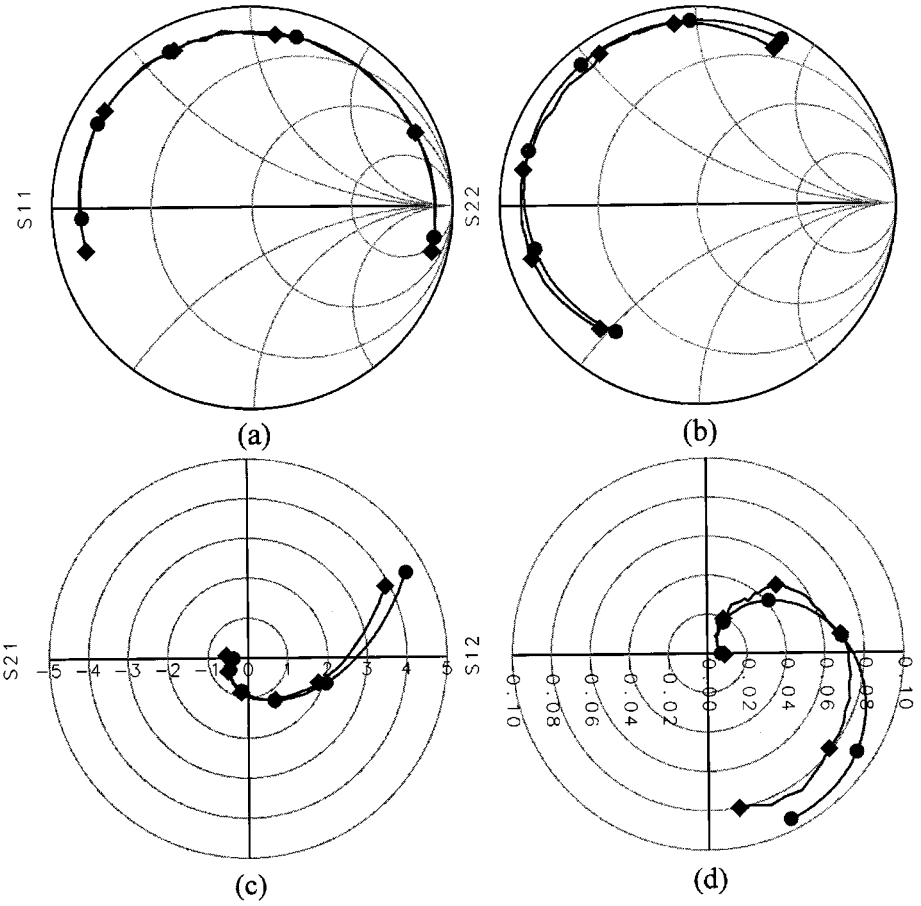

Fig. 7. Small-signal modeling results at the quiescent bias point from 1.3 to 6 GHz, measured (squares) and simulated (circles).

TABLE I
EXTRACTED SMALL-SIGNAL MODEL PARAMETERS AT THE QUIESCENT OPERATING POINT (ALL REMAINING PARAMETERS ARE SET TO ZERO)

C_{GPAD}	C_{DPAD}	L_G	L_D	L_S	R_D	C_{GS}	C_{GD}	C_{DS}	R_{GS}	G_{DS}	G_M	Tau
610fF	440fF	1.27nH	1.10nH	55pH	1.1Ω	9.38pF	144fF	2.95pF	2.1Ω	1.58mS	350mS	20ps

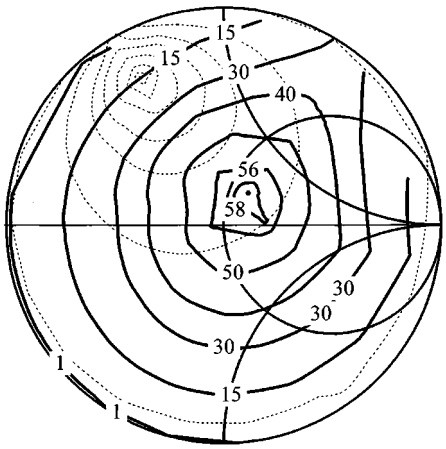

Fig. 8. Efficiency load–pull contours: extrinsic (dotted) and intrinsic (solid).

identified from the measured RF load lines that the device has an inherent almost accomplished class-B harmonic loading [2], which is due to the output parasitic network. In particular, the large output capacitance creates almost a short circuit for the harmonics at the output current generator plane.

VII. HARMONIC TUNING FOR EFFICIENCY

The harmonic tuning was performed on the device biased in the same bias point applying the fundamental load Γ_{OPT} at the package lead, while changing the second and third harmonic load at the current generator plane. In the following investigation, the appropriate loads to be applied at the package leads have been computed using the small-signal model. The drive level of 19.2 dBm, which is backed off by approximately 3 dB from the -1-dB compression point, provides a high gain, while still having a high harmonic content, thus allowing for harmonic tuning [20]. In order to investigate the effect of harmonic tuning on the device, a first measurement involved a 50-Ω match at the second and third harmonic frequency at the current generator plane. This measurement resulted in an output power of 2.5 W with an efficiency $\eta = 47\%$.

Class-F loading was investigated next, applying a short at the second harmonic and open at the third harmonic frequency

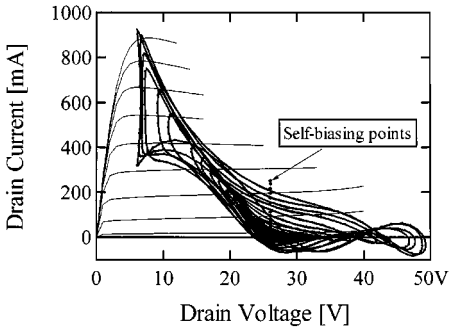

Fig. 9. RF load lines at increasing input power into optimum fundamental load, together with measured dc output characteristics.

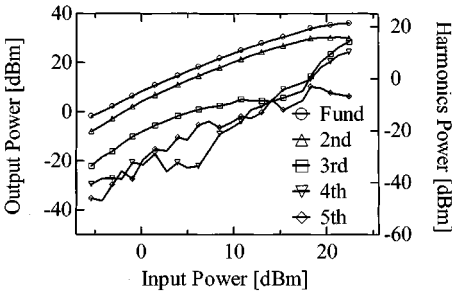

Fig. 10. Harmonic powers at increasing input power into optimum fundamental load.

[21] at the current generator plane. The result was an increase in both the output power and efficiency. In order to show how much harmonic loading at constant output power can improve efficiency, $V_{\rm DS}$ was reduced until the device provided the same output power $P_{\rm OUT} = 2.5$ W, resulting in efficiency $\eta = 59\%$. This indicates that the increase in efficiency was achieved by squaring the voltage waveform [1], [2]. However, the obtained efficiency, which is far from the theoretical value achievable with three harmonic loads [1], suggest that the applied loading does not constitute the optimum class-F loading. This can be readily verified by looking at the measured current and voltage waveforms. Fig. 11 shows the waveforms before [see Fig. 11(a)] and after [see Fig. 11(b)] harmonic tuning. It can be seen that the achieved gain in efficiency is due to a slightly more compressed (squared) voltage waveform, as well as by a reduction of the area where high current and voltage values co-exist. These results agree with theoretical considerations [20] that a short at the second harmonic and open at the third harmonic do not always constitute an optimum class-F loading.

VIII. Harmonic Tuning Through Waveform Engineering

Applying the same traditional harmonic-tuning approach to the device at the optimum operating conditions described in Section VI improved overall neither the efficiency ($\eta = 59.5\%$), nor the output power ($P_{\rm OUT} = 3.91$ W). It was, therefore, decided to directly use the time-domain waveform data as an alternative load–pull approach, with the aim of engineering the intrinsic current and voltage waveforms in order to improve the device performances. The results are shown in Fig. 12, depicting output current and voltage waveforms before and after waveform engineering. While changing the fundamental load in order

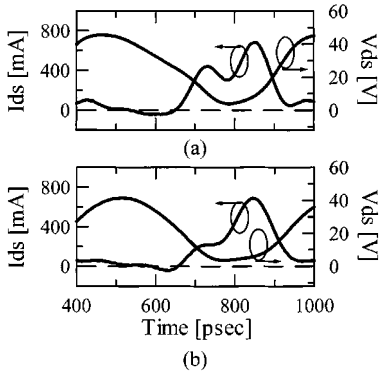

Fig. 11. Measured waveforms at the output current generator: (a) before and (b) after harmonic tuning for efficiency.

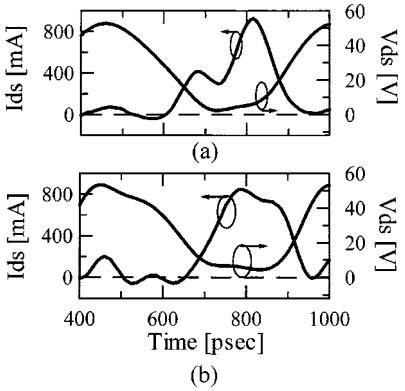

Fig. 12. Measured waveforms at the output current generator: (a) before and (b) after waveform engineering.

to increase the peak current, the second harmonic load is varied in order to reduce the dip within the current waveform. This results in an output power increase by 450 mW while maintaining the efficiency at $\eta = 59.5\%$. The loading for the third harmonic is then used to square the voltage waveform and to minimize the overlap between the voltage and current. The final current and voltage waveforms, depicted in Fig. 12(b), were a tradeoff between reducing their overlap and increasing the current values in the area of low voltages. Overall, the tuning increased the output power by 800 mW (20%), giving in total $P_{\rm OUT} = 4.71$ W, without compromising gain and efficiency. The resulting harmonic loads at the current generator plane are: fundamental $\Gamma_{\rm OPT} = (0.535\angle 156°)$, second harmonic $\Gamma_{\rm 2ND} = (1.0\angle -57°)$, and third harmonic $\Gamma_{\rm 3RD} = (1.0\angle -158°)$.

Fig. 12(b) depicts both the current and voltage having a square-shaped waveform, which explains the increase in output power due to the increased fundamental current swing [2], but not an increase in efficiency due to the increased quiescent point of a squared waveform. The fact that the gain has not changed suggests that further improvement in efficiency and output power could be achieved by increasing the drive level, but neither the efficiency nor output power are found to increase significantly with higher drive level. Besides, a dipping in the current waveform appears while the output power is increased, as shown in Fig. 13 for a drive level increased by 2 dB. This indicates a drive dependent effect, which prevents the device from reaching its optimum performance.

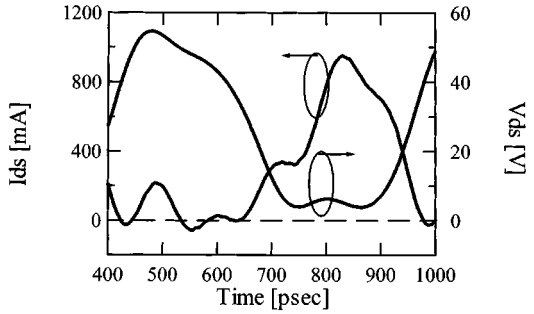

Fig. 13. Measured waveforms at the output current generator after waveform engineering and 2-dB increase in drive level.

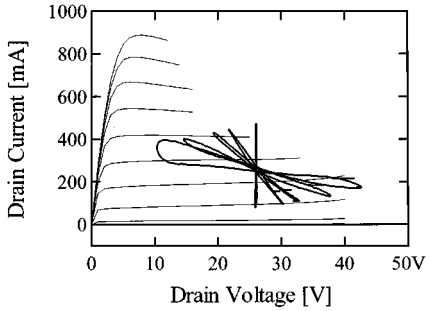

Fig. 14. Measured RF load lines with $V_{\mathrm{DS},Q} = 26$ V and $I_{\mathrm{DS},Q} = 260$ mA.

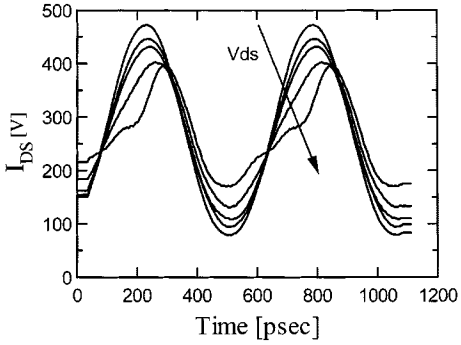

Fig. 15. Measured output current waves for changing loads, resulting in an increased output voltage waveform swing indicated by the arrow.

IX. Device Investigation Through Waveform Analysis

The reoccurring current dips with increasing drive level might result from the injection of harmonic components from the drive amplifier or from other device nonlinearities. Measurements have shown that the harmonic large-signal reflection coefficients of the source are found to be constant with drive power level, confirming that the drive stage followed by the low-pass filter is not injecting any harmonic components. In order to identify the origin of the current distortion, the device has been measured for the set of load lines shown in Fig. 14, all measured at the same drive signal level. Fig. 15 shows the correspondent measured current waveforms presenting an increasing distortion for increasing output voltage swing. The output current consists of a real current component, whose dependency on V_{DS} is defined by the output conductance and a displacement current term. Since the voltage waveform does not progress into the knee region, we can assume that the transconductance does not change significantly along the measured load lines. Therefore, it can be concluded that the distortion of the output current is caused by the displacement term associated to nonlinear capacitances. This directly demonstrates the significance of nonlinear capacitance effects for the performance of the power amplifier operating in high-efficiency modes. Therefore, in order to further improve the efficiency of power amplifiers based on LDMOS devices, nonlinear capacitance will have to be accounted for.

X. Conclusions

A time-domain measurement system and a waveform vector correction technique have been developed and validated. High-power measurements at levels consistent with telecommunication applications (at present up to 30 W) have been performed on commercially available LDMOS devices. Through the integration of this system with harmonic load–pull, operating also at these high-power levels, a novel load–pull approach based on real-time waveform engineering has been demonstrated. Experimental investigation on 4-W LDMOS devices showed how "real-time" knowledge of the voltage and current waveforms was essential when optimizing (tuning) for both power and efficiency. Waveform engineering at various drive and load conditions additionally provided direct insight into the nonlinear device behavior, identifying the nonlinear capacitance effects as being a dominant design issue for power-amplifier performance.

References

[1] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2007–2012, Nov. 1997.

[2] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[3] M. Sipila, K. Lehtinen, and V. Porra, "High-frequency periodic time-domain waveform measurement system," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1397–1405, Oct. 1988.

[4] M. Demmler, P. J. Tasker, and M. Schlechtweg, "A vector corrected high power on-wafer measurement system with a frequency range for the higher harmonics up to 40 GHz," in *24th European Microwave Conf.*, 1994, pp. 1367–1372.

[5] P. J. Tasker, M. Demmler, M. Schlechtweg, and M. Fernandez-Barciela, "Novel approach to the extraction of transistor parameters from large signal measurements," in *24th European Microwave Conf.*, 1994, pp. 1301–1306.

[6] D. Barataud, C. Arnaud, B. Thibaud, M. Campovecchio, J.-M. Nebus, and J. P. Villote, "Measurements of time-domain voltage/current waveforms at RF and microwave frequencies based on the use of a vector network analyzer for the characterization of nonlinear devices—Application to high efficiency power amplifiers and frequency-multipliers optimization," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1259–1264, May 1998.

[7] P. J. Tasker, S. S. O'Keefe, G. D. Edwards, W. A. Philips, M. Demmler, M. C. Curás-Francos, and M. Fernández-Barciela, "Vector corrected nonlinear transistor characterization," in *5th European Gallium Arsenide Related III–V Compound Applicat. Symp. Dig.*, Bologna, Italy, 1997, pp. 91–94.

[8] "The microwave transition analyzer: Measure 25 ps transitions in switched and pulsed microwave components," Hewlett-Packard, Santa Rosa, CA, HP product note 70 820-2.

[9] Y. Takayama, "A new load–pull characterization method for microwave power transistors," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1976, pp. 218–220.

[10] "Specifying calibration standards for the HP 8510 network analyzer," Hewlett-Packard, Santa Rosa, CA, HP product note 8510-5A, 1997.

[11] W. Kruppa and K. F. Sodomsky, "An explicit solution for the scattering parameters of a linear two-port measured with an imperfect test set," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 122–123, Jan. 1971.

[12] U. Lott, "Measurement of magnitude and phase of harmonics generated in nonlinear microwave two-ports," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1506–1511, Oct. 1989.
[13] G. Kompa and F. van Raay, "Error-corrected large signal waveform measurement system combining network analyzer and sampling oscilloscope capabilities," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 358–365, Apr. 1990.
[14] J. Verspecht, P. Debie, A. Barel, and L. Martens, "Accurate on wafer measurement of phase and amplitude of the spectral components of incident and scattered voltage waves at the signal ports of a nonlinear microwave device," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, May 16–20, 1995, pp. 1029–1032.
[15] J. Verspecht and K. Rush, "Individual characterization of broad-band sampling oscilloscopes with a nose-to-nose calibration procedure," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 247–354, Apr. 1994.
[16] D. Rytting, "Appendix to an analysis of vector measurement accuracy enhancement techniques," in *Hewlett-Packard RF Microwave Symp. Dig.*, Mar. 1982, pp. 1–42.
[17] G. F. Engen and C. A. Hoer, "Thru-reflect-line: An improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 987–993, Dec. 1979.
[18] "In-fixture microstrip device measurements using TRL* calibration," Hewlett-Packard, Santa Rosa, CA, HP product note 8720-2, 1991.
[19] D. Lovelace, J. Costa, and N. Camilleri, "Extracting small-signal model parameters of silicon MOSFET transistors," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, San Diego, CA, 1994, pp. 865–868.
[20] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "On the class-F power amplifier design," in *International Journal of RF and Microwave Computer-Aided Engineering*. New York: Wiley, 1999, vol. 9, pp. 129–149.
[21] D. M. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and over-driven RF power amplifiers," *IEEE Trans. Electron Devices*, vol. ED-14, pp. 851–857, Dec. 1967.

Johannes Benedikt was born in Olsztyn, Poland, on January 2, 1969. He received the Dipl.-Ing. degree in electrical engineering from the University of Ulm, Ulm, Germany, in 1997, and is currently working toward the Ph.D. degree at Cardiff University, Cardiff, U.K.

In October 1997, he joined the Circuit Systems Research Group, Cardiff University, Cardiff, U.K., where he started a collaborative research project with Nokia Networks, Camberley, U.K. His main work interests are nonlinear microwave characterization and measurement systems, their application to linear-efficient high-power amplifiers for future telecommunication systems, as well as the design and realization of microwave linear-efficient high-power amplifiers.

Roberto Gaddi was born in Reggio Emilia, Italy, on May 27, 1972. He received the Laurea degree (*cum laude*) in electronic engineering from the University of Parma, Parma, Italy, in 1997, and is currently working toward the Ph.D. degree at Cardiff University, Cardiff, U.K.

After serving in the army in 1998, he joined the Dipartimento di Scienze dell'Ingegneria, University of Modena, Modena, Italy, where he collaborated with the device reliability physics group and studied aging and failure mechanisms of electron devices for high-frequency applications. In October 1998, he joined the Centre for High Frequency Engineering, Cardiff University, Cardiff, Wales, and is currently working in collaboration with Nokia Networks. His research work covers large-signal time-domain measurement techniques at radio and microwave frequencies and nonlinear characterization and modeling of high-power high-frequency transistors such as silicon LDMOSFETs for telecommunication applications.

Paul J. Tasker was born in Douglas, Isle of Man, U.K., in 1958. He received the B.Sc. degree (first-class honours) in combined studies, physics, and electronics and the Ph.D. degree from Leeds University, Leeds, U.K., in 1976 and 1983, respectively.

From January 1984 to December 1989, he was with Cornell University, Ithaca, NY, as a Research Associate, where he established and managed a research program in the area of fabrication, design, characterization (dc and microwave) and modeling (analytical and numerical) of compound semiconductor devices. In January 1990, he joined the Frauenhofer Institut für Angewandte Festkörperphysik (Frauenhofer IAF), Freiburg, Germany, where he managed groups responsible for the development, characterization, and optimization of compound semiconductor devices and the development, design, and characterization of millimeter-wave monolithic microwave integrated circuits (MMICs). In August 1995, he joined the School of Engineering, Cardiff University, Cardiff, U.K., as Professor of electronic engineering, where he currently establishes research activities in both high-frequency semiconductor devices and microwave nonlinear characterization techniques. His main technical interest and expertise are in areas of fabrication, characterization, and optimization of high-frequency (microwave and millimeter-wave) compound semiconductor electronic and optoelectronic devices and circuits, along with expertise in high-frequency (microwave and millimeter-wave) characterization and measurement systems. He has also consulted for various industries, including General Electric, AT&T, Bell Laboratories, Alpha, Martin Marietta, Siemens, Nokia, and EG&G Prinston Applied Research, Celeritek, U.K., in the areas of device design, characterization, and modeling.

Martin Goss was born in Loda, Yemen, in 1965. He received the B.Sc. degree in electronic engineering with communications from Sheffield University, Sheffield, U.K, in 1995.

From July 1995 to January 1997, he was with Navico, a Marine Radio/Electronics Company, where he ensured electromagnetic compatibility (EMC) compliance. Since February 1997, he has been with Nokia Networks, Camberley, U.K., where he is currently a Senior RF Engineering concentrating on high-power amplifier design for current and future base-station requirements. He has been actively involved in collaboration between Nokia Networks and Cardiff University since August 1997, focusing on large-signal time-domain characterization of high-power high-frequency transistors, such as LDMOSFETs for use in base-station power-amplifier applications.