A High-Efficiency and Low-Phase-Noise 38-GHz pHEMT MMIC Tripler

Ali Boudiaf, *Member, IEEE*, Didier Bachelet, and Christian Rumelhard, *Member, IEEE*

***Abstract*—Frequency translation circuits are key elements in communication systems. This paper presents a frequency tripler for 38-GHz short-range communication systems, designed using a pseudomorphic high electron-mobility field-effect transistor (pHEMT) technology. The successful first iteration monolithic microwave integrated circuit achieved a state-of-the-art output power of 3.1 dBm and a minimum conversion loss of 3.4 dB. The multiplier exhibits a conversion efficiency of 11% and average phase noise degradation at 10 and 100 kHz offset frequency from carrier of 9 $\pm$ 1 dB. Through a comprehensive study of the frequency multiplier, we demonstrate the optimum performance achieved under a class B mode of operation. To our knowledge, this is the first reported Ka-band single-stage frequency tripler based on pHEMT technology that has been fully characterized for phase noise degradation.**

***Index Terms*—Millimeter-wave frequency conversion, monolithic microwave integrated circuit (MMIC) frequency converters.**

I. Introduction

POINT-TO-POINT millimeter-wave digital radio communications are rapidly developing due to consumer application emergence, offering unprecedented opportunities to the microwave industry. These communication systems require stable, compact, local oscillator sources to translate base-band signals to microwave frequencies. The modulation schemes used in digital microwave radios, for achieving high data-transmission rates up to 155 Mbytes/s, must balance the effects of phase noise from local oscillators to meet the specifications in terms of bit error rates (BERs) [1], [2]. Phase noise specifications for millimeter-wave radios for the most common modulation schemes are listed in Table I [5].

Frequency multipliers are used extensively for transmitters and receiving chains in modern systems [10]. The active multipliers have the advantage over the diode-based type for lower conversion loss or even, in some cases, conversion gain and monolithic microwave integrated circuit (MMIC) process compatibility [6]. The signal generation in the millimeter-wave bands can be realized either directly by an oscillator [4] or by multiplication from a lower frequency. The second approach increases the flexibility of the system design, allowing the use of a technology with superior noise performance for realizing high-quality oscillators at lower frequencies in combination with a high-electron mobility transistor (HEMT) technology for the multiplier. Active multipliers have generally been configured as frequency doublers [10], although many system configurations operating in the millimeter-wave range may require frequency triplers. However, the development of such circuits is still a challenge. To our knowledge, very few single-stage millimeter-wave field-effect transistor (FET) triplers have been reported so far [3], [5], [6], [8], but none of them has been characterized in terms of phase noise degradation or conversion efficiency. In the literature, there is apparently little substantive in-depth coverage of this topic with supporting modeled and measured data for either bipolar junction transistor or FET family realization.

A comprehensive study of a single-stage frequency tripler based on GaAs pHEMT technology, for 38-GHz short-range communication applications, is presented. Special emphasis is placed on exploring the different means of third harmonic generation in Section II while yielding explanations for the importance of harmonic terminations, drain voltage distortion, and comparing the state-of-the-art frequency tripler performance achievements. In Section III, a specific computer-aided design (CAD) oriented design method, based on the "substitute generator technique," is used to demonstrate the optimum frequency tripler performance achieved under a class B mode of operation.

In Section IV, we describe the experimental characterization performed to find the optimum operating conditions of the

TABLE I
PHASE NOISE SPECIFICATIONS FOR DIGITAL RADIOS

BPSK	**-85 dBc/Hz @ 100 kHz**
QPSK	**-90 dBc/Hz @ 100 kHz**
16QAM	**-90 dBc/Hz @ 10 kHz**

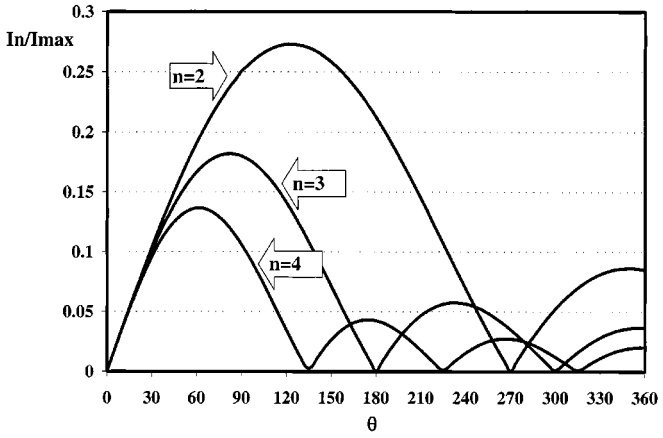

Fig. 1. Normalized harmonic current as function of conduction angle.

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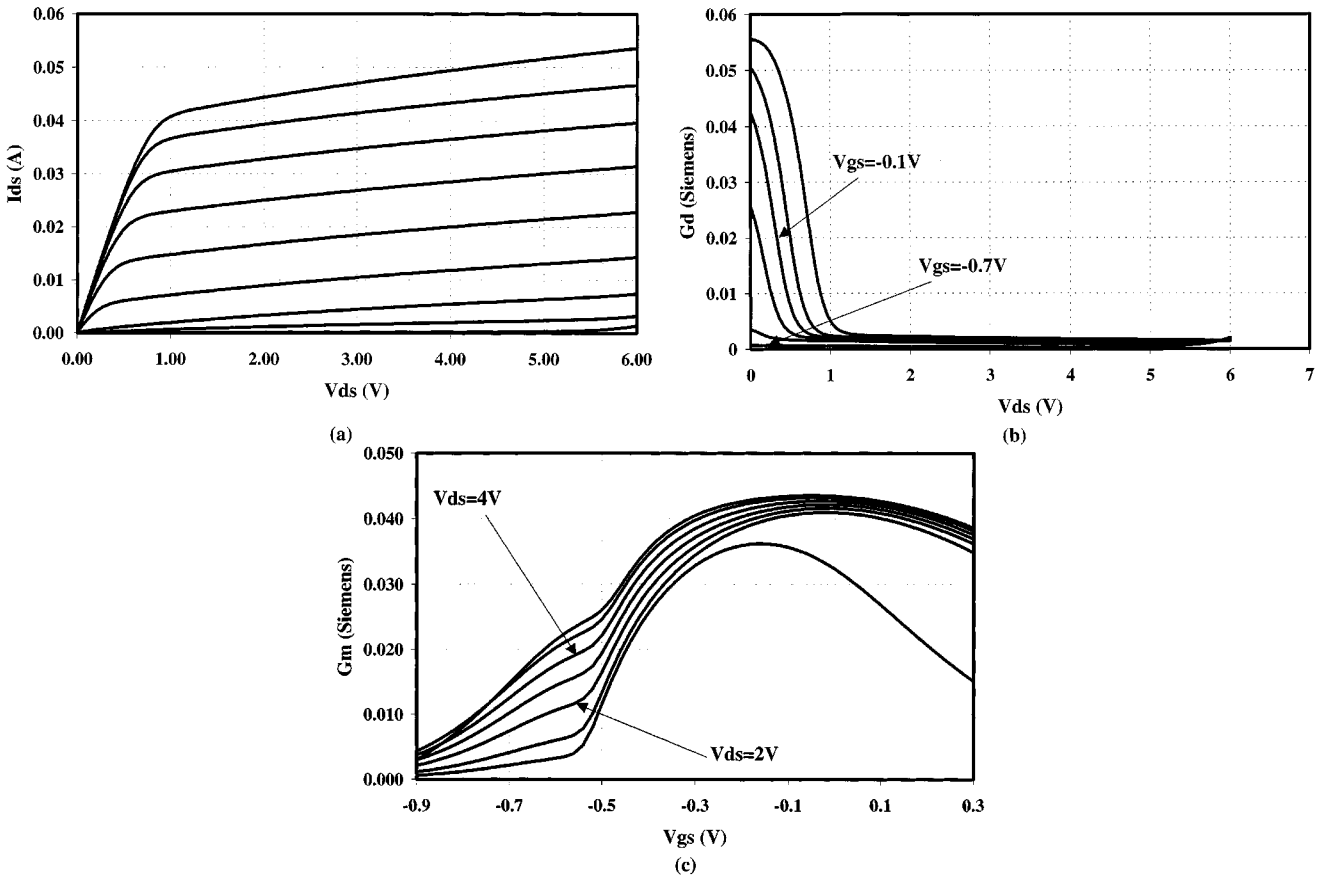


Fig. 2. (a) Simulated I–V curves of ED02AH pHEMT transistor, nonlinear elements, (b) the output conductance G_d, and (c) the transconductance G_m as a function of $V_{\rm ds}$ and $V_{\rm gs}$.

tripler, which validated the design methodology. To address the spectral purity issue related to the frequency multiplier, an experimental investigation of phase noise degradation due to the active frequency tripler is also described. The MMIC chip, which was developed and fabricated using the ED02AH pHEMT from Philips-PML technology, achieved the optimum operating conditions of 3.1-dBm output power level at 38.64 GHz, 3.4 dB conversion loss with 11% conversion efficiency, and a very low phase noise degradation at 10 and 100 kHz offset frequency of 9 ± 1 dB. To the authors' knowledge, these are the best achieved performances for a frequency tripler designed for 38-GHz applications.

II. Harmonic Generation for FET Triplers

The standard procedure to design a frequency multiplier is to determine the appropriate biasing and the best conduction angle for the active device to generate at the output a signal waveform rich with the desired harmonic. The first approximation is found by calculating the derivative of the specific harmonic current in respect to the conduction angle assuming a constant transconductance. Applying a sinusoidal gate voltage, the drain current is composed of a train of cosine-wave tips that can be expressed by the Fourier series [7] as

$$I_d(t) = I_0 + I_1\cos(\omega_0 t) + I_2\cos(2\omega_0 t) + \cdots + I_n\cos(n\omega_0 t) \quad (1)$$

where for $n = 0$

$$I_0 = \frac{2I_{\max}}{\pi}\frac{t_0}{T} \quad (2)$$

for $n \geq 1$

$$I_n = I_{\max}\frac{4\cdot t_0}{\pi\cdot T}\left|\frac{\cos\left(n\cdot\pi\cdot\frac{t_0}{T}\right)}{1-\left(2\cdot n\cdot\frac{t_0}{T}\right)^2}\right| \quad (3)$$

if $n = (T/2\cdot t_0)$

$$I_n = I_{\max}\frac{t_0}{T}. \quad (4)$$

$I_{\max}$ is the peak drain current, and the ratio of the conduction time over the period of the input signal defines the conduction angle $\theta = 2\cdot\pi(t_0/T)$. Fig. 1 shows a plot of the normalized harmonic currents $I_n/I_{\max}$ as a function of the conduction angle when $n = 2$ to $n = 4$. From this figure, one way to generate current waveform rich in third harmonic is by biasing the device in class C with an optimum conduction angle of 80°. The maximum normalized third harmonic current is 0.185 in this case. However, this mode of operation is not adequate, because it requires a high breakdown-voltage device.

The second approach consists of biasing the device in class A and overdriving it until there is a clipping due to pinchoff on the negative swing and due to gate conduction on the positive swing. In this case, the drain current waveform tends to be a square waveform, for which only odd harmonics exist. A theoretical analysis of this mode of operation has been presented by

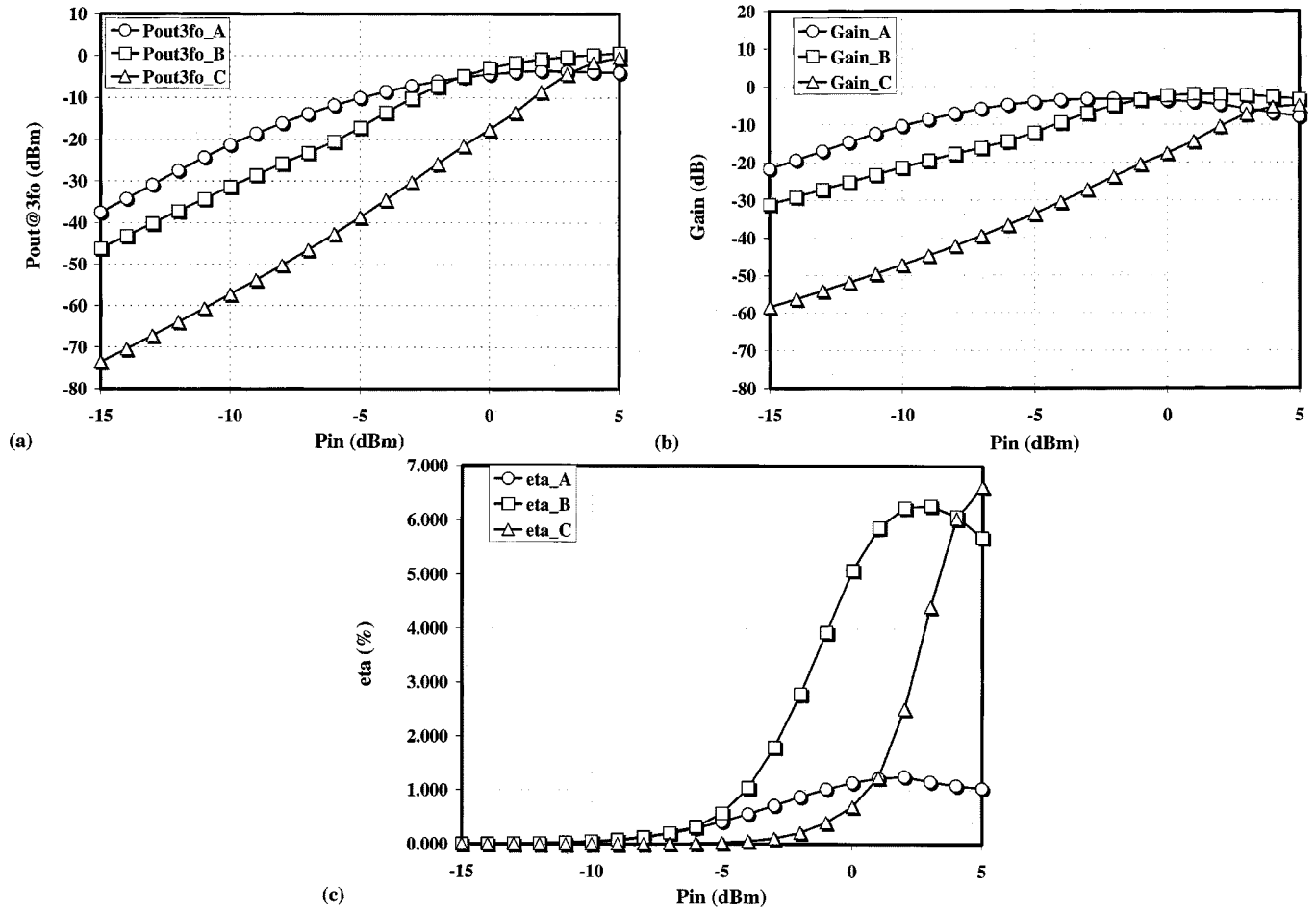


Fig. 3. Response simulations to various classes of operation: (a) output power, (b) conversion gain, and (c) conversion efficiency.

Fudem [6]. It is stated that for a full drive, with a knee voltage set to zero, the power at the third harmonic is 4.8 dB below that of the fundamental. The output efficiency η, defined as the ratio of the output power at the third harmonic over the dissipated dc power, is 16.7%. For the overdriven class A mode of operation, a high gate resistor is usually needed to limit the gate dc conduction and assure a reliable operation [5]. As can be seen in the design of the active balanced tripler in [6], the achieved results for the 15/45-GHz tripler were 12.5 dBm output power and 11 dB conversion loss. The suppression of the fundamental and the second harmonic were 40 and 20 dB, respectively.

For efficient operation of the previous biasing schemes, short circuits are required across the transistor's output at all frequencies except for the third harmonic. A third option to get a high third harmonic is based on the generation of distorted drain voltage waveform. It is obtained by biasing the device in class A and presenting short circuits at the even harmonics and open circuits at the odd harmonics, except for the output third harmonic, which is matched for maximum output power. The voltage distortion approach provides higher odd harmonic current, compared to the previous approaches, as described by Camargo [5]. Published results over the fundamental frequency band 8.5–10.5 GHz tripler using the latter technique achieved 10 dB of conversion loss for 10-dBm input drive [11].

The remaining biasing schemes class AB and B, which are defined when the device is biased near or at the pinchoff gate voltage V_p *a priori*, seem not to be appropriate for third harmonic generation. Based on Fig. 1, when the angle of conduction is equal to 180°, there's no third harmonic component. Also, it has been stated in some previous studies that class B FET multipliers have poor conversion gain and good dc to radio-frequency (RF) efficiency [9], compared to class A FET multipliers, which provide better conversion gain but poor dc to RF efficiency. In spite of these arguments, two recent studies have been published on tripler design based on a class B bias scheme. Zhang [8] proposed to add a fundamental rejection feedback on the output to adjust independently the load of the fundamental frequency and the third harmonic; therefore, the conversion gain can be improved. They demonstrated a 11.5/34.5-GHz HEMT tripler that achieved 7 dB of conversion loss for 0 dBm input drive. The second study, by Thibaud [3], designed a 13/39-GHz pHEMT tripler using a single-ended topology and followed by an output buffer amplifier. The achieved results were 3 dB of conversion loss for an input drive of 16 dBm, with the fundamental and the second harmonic suppression of 37 and 21 dB, respectively. Unfortunately, the authors of these two studies did not give enough explanation on how the third harmonic generation had been enhanced for the class B mode of operation, nor

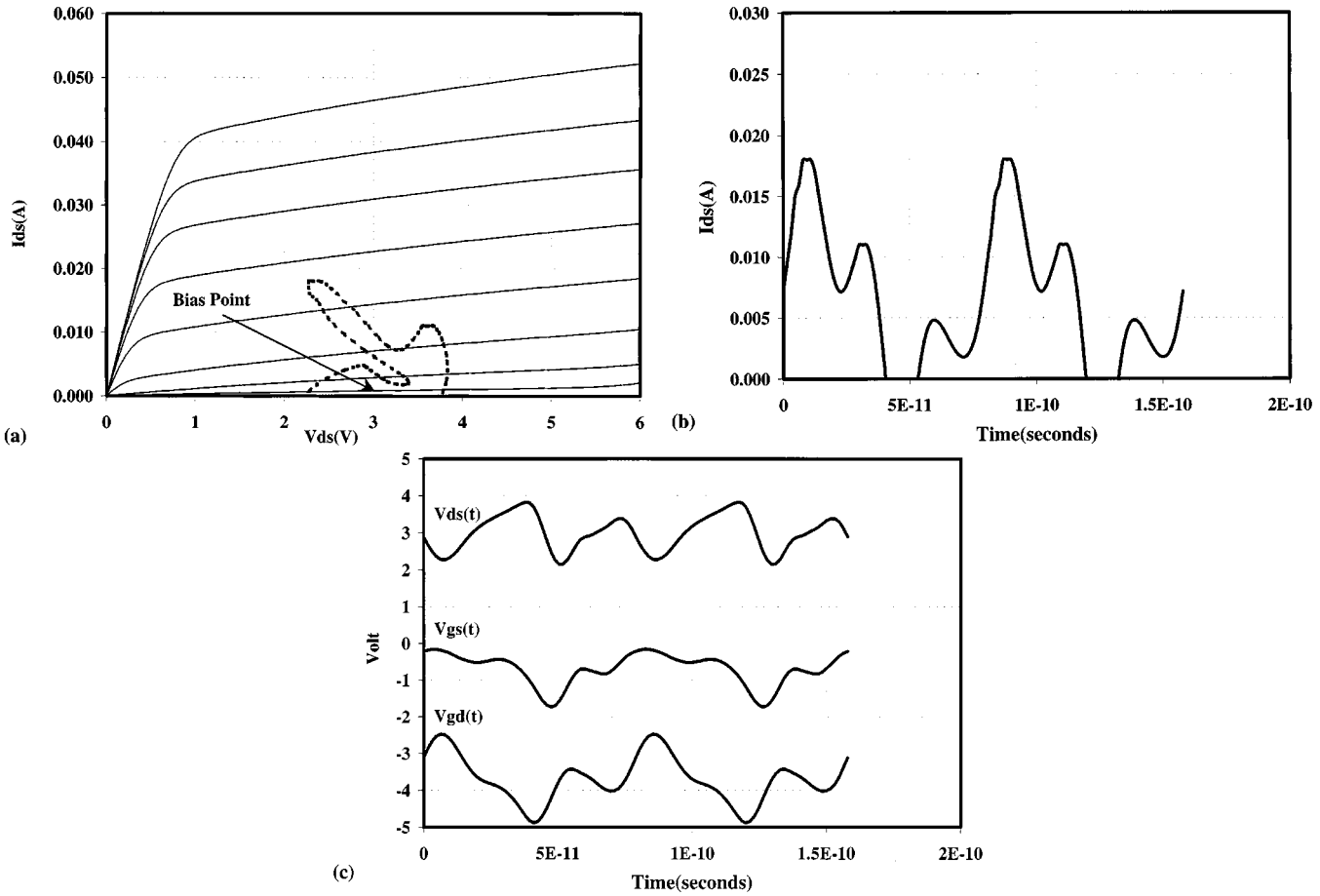


Fig. 4. Simulated time-domain signal waveforms: (a) device dynamic load-line with dc curves, (b) device drain current waveform, and (c) input/output device voltage waveforms.

did they describe the different characteristics of their tripler in terms of conversion efficiency and phase noise degradation.

III. Circuit Design

The frequency tripler is based upon a common source, single-ended topology. The active device is a 6×15 μm GaAs pHEMT with a gate length of 0.2 μm and an f_T of 62 GHz from Philips Microwave Limeil foundry. It is known that the elements that contribute to the nonlinear behavior are the drain-source current $I_{\rm ds}$, gate-source capacitance $C_{\rm gs}$, gate-drain capacitance $C_{\rm gd}$, and diodes $D_{\rm gs}$ and $D_{\rm gd}$, which describe the forward conduction of gate-source and gate-drain junctions, but the dominant nonlinear sources causing frequency multiplication are the transconductance G_m, and the output conductance $G_{\rm ds}$ (Fig. 2).

The first set of simulation was done to investigate the performance of the frequency tripler under three classes of operation A, B, and C. For class A, $I_{\rm ds}$ was set to 50% $I_{\rm dss}$. For class B, $V_{\rm gs}$ was set to V_p, pinchoff voltage, and for class C, $V_{\rm gs}$ was set to a value below V_p such as the conduction angle meets the optimum defined in the previous paragraph. The following analysis provides motivation for development of an optimal design approach. To assess performance under various bias conditions, we used the same terminating impedance for the multiplier at the fundamental and the harmonic frequencies. For the input, we have set a short-circuit at the second and third harmonic

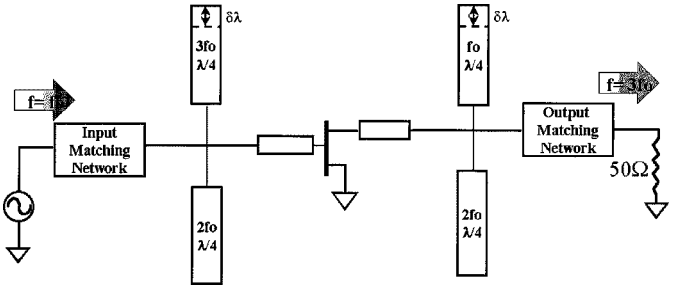


Fig. 5. Single-ended frequency tripler schematic.

and matched the fundamental. On the output side, we have optimized the termination at the fundamental, set a short-circuit at the second harmonic, and matched the third for maximum power transfer. The results of these simulations are reported in Fig. 3. We can see from these curves that class A FET tripler provides better conversion gain [Fig. 3(b)] and higher output power than class B [Fig. 3(a)] only for low input-power levels. When input power increases, there is a cross-point above which class B starts to show a better conversion gain and a higher output power. Moreover, a better conversion efficiency is achieved for the same levels of input power [Fig. 3(c)]. The conversion efficiency is defined as the ratio of output power at the third harmonic over the sum of the dissipated dc power and the RF input power injected at the fundamental frequency.

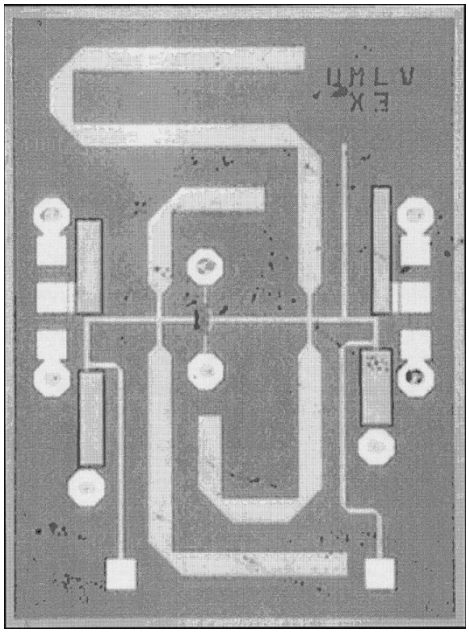


Fig. 6. Photograph of the MMIC layout.

The second step of the design consists of optimizing the waveforms and the harmonic terminations. The bias point is set now near the pinchoff region [Fig. 4(a)]. In order to generate high odd harmonics, we used a new technique that controls simultaneously all the harmonic terminations through a specific CAD-oriented design method of frequency multipliers, based on the "substitute generator technique" [3], [12]. Its fundamental principle is to force voltages at both ports of the transistor with independent generators at specific frequency harmonics. This approach has been implemented in the nonlinear harmonic-balance software, HP-EESOF MDS, to visualize and to control the current/voltage waveforms at both ports of the device under test and the associated load lines.

The determination of the optimum operating conditions, in order to get a maximum output power and low conversion loss over a given frequency bandwidth, has been achieved through some swept harmonic-balance analysis. The multiplier's dynamic load line has been optimized within the limits imposed by the breakdown voltage $V_{\rm gd}$ and the conduction input diode $V_{\rm gs}$ (Fig. 4(c)). The adequate terminations for odd harmonic generation have been emphasized through the drain voltage distortion [Fig. 4(c)]. When a large input power is applied to swing the gate from pinchoff to zero gate voltage, the drain current waveform, shown in Fig. 4(b), presents a high peak of 75% $I_{\rm dss}$ for a brief period of the microwave signal. The signal trajectory observed in Fig. 4(a) corresponds to an optimized class B device's dynamic load line.

Looking to the time-domain waveforms $V_{\rm ds}(t)$ and $V_{\rm gs}(t)$, as well as to the dynamic load line, and by comparing these curves to the plots of G_m [Fig. 2(c)] and $G_{\rm ds}$ [Fig. 2(b)], we can see that during the drain voltage and gate voltage swing, $V_{\rm ds}$ from 2.3 to 3.8 V and $V_{\rm gs}$ from -1.7 to -0.2 V, $G_{\rm ds}$ is fairly constant while G_m varies within a large proportion. One can conclude that the dominant nonlinear source in the frequency multiplication, in the case of a tripler, is the transconductance.

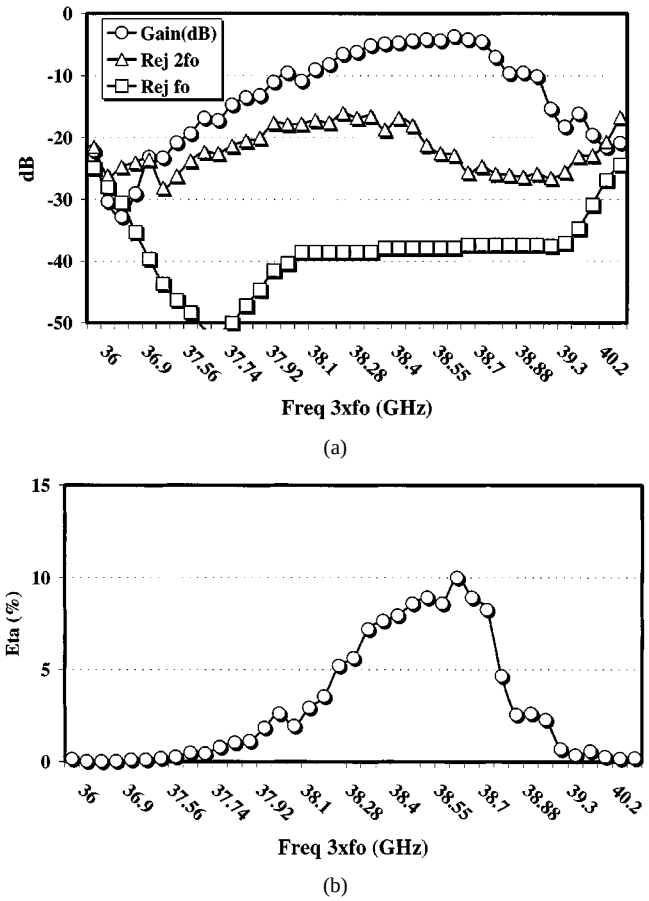


Fig. 7. Measured as a function of output frequency at fixed input power of 6.5 dBm: (a) Conversion gain and harmonic suppression, (b) Conversion efficiency.

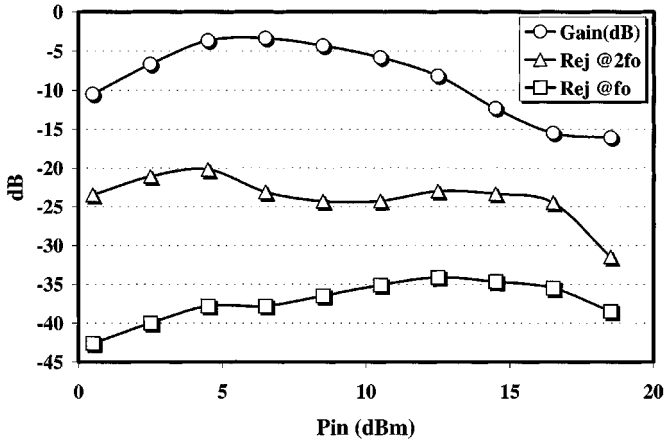
After finding the optimum source and load impedance at the fundamental and harmonic frequencies, a linear optimization was used to synthesize the input/output circuits. The tripler includes a double open stub at the output of the transistor for fundamental and second harmonic suppression. Additionally, the output of the device is optimally matched. The input networks have been designed to achieve the best compromise between conjugate matching at the fundamental frequency and terminating optimum reactive impedance for the second and third harmonic (Fig. 5).

All fabrication was carried out by Philips Microwave Limeil, France, on 100-μm substrates. Fig. 6 shows the chip photograph of the frequency tripler, which has an area of 1.5×2 mm^2.

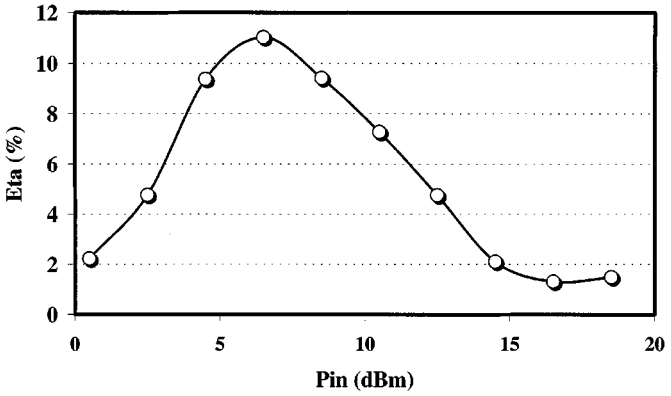
IV. Measured MMIC Performance

The circuit has been tested on-wafer using a measurement setup based on an HP83623B synthesizer and an HP8565E spectrum analyzer. For the phase noise characterization, the signal from the output of the tripler has been down-converted using a 4–40 GHz double balanced mixer and measured with an HP89441 vector spectrum analyzer [2].

To determine the optimum operating conditions, full characterization of the tripler has been performed versus frequency, input power level, and gate bias. The first experimental test shows in Fig. 7 the characteristics of the tripler versus frequency. The measurements were performed at a gate voltage of -0.7 V,

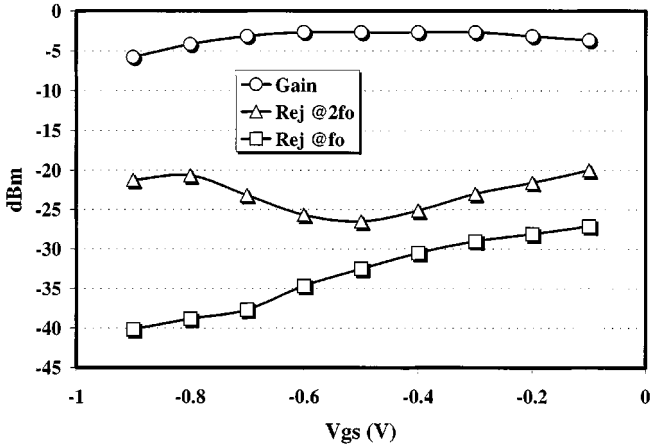


(a)

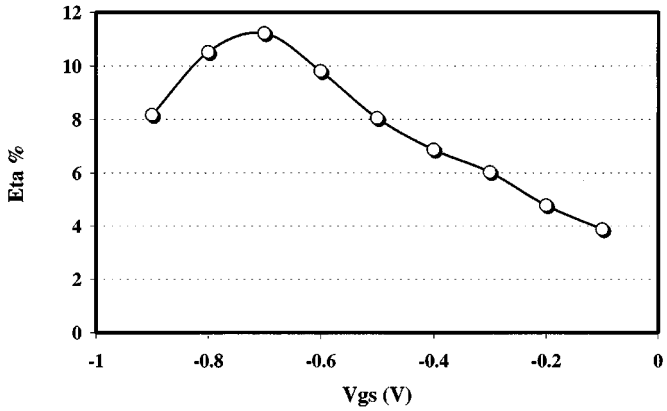


(b)

Fig. 8. Measured as a function of input power at fixed output frequency of 38.64 GHz: (a) conversion gain and harmonic suppression (b) conversion efficiency.



(a)



(b)

Fig. 9. Measured as a function of gate voltage at fixed input power of 6.5 dBm: (a) conversion gain and harmonic suppression (b) conversion efficiency.

a drain voltage of 3 V, and fixed input power of 6.5 dBm. The frequency tripler demonstrates a maximum output power of 3.1 dBm at 38.64 GHz, which relates to a conversion loss of 3.4 dB. The suppression of the second harmonic and the fundamental is 23 and 38 dB, respectively. The circuit achieves a 3-dB bandwidth of 1.4%, which is considerably high for a single-ended configuration. Fig. 7(a) shows also that the conversion loss is lower than 10 dB from 38 to 39 GHz. The maximum measured conversion efficiency is about 10% at 38.64 GHz [Fig. 7(b)].

The second experimental test shows on Fig. 8, the characteristics of the tripler versus input power. The measurements were performed at the same bias point as before and fixed third harmonic frequency of 38.64 GHz. The minimum measured conversion loss is 3.4 dB for 6.5 dBm input signal power. The circuit achieves rejections of 23 and 38 dB for the second harmonic and the fundamental, respectively (Fig. 8(a)). The maximum measured conversion efficiency is about 11% at 38.64 GHz for an input power level of 6.5 dBm (Fig. 8(b)). The latter defines the optimum operating condition of the frequency tripler. When the input power increases, the tripler achieves a saturated output power of 4.7 dBm with a conversion loss of 5.8 dB, while the conversion efficiency drops to 7%. Under these conditions, the tripler operates in an over-driven class B mode.

The third experimental test shows in Fig. 9 the characteristics of the tripler versus gate voltage. The measurements were performed at fixed input power of 6.5 dBm and 38.64 GHz output frequency. By varying the gate bias, the frequency tripler operated under different classes. From these curves, it is shown that an optimum of 27 dB for second harmonic suppression is reached at $V_{\rm gs} = -0.6$ V, for which the tripler achieved 3.8 dBm output power and 2.7 dB conversion loss [Fig. 9(a)]. The maximum conversion efficiency of 11% is only reached at the pinchoff voltage $V_{\rm gs} = -0.7$ V [Fig. 9(b)].

To draw the conclusions on the optimum operation mode of the frequency tripler, we have set a criterion for the comparison based on the dc power consumption. In Fig. 10, we compare the results of the three experimental tests performed as a function of frequency, input power, and gate bias versus the dissipated dc power. The optimum operating condition of the frequency tripler is then found at $P\_{\rm DC} = 14.7$ mW, for which the maximum conversion efficiency of 11% is reached [Fig. 10(e)]. This corresponds to an input power of 6.5 dBm and a gate bias close to the pinchoff. Finally, the experimental characterization, performed to find the optimum operating conditions of the tripler, validated the design methodology. We demonstrated for the first time that an active FET multiplier that uses a class B operation has resulted in good tripler operation in the millimeter wave.

Most of the published papers on active frequency multipliers have not treated the subject of phase noise degradation. Since phase noise is an important characteristic for frequency generation systems, especially when the specifications start to get very tight, we wanted to address this important topic here. Fig. 11

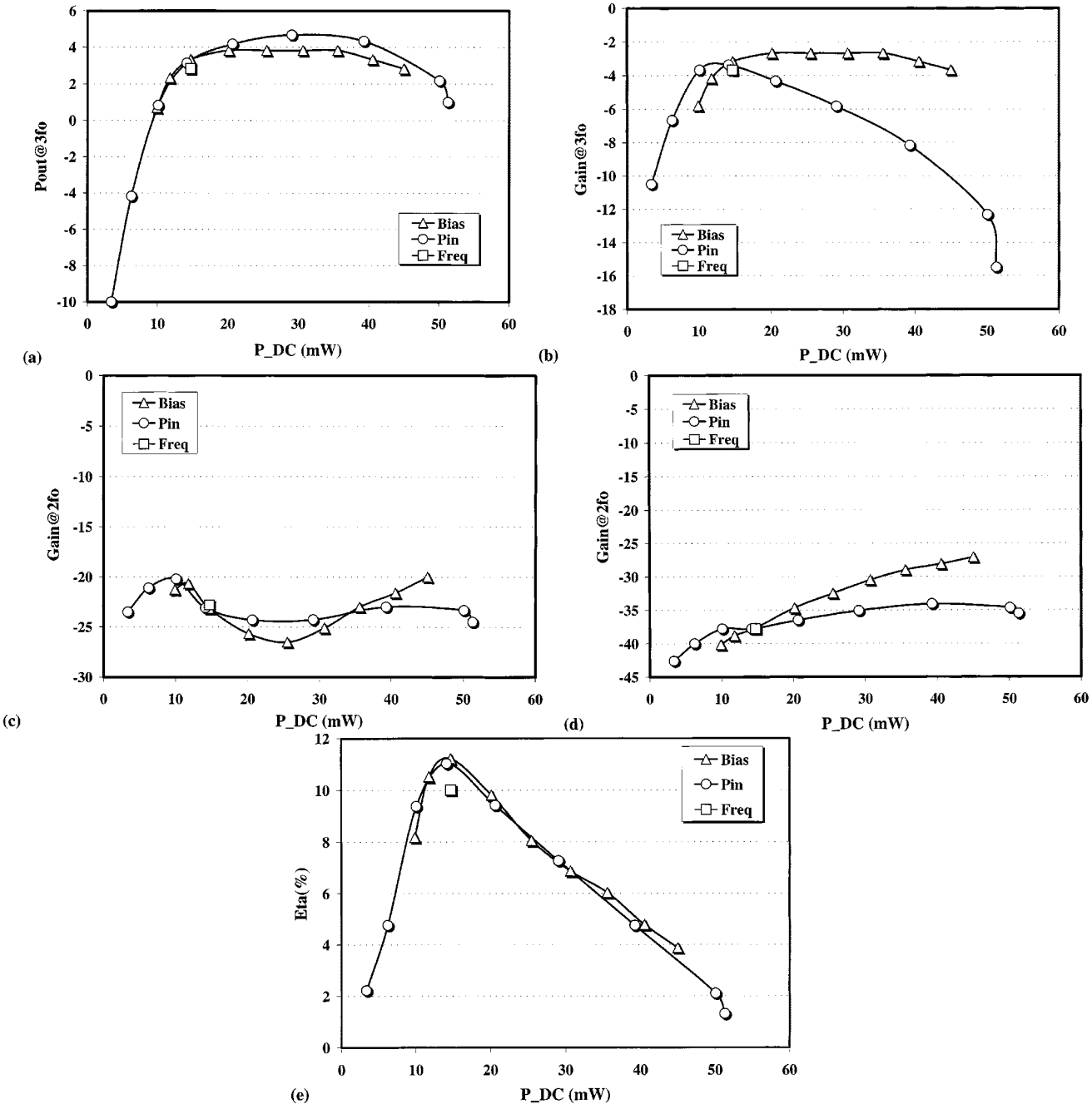


Fig. 10. Comparison of the three tests as a function of the dissipated dc power: (a) output power, (b) conversion gain, (c) second harmonic suppression, (d) fundamental suppression, and (e) conversion efficiency.

shows the measured phase noise degradation caused by the frequency tripler at 10- and 100-kHz frequency offsets from the carrier. The phase noise degradation given by $20 \cdot \log(N)$, where N is the multiplication order, is known to be the minimum degradation in an ideal frequency multiplier [5]. The reason for this characteristic is that a frequency multiplier is, in fact, a phase multiplier, so it multiplies the phase deviations as well as the frequency of the input signal. In the case of a frequency tripler, the theoretical value is 9.5 dB. The measured values are within 9 ± 1 dB. However, the degradation at10-kHz offset frequency increases when the input power is higher than 9.5 dBm, while the degradation at 100-kHz offset frequency seems not to be affected. The latter phenomenon has been studied by running different simulations for different levels of the transistor's $1/f$ noise. We found that the impact of the transistor's baseband noise on phase-noise degradation, due to the up-conversion process, has a stronger effect on an overdriven class B tripler.

V. Conclusion

An extensive treatment of a single-stage pHEMT frequency tripler has been described, focusing on the pinchoff device characteristic and drain voltage distortion as the primary multiplying mechanism. The class B mode of operation is believed to be preferable to other alternatives when it comes to achieving good conversion efficiency. Besides offering a comprehensive set of

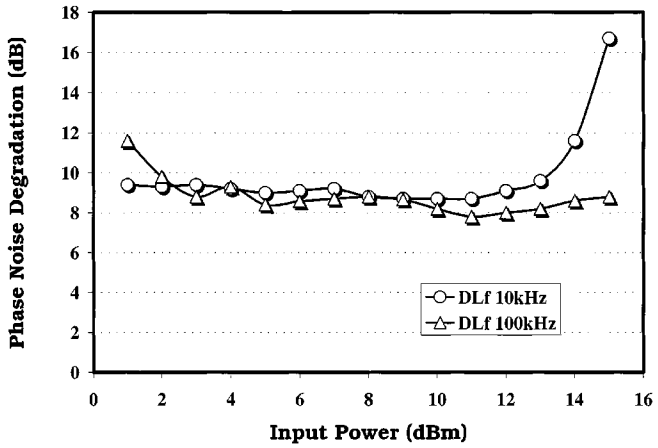


Fig. 11. Measured phase noise degradation as a function of input power at fixed output frequency of 38.64 GHz.

simulation results relative to a variety of different modes of operation, the study has above all demonstrated the important role that class of operation, voltage/current waveform optimization, and harmonic terminations together play in the performance of a frequency tripler. An active FET multiplier designed to function in class B has resulted in good tripler operation in the millimeter wave. The MMIC chip was developed and fabricated using the ED02AH pHEMT from Philips-PML technology. The circuit achieved the optimum operating conditions of 3.1 dBm output power level at 38.64 GHz, 3.4 dB conversion loss with 11% conversion efficiency, and a very low phase noise degradation of 9 $\pm$ 1 dB.

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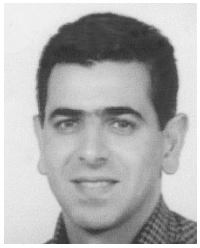
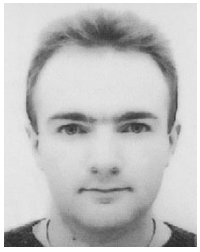


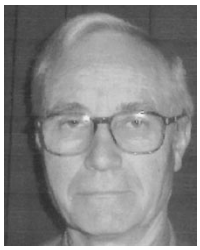
Ali Boudiaf (M'98) was born in Algiers, Algeria, in 1963. He received the B.Eng. degree in electronic engineering from the National Polytechnic School, Algiers, Algeria, in 1987, the M.Sc. degree in metrology and physic measurement systems from the National Institute of Metrology, Paris, France, and the Ph.D. degree in microelectronics and microwave systems from the University of Paris XI, Orsay, France, in 1989 and 1993, respectively.

From 1989 to 1993, he did his doctoral research at the France Telecom Research Center (CNET), Bagneux, France. He focused on microwave III–V semiconductor device characterization, noise modeling, and low-noise MMIC design. In 1993, he became an Assistant Professor in the Microwave Engineering Department at the Ecole Nationale Supérieure d'Electronique et de ses Applications, Cergy, France. In 1994, he accepted an Assistant Professorship at the University of Marne-la-Vallée, Noisy-le Grand, France. He worked on the development of new noise characterization techniques, HBT noise modeling, and the design of low-phase-noise MMIC VCO. He joined ATN-Microwave Inc., North Billerica, MA, in 1998. He is currently assigned to lead and guide the enhancement of device characterization products: noise parameter measurement systems NP5B, and load-pull measurement systems LP2. He is also in charge of development projects on LNA and balanced circuit characterization. He is the author of several technical papers and has received one patent. His current research interests include low-noise nonlinear circuit design and power amplifier characterization.



Didier Bachelet was born in Bourg-la-Reine, France, in 1972. He received the degree in electronics engineering from the University of Marne-la-Vallée, France, in 1996. He is currently pursuing the Ph.D. degree at the Laboratoire Systèmes de Communication, Marne-la-Vallée University.

His research focuses on the design of low-phase-noise frequency triplers.



Christian Rumelhard (M'83) received the electronic engineer degree in 1966 and the Dr.-Ing. degree from Paris VI University, Paris, France, in 1977.

He worked at Thomson CSF on the design of microwave tubes until 1969 and on the design of hybrid microwave integrated circuits until 1975. He then joined the Computer Science Division of Thomson to develop CAD algorithms and numerical models for the simulation of microwave circuits and devices. In 1980, he created an MMIC laboratory in the Central Research Laboratory of Thomson-CSF. In 1985, he was in charge of a design and characterization team in the Gallium Arsenide Department. In 1990, he went back to the Central Research Laboratory as a Senior Scientist. During this decade, tens of MMIC circuits were designed and characterized in his different teams. This activity resulted in many communications, contributions to four different books on microwave circuits, and three patents. In 1992, he became a Professor in Conservatoire National des Arts et Métiers, Paris, where he teaches and works on microwave and optoelectronic integrated circuits. There, he is responsible for the "Electronic, Systems and Metrology" research pole. He is Vice-President of the French chapter of MTT.