A Compact 5-Bit Phase-Shifter MMIC for K-Band Satellite Communication Systems

Charles F. Campbell and Steven A. Brown

***Abstract*—The design and performance of a compact K-band 5-bit phase-shifter monolithic microwave integrated circuit (MMIC) is presented. Extensive electromagnetic simulation and compact circuit design techniques were employed to yield an MMIC with a 1.693 mm $\times$ 0.750 mm (1.27 mm^2) die size. Measured performance of the phase shifter at 19 GHz demonstrates 5 dB$\pm$0.6 dB insertion loss and 3° rms phase error.**

***Index Terms*—Monolithic microwave integrated circuit (MMIC) phase shifters, phase shifters.**

I. Introduction

RECENTLY, several K-band commercial satellite systems have been proposed for high-speed data transmission. Many of these systems will utilize phased array antennas and may require tens of thousands of phase-shifter monolithic microwave integrated circuits (MMICs) per satellite. High-volume production of compact low-cost phase-shifter MMICs will be critical to the success of these programs. In this paper, the design and performance of a highly integrated K-band 5-bit phase shifter MMIC utilizing 0.25-μm pseudomorphic high electron mobility transistor (pHEMT) technology is discussed. The 0.25-μm pHEMT process was selected for its high switch figure-of-merit $\omega_\tau = 1/(R_{\rm on}C_{\rm off})$ and low pinchoff voltage (typically -1.0 V). At a control voltage of -2.5 V, TriQuint's 0.25-μm pHEMT switch field-effect transistor (FET) has a figure of merit of approximately 333 GHz. By comparison, TriQuint's implanted MESFET process has a 180-GHz switch figure of merit at a control voltage of -5.0 V and a typical pinchoff voltage of -3.0 V. The lower pinchoff voltage of the pHEMT process permits the utilization of control voltages as low as -2.5 V and will result in improved power handling capability for shunt devices. Use of the 0.25-μm pHEMT process also provides the opportunity for future integration of the phase-shifter function with other high-performance K-band components.

Employing extensive electromagnetic (EM) simulation and compact circuit design techniques yielded a MMIC that consumes only 1.27 mm^2 of GaAs real estate. The small size of this MMIC will not only reduce cost but will also enhance the level of integration for the higher level assemblies. A benchmark for compact phase-shifter MMICs is provided in [1]. A compact 1.29-mm^2, 4-bit, 11.7–12.7 GHz digital phase shifter is described, and it is claimed in [1] that the MMIC consumes only 30% of the die area of any other phase shifter previously reported. The circuit demonstrated 6-dB typical insertion loss and about $+7$° worst-case phase-shift error. Some notable work has also been published for K-band analog phase shifters. Hayashi and Muraguchi reported a compact (0.71 mm^2) analog phase-shifter MMIC with 2.2 dB $\pm$ 0.8 dB insertion loss that achieved approximately 124° of phase shift at 19 GHz for a 0 to -5 V control voltage range [2]. Nagra and York published results for a varactor diode loaded coplanar waveguide line analog phase shifter with 360° of phase shift at 20 GHz and 1.8–4.2 dB insertion loss variation over bias [3]. Die area was not reported, and a 0.0 to -10.0 V control voltage was required to achieve the full 360° of phase shift. Due to part-to-part variability, dc power consumption, and control voltage issues associated with analog designs, a digital phase-shifter solution is usually preferred for phased array applications.

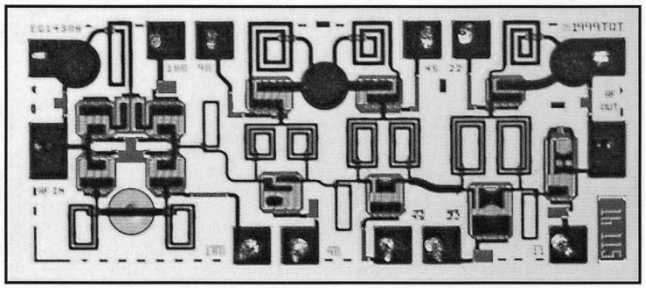

Fig. 1. Photograph of 5-bit phase shifter MMIC.

II. Circuit Design

A photograph of the fabricated 5-bit phase-shifter MMIC is shown in Fig. 1. The die size is 1.693 $\times$ 0.750 mm^2 and was achieved with the use of extensive EM simulation. All spiral inductors and connecting vias were EM simulated. The three spiral inductor pairs in the middle portion of the MMIC were each EM simulated as three-port networks. The 180° phase bit circuit at the far left of the photograph employs a widely utilized switched high-pass/low-pass design [1]. The 90°, 45°, and 22.5° phase bit topology is illustrated in Fig. 2. For reference state operation Q2 is pinched off and Q1 is turned on. Inductor Lp is sized to parallel resonate the off-state capacitance of Q2, which places the series combination of inductors L in parallel with the on-state resistance of Q1. As long as the reactance of the series inductors is large compared to the on-state resistance of Q1, the reference state may be modeled as a single series resistor. Therefore, the reference state has an insertion loss that is determined by the size of Q1 and effectively zero insertion phase. To activate the phase shift state, Q1 is pinched off and

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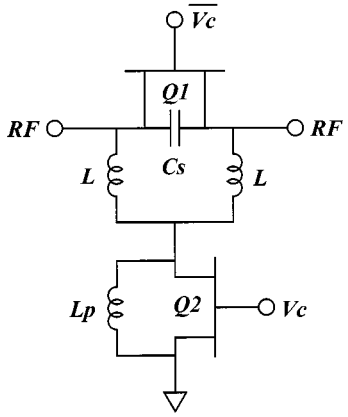

Fig. 2. 90°, 45°, and 22.5° phase bit topology.

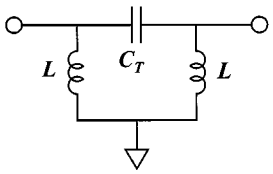

Fig. 3. Approximate 90°, 45°, and 22.5° phase state equivalent circuit.

Q2 is turned on, resulting in the approximate equivalent circuit shown in Fig. 3, where C_T is the parallel combination of C_s and the off-state capacitance of Q1. The nonzero on-state resistance of Q2 has a negligible effect on the insertion phase and impedance of the circuit. However, it will cause an insertion loss increase for the phase shift state.

Neglecting the on-state resistance of Q2, the transmission matrix for the phase shift state is given by (1). To satisfy the impedance matching condition ($S_{11} = S_{22} = 0$) at frequency ω, normalized matrix element B/Z_o must be equal to Z_oC. This equality relates the capacitance and inductance of the circuit as expressed in (2).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - \dfrac{1}{\omega^2 LC_T} & \dfrac{1}{j\omega C_T} \\ \dfrac{2}{j\omega L} - \dfrac{1}{j\omega^3 L^2 C_T} & 1 - \dfrac{1}{\omega^2 LC_T} \end{bmatrix} \quad (1)$$

$$C_T = C_s + C_{\text{Q1}}^{\text{off}} = \frac{L}{2Z_o^2} + \frac{1}{2\omega^2 L}. \quad (2)$$

andWith (2) satisfied, the inductance and capacitance required to realize insertion phase ϕ are approximately equal to the following:

$$L = \frac{Z_o}{\omega \tan(\phi/2)} \quad (3)$$

$$C_T = \frac{1}{\omega Z_o \sin\phi}. \quad (4)$$

Figs. 4 and 5 show the insertion loss, return loss, and phase shift versus frequency realizable using the ideal phase shift state topology shown in Fig. 3.

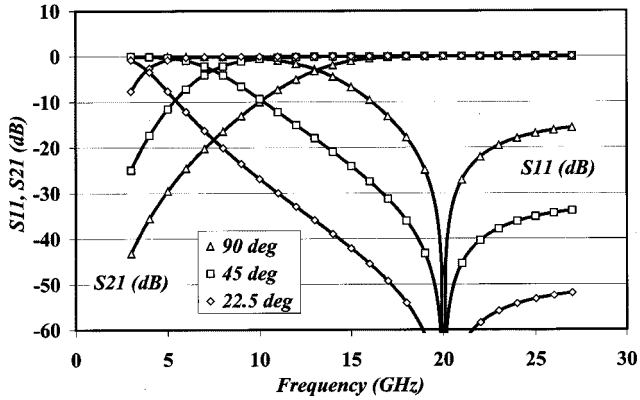

Fig. 4. Phase state insertion loss and return loss response of the ideal phase bit topology for a design frequency of 20 GHz.

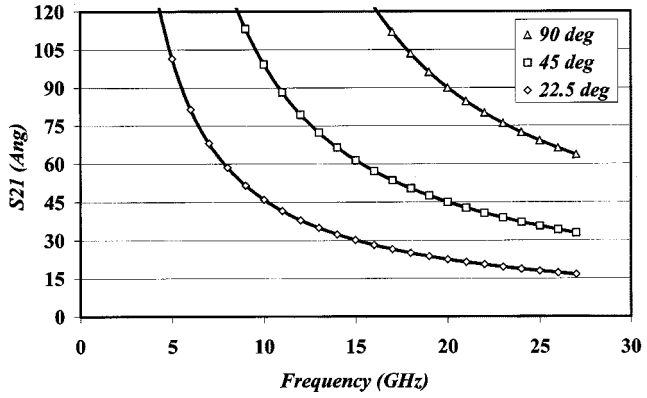

Fig. 5. Phase state phase response of the ideal phase bit topology for a design frequency of 20 GHz.

The impedance matching condition (2) places a constraint on the size of Q1 and sets the insertion loss for the circuit in the reference state

$$\text{IL}_{\text{REF}} = -20\log\left[\frac{\omega}{2\omega_\tau}\left(\frac{\sin\phi}{1 - \omega Z_o C_s \sin\phi}\right) + 1\right]. \quad (5)$$

The transistor figure of merit ω_τ determines the minimum realizable insertion loss in the reference state. The periphery of Q2 may be adjusted to equalize the insertion loss of the reference and phase states, as shown in Fig. 6. The phase shift is relatively insensitive to the parasitic resistances in Q1 and Q2. Fig. 7 shows the 90° bit response developed using the design equations (3) and (4), with and without the effect of parasitic resistance. An external capacitor C_s may be employed for additional adjustment of the reference-state insertion loss. This fixed capacitance reduces the periphery of Q1 required to satisfy (2) and decreases the phase shift dependence on bias, at the expense of increased insertion loss. As Q2 should be adjusted to equalize the insertion loss between the reference and phase states, higher insertion loss in the reference state reduces the periphery required for Q2 and the die area consumed by the phase bit.

The 11.25° phase bit can be viewed as a limiting case of the circuit in Fig. 2, where the inductances L have become large enough that they can be removed from the circuit, leaving only

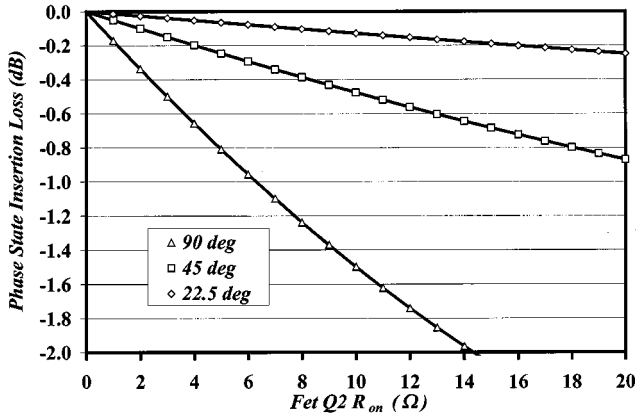

Fig. 6. Phase shift state insertion loss as a function of the on-state resistance of Q2.

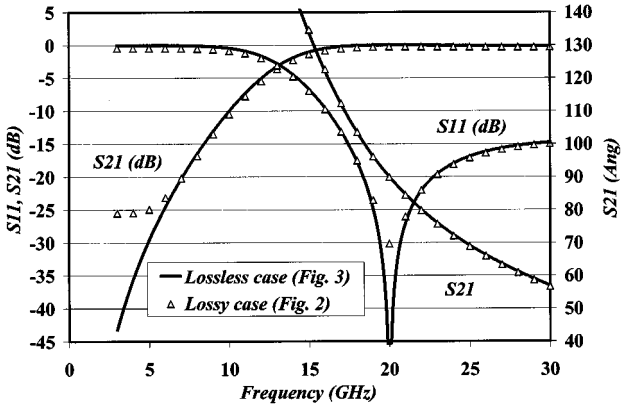

Fig. 7. Effect of including parasitic resistance on the phase shift response of the 90° bit.

Q1 and C_s. The circuit is no longer impedance matched and is practical only for small amounts of phase shift. The total capacitance required to realize a given phase shift and the associated return loss is given by

$$C_T = C_s + C_{\mathrm{Q1}}^{\mathrm{off}} = \frac{1}{2\omega Z_o \tan\phi} \tag{6}$$

and

$$RL = 20\log(\sin\phi). \tag{7}$$

III. Measured Results

The fabricated devices were characterized in-fixture at room temperature. Measured 17–21 GHz circuit performance is plotted in Figs. 8 and 9 for all 32 phase states at a control voltage of −5.0 V. The typical insertion loss was observed to be less than 6 dB over the measured frequency band and 5.0 dB ± 0.6 dB at 19 GHz. The measured return loss showed significant state-to-state variation with worst-case results of 8.6 and 7.2 dB at the input and output ports, respectively. Over the 17 to 21 GHz band, the worst-case phase-shift error varied between −8° and +5°.

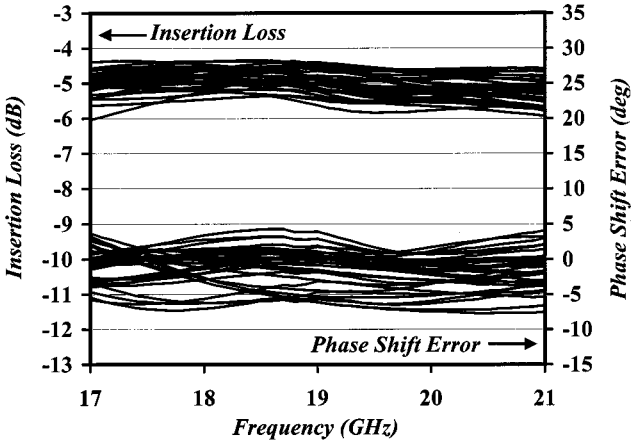

Fig. 8. Measured 32-state insertion loss and phase shift error for a −5.0 V control voltage.

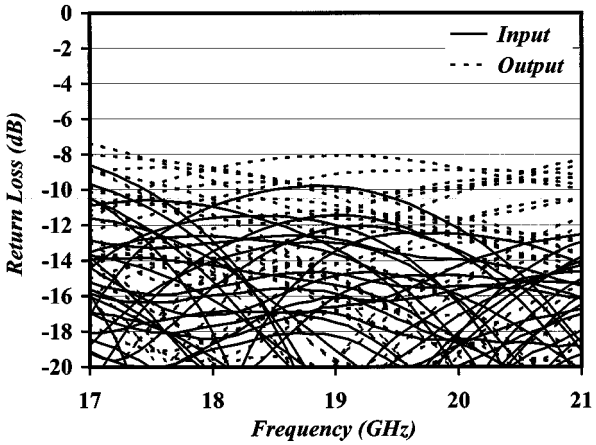

Fig. 9. Measured 32-state return loss for a −5.0 V control voltage.

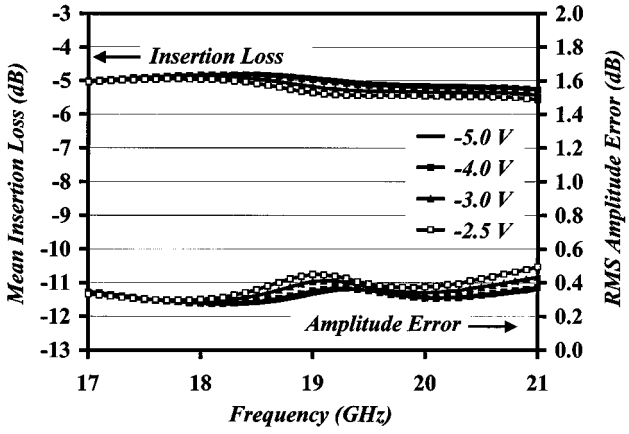

Fig. 10. Mean insertion loss and rms amplitude error versus control voltage.

The circuit topologies utilized for this design exhibit good tolerance to control voltage variation. The insertion loss averaged over 32 phase states and the corresponding root mean square (RMS) amplitude error are plotted in Fig. 10 for control voltages ranging from −5.0 to −2.5 V. The rms/peak phase shift error

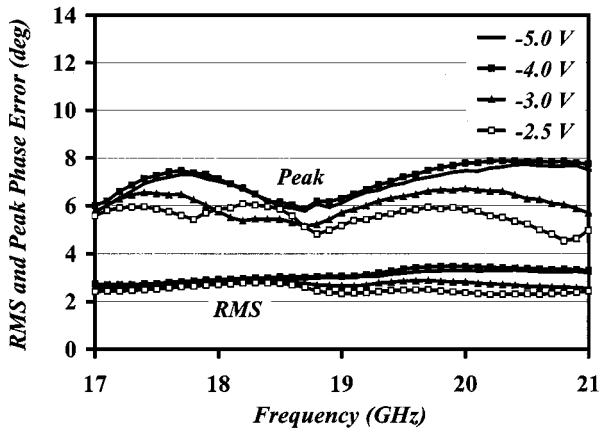

Fig. 11. RMS and peak phase shift error versus control voltage.

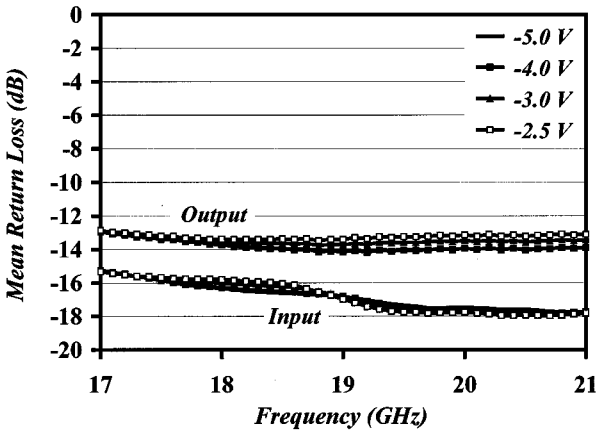

Fig. 12. Mean input and output return loss versus control voltage.

TABLE I
TYPICAL −5.0 V PERFORMANCE AND MAXIMUM VARIATION OVER THE −5.0 TO −2.5 V CONTROL VOLTAGE RANGE

Parameter	*Unit*	*Typical*	*Variation*
Mean Insertion Loss	dB	-5.0	0.5
RMS Amplitude Error	dB	0.32	0.13
Peak Amplitude Error	dB	0.61	0.22
RMS Phase Shift Error	deg	3.0	1.2
Peak Phase Shift Error	deg	6.9	3.3
Mean Input Return Loss	dB	-16.8	0.4
Max Input Return Loss	dB	-10.9	1.4
Mean Output Return Loss	dB	-13.8	0.9
Max Output Return Loss	dB	-8.4	1.1

and the mean input/output return loss are plotted in Figs. 11 and 12, respectively, for the same control voltage range. The measured typical −5.0 V results and maximum observed variation over bias voltage are summarized in Table I. Figs. 13–15 show the variation in phase shift and insertion loss for a typical production lot. The observed standard deviation of the phase shift, state 0 insertion loss, and state 31 insertion loss for the 4703 device sample were 1.2°, 0.08 dB, and 0.08 dB, respectively.

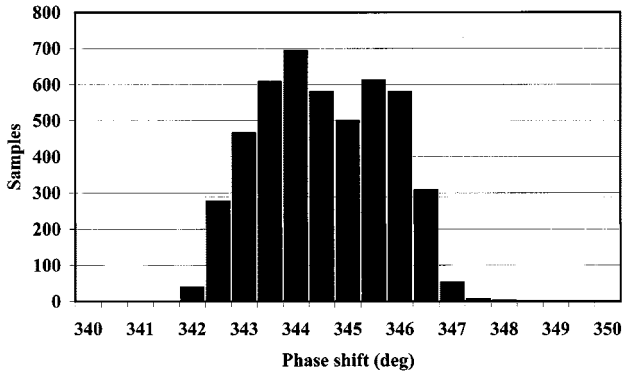

Fig. 13. Phase shift distribution on a typical production lot at 19 GHz, −2.5 V bias, state 31.

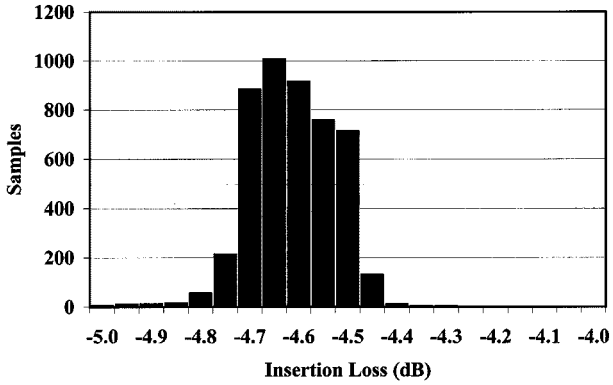

Fig. 14. Insertion loss distribution on a typical production lot at 19 GHz, −2.5 V bias, state 0.

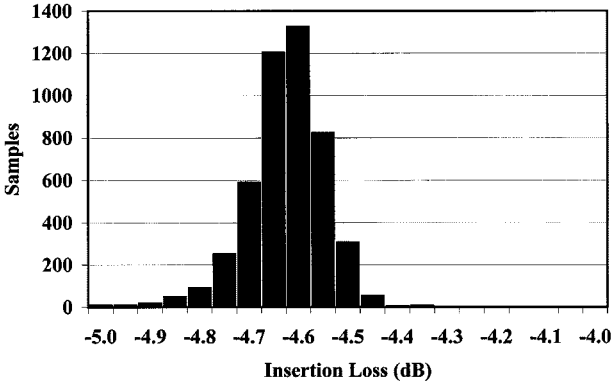

Fig. 15. Insertion loss distribution on a typical production lot at 19 GHz, −2.5 V bias, state 31.

IV. CONCLUSIONS

The design and performance of a 5-bit K-band phase-shifter MMIC has been reported. Compact circuit topologies and extensive EM simulation were utilized to realize with a MMIC with 1.27 mm^2 die area. Measured results for the circuit demonstrate a typical 5.0 dB $\pm$ 0.6 dB insertion loss and 3.0° rms phase-shift error at 19 GHz. The design also exhibited good tolerance to

supply-voltage variation. For a control voltage range of −2.5 to −5.0 V, the worst case observed change for the mean insertion loss and rms phase shift error was 0.5 dB and 1.2°, respectively. The insertion loss and die area for this MMIC are believed to be among the lowest reported for a monolithic 5-bit digital phase shifter at 19 GHz.

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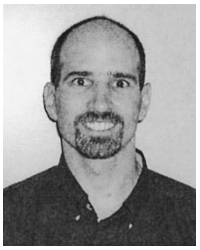

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From 1993 to 1998, he was with Texas Instruments, Dallas, where he was involved with MMIC development and design. Since 1998, he has been the Lead Engineer for the space products business segment of the Texas division of TriQuint Semiconductor. His interests are compact, high-power MMIC design techniques and device modeling.

Steven A. Brown was born in New York, NY, in 1967. He received the B.S. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1988 and the M.S.E.E. degree from the University of Michigan at Ann Arbor in 1990.

From 1990 to 1996, he served on active duty with the U.S. Air Force. In 1996, he joined Texas Instruments, Dallas, as an MMIC designer. Since 1998, he has been with the Space Products Group of TriQuint Semiconductor, Dallas, TX. His interests include the development of high-power compact amplifiers for millimeter-wave applications.