Tuning Analysis for the High-Q Class-E Power Amplifier

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***Abstract*—The effects of component variations on a high-Q class-E amplifier are simulated and measured. Design equations are provided for the case of a 50% duty cycle with B at its optimum value for a given R. Six distinct operating points are analyzed for the output network. The problem of tuning a high-Q class-E amplifier is addressed. Normally, it cannot be tuned for maximum output power without degrading efficiency. An auxiliary circuit is added to the design so that it can be tuned for maximum output power in order to achieve optimum efficiency. Measured data are obtained at low frequencies for an amplifier with a loaded Q of 340.**

***Index Terms*—Class-E, high efficiency, high Q, Litz wire, low frequency, Q-factor, tunable amplifiers.**

I. Introduction

THE CLASS-E power amplifier [1]–[5] is being used in a greater variety of applications, extending into the microwave region [6], [7]. Tuning it is a sometimes difficult and confusing task because maximum output power and maximum efficiency occur at different operating points [3], [8]. High-Q circuits must be tuned initially to account for part tolerances. They must also be tuned periodically to account for load variation and component aging.

The class-E amplifier (Fig. 1) is a switched-mode circuit capable of amplifying a phase-modulated constant-envelope RF carrier. It consists of an active device operated as a switch [1]. Radio-frequency (RF) choke $L1$ is charged magnetically when the switch is on. When the switch is off, this energy is released into the shunt capacitance and the series output network consisting of $L2$, $C2$, and R. For the case of *optimum class-E operation*, no energy is dissipated in the field-effect transistor (FET) (ideally), and the power amplifier is 100% efficient [1]–[3]. This requires the drain voltage to return to zero with a slope of zero at the moment the FET is turned on. If the carrier frequency or any of the component values are varied from their optimum design values, the circuit becomes *suboptimum* [5]. This usually implies operation at a desired operating point with less than optimum efficiency, although 100% is possible under certain conditions.

A review of the literature suggests that a detailed analysis of output network tuning, for the popular case of a 50% switch duty cycle, could clarify the power-efficiency interaction and serve as a design guideline. This paper seeks to provide this information by analyzing six distinct operating points for the class-E amplifier:

maximum efficiency at rated power (optimum);
"peak-tuning" for maximum output power;
series resonance of the output network $(jX = 0)$;
maximum efficiency at reduced output power;
maximum dc input power;
maximum power dissipation in the switch.

In addition, this paper provides circuit design equations for the case of optimum operation. Simulation and measured data are shown using a circuit with a loaded Q of 340. Tuning strategies are discussed and equations are derived to predict power, efficiency, dc-input resistance, and phase angle, depending upon the load ratio X/R at the output. An auxiliary tuning circuit is described to allow the class-E amplifier to be peak-tuned for maximum output power in order to achieve optimum operation, in effect, a unification of points "A" and "B."

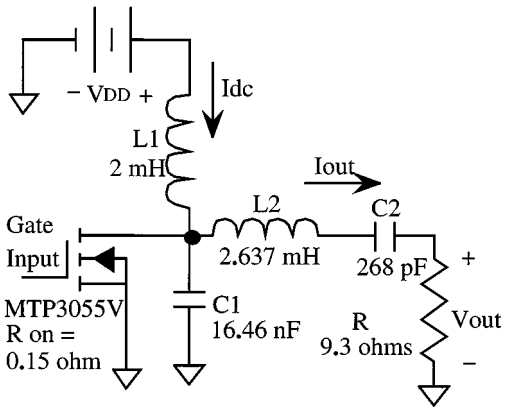

Fig. 1. Class-E amplifier with a loaded Q of 340 at 189.700 kHz.

II. Design Equations for Optimum Operation

As a foundation for the analysis, the optimum design equations can be determined for the high-Q class-E amplifier from [2] and [3] by assuming 100% efficiency and a 50% duty cycle for the square-wave input signal. $P_{\rm in}$ and $P_{\rm out}$ are the input and output powers, $V_{\rm DD}$ is the dc supply voltage, $I_{\rm dc}$ is the dc supply current, $I_{\rm out}$ is the magnitude of the rms current into R, $V_{\rm out}$ is the magnitude of the rms voltage across R, and ω_0 is the operating frequency. Ideally, for a given power and load resistance, $V_{\rm out}$ and $I_{\rm out}$ are determined using

$$P_{\rm in} = P_{\rm out} = I_{\rm out}^2 R = V_{\rm out}^2/R. \tag{1}$$

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If the desired load termination has a reactive component, its reactance must be combined into either $L2$ or $C2$, for the purpose of calculating component values. Furthermore, R includes any resistive losses associated with $L2$ and $C2$. The required supply voltage and current are found using

$$V_{\rm DD} = V_{\rm out}\sqrt{\frac{1}{2}+\frac{\pi^2}{8}} \tag{2}$$

and

$$I_{\rm dc} = P_{\rm in}/V_{\rm DD}. \tag{3}$$

The next step is to compute shunt capacitor $C1$ using

$$C1 = \frac{2}{\pi(1+\pi^2/4)\omega_0 R} - C_{\rm DS}. \tag{4}$$

The drain-to-source capacitance $C_{\rm DS}$ of the FET is absorbed into the value of $C1$. This compensates for the switch capacitance and makes it part of the overall circuit. During optimum operation, $C1$ will see no more than $3.56V_{\rm DD}$ V peak across it [2], [4]. This agrees with the simulation to within 0.2%, and with the measured data to within 3.9%. For the optimum-tuned case, it is the maximum voltage to which the switch is exposed. The peak switch current is 2.86 $I_{\rm dc}$, which agrees with the simulation to within 0.4%.

If either $L2$ or $C2$ is predetermined for a given application, the designer must accept the value for the loaded Q that this imposes on the circuit. Otherwise, Q can be chosen based on the tradeoff between efficiency and harmonic suppression. The impact to efficiency occurs because a high loaded Q implies a large reactance in the output network. A large inductive reactance inevitably has a nonnegligible resistance associated with it. Although this resistance is lumped in with the load resistance for the purpose of calculation, it forms a resistive divider with the actual load resistance, and efficiency is reduced accordingly.

For many low-frequency transmitter applications, the values for R and $C2$ are predetermined. Therefore, the value for $L2$ must be calculated using

$$L2 = \frac{1}{\omega_0^2 C2} + \frac{\pi}{4}\left(\frac{\pi^2}{4}-1\right)\frac{R}{\omega_0}. \tag{5a}$$

For the case where $L2$ is the fixed component, $C2$ can be determined using

$$C2 = \left[\omega_0^2 L2 - \frac{\pi}{4}\left(\frac{\pi^2}{4}-1\right)\omega_0 R\right]^{-1}. \tag{5b}$$

It is obvious from an examination of (5a) that the series combination of $L2$ and $C2$ does not go resonant at the center frequency ω_0.

The value of $L1$ is not critical. It should have a reactance of at least ten times the RF load resistance ($L1 \geq 10R/\omega_0$). $L1$ has an effect on the carrier envelope attack and decay times for an amplifier driven with on–off keyed or binary phase-shift keying (BPSK) modulation. Note that during BPSK phase reversals, $L1$ has a dominant effect on transient thermal stresses in the FET.

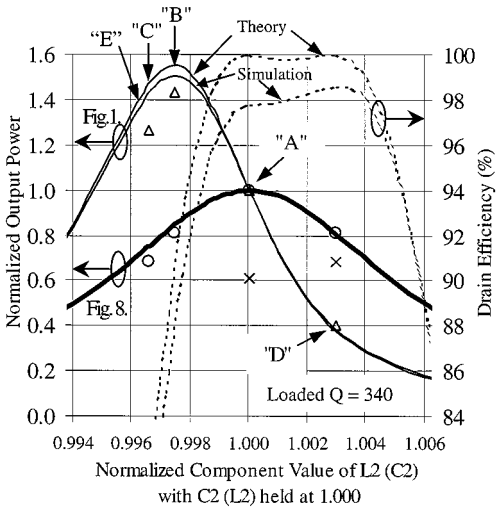

Fig. 2. Output power and efficiency versus output network tuning for the circuits shown in Figs. 1 and 8.

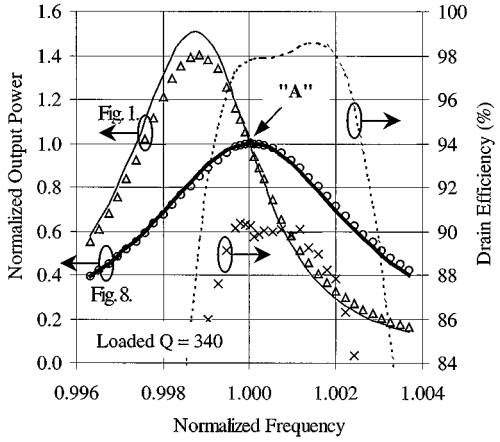

Fig. 3. Output power and efficiency versus frequency.

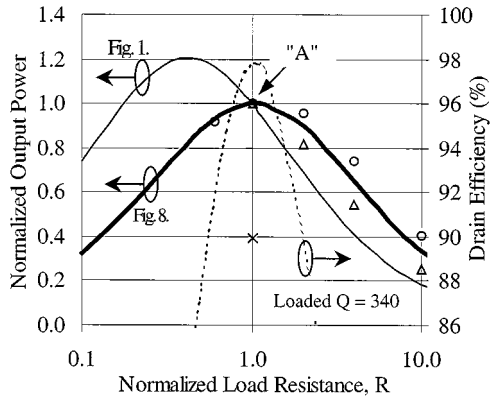

Fig. 4. Output power and efficiency with variation in R, the RF load.

III. Amplifier Characteristics

Optimum operation does not coincide with the operating point for maximum input or output power; therefore, the circuit cannot be tuned in the classic manner (peak-tuned) without degrading efficiency. This is illustrated by the results of several PSPICE simulations, as shown in Figs. 2–5. Simulation data (lines) and circuit measurements (data points) are shown

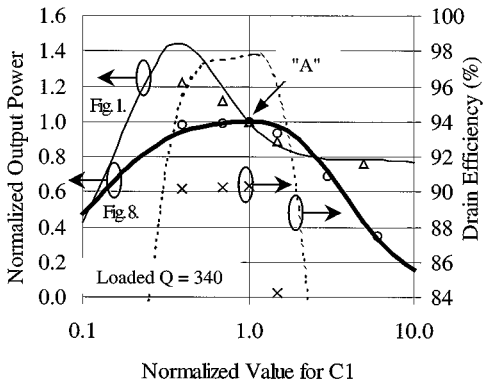

Fig. 5. Output power and efficiency with variation in $C1$, the shunt capacitor.

on these graphs. The circuit implementation is discussed in Section VII.

A. Variation of Output Network Component Values

Normalized output power and efficiency are shown in Fig. 2 versus a ($\pm$0.6% adjustment in the value of $L2$ ($C2$). The intent is to show the result of "tweaking" a component value to tune the circuit. An optimal design using the circuit shown in Fig. 1 places the operating point at "A." If this circuit is tuned by adjusting $L2$, the variation causes the output power to vary along the thin-solid line.

A "peak" adjustment places the operating point at "B." The normalized value of $L2$ (0.9975) for maximum output power is slightly less inductive than the design value (1.000) for optimum operation. Point "B" results in a simulated efficiency of only 88%. This lost power is dissipated in the FET at turn-on. Note that the output power increases to 150% of the original design value, and the power dissipated in the FET increases by almost an *order of magnitude*. This has a significant impact on the design of the heatsink at high power levels.

There are other points of interest associated with output network tuning. The series-resonance point occurs at "C" (not at "B"), where $jX = jX_{L2} - jX_{C2} = 0$. Another point of interest occurs at "D," where the efficiency is maximum again, but the output power drops to 40% of the intended design value. Tuning to point "E" results in maximum dc input power and reduced efficiency.

B. Variation with Operating Frequency

The effects of frequency variation are shown in Fig. 3. Off-centered power peaking is observed, with some similarity to Fig. 2. A frequency shift alters the net reactance of both $L2$ and $C2$. This has a compounded effect on the net reactance compared to an adjustment of $L2$ alone. The measured data for the circuit of Fig. 1 track the simulation data over most of the region shown, except in the vicinity of peak output power. This power slump may be due to corona losses in the output network, where the voltage across $C2$ (or $L2$) climbs to 1700 V peak for a 1-W amplifier. This suggests further study using a vacuum capacitor.

It is accepted practice with class-E circuits to consider the ratio of the output network reactance (choose, say, the inductor's reactance) to the load resistance as the definition for circuit Q. Hence the circuit of Fig. 1 has a loaded Q of 340. Ambiguity exists if the 3-dB bandwidth is used to calculate Q, because the circuit does not peak around its center frequency. (If $Q_{3\,\mathrm{dB}}$ is calculated about the peak, a value of 270 is obtained.) The X_{L2}/R definition for Q is the better choice because it can be used to estimate harmonic content at the output. For example, the second harmonic can be predicted [1] using $-20\log(2X_{L2}/R)$ with respect to the fundamental. This agrees with the measured data to within 0.2 dB.

C. Variation of RF Load Resistance

The effects of a variation in the RF load resistance are shown in Fig. 4. When the data are plotted on a log-scale, the same power-peaking effect can be seen as R is reduced. The efficiency curve shows a peaking characteristic about the intended design value as expected.

D. Variation of Shunt Capacitance

A variation in the value of $C1$ also shows a similar power-peaking effect when plotted on a log-scale. This is shown in Fig. 5.

IV. Tuning Analysis

A. Tuning Techniques

Given the sensitivity of the circuit to variations in the output network, the question is how to tune it properly. The easiest technique is to peak-tune the output power (by peaking the output current), but this has undesirable effects. Another method is direct measurement and adjustment of the output network, but this is not practical for a high-Q circuit. It is difficult to measure $L2$ and $C2$ with sufficient accuracy due to circuit and measurement parasitics. Another approach is to calculate efficiency while the circuit is being tuned. This "efficiency-meter" technique has limited appeal because the output power may not be directly measurable. For instance, a portion of the output circuit may be part of an antenna or embedded structure. It is a simple matter to monitor the output current with a suitable detector, but it may not be possible to measure the output voltage. Nevertheless, a peak in the efficiency curve *can* be found using this method.

Phase measurements can also be used for tuning. It is relatively easy to measure the phase at low-impedance nodes within the circuit. If a relationship can be exploited between the phase of the voltage across $C1$ and the phase of the output current (or output voltage), this information can be used to tune the circuit and predict performance. This section extends the analysis presented in [3]. A broad range of duty cycles is possible for high-efficiency operation, but only the case of a 50% duty cycle ($y = \pi/2$) will be addressed here. This is optimal from a switch stress standpoint [2] and simplifies the analysis. The waveforms and phase relationships used for class-E analysis are shown in Fig. 6.

B. Development of Equations

The analysis begins by defining several terms and equations. The goal is to analyze the impact of *detuning* the circuit from optimum conditions. The following assumptions apply.

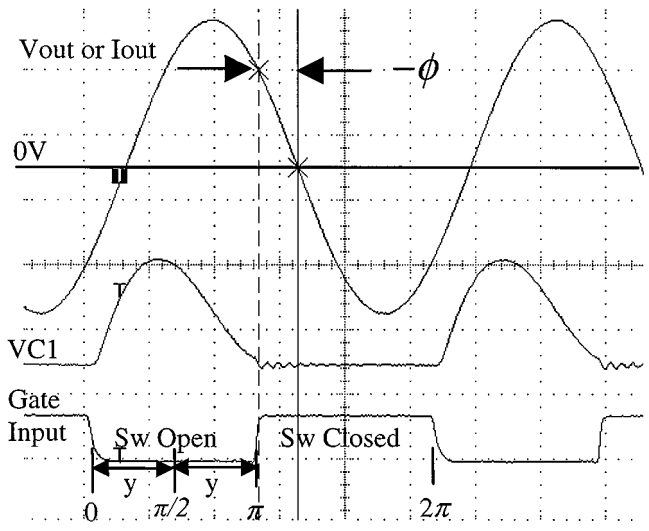

Fig. 6. Class-E waveforms used to define y and ϕ.

1) RF choke $L1$ is large so that a constant dc current with negligible ripple flows through it at all times.
2) The switching behavior of the FET is ideal and lossless (except at turn-on when $C1$ is discharged during suboptimum operation). The FET can handle negative voltages and currents.
3) The loaded Q of the output network is high enough to suppress harmonic currents; that is, $I_{\rm out}$ is essentially a sinusoid at the RF carrier frequency.
4) The circuit is operated at or below the critical frequency [5], where $C_{\rm DS}$ makes up all of the shunt capacitance.
5) All network components are passive, linear, time-invariant, and ideal without parasitics.

The output network does not operate at resonance in general, so the difference term $X = X_{L2} - X_{C2}$ is used. A load angle term $\psi = \arctan(X/R)$ is defined for mathematical convenience. A magnitude term is also defined

$$\rho = \sqrt{1 + (X^2/R^2)} = \sec\psi \tag{6}$$

The shunt capacitance is expressed more conveniently in terms of its susceptance: $B = \omega_0(C1 + C_{\rm DS})$. Throughout this analysis, R and B are *fixed* at their given and optimum design values, respectively. Using (4), the expression for B can be written in terms of the RF load resistance as

$$B_{\rm opt} = \frac{2}{\pi(1+\pi^2/4)R}. \tag{7}$$

The analysis in [2] and [3] derives an expression g. It represents the ratio of the peak-ac output current to the dc supply current. The expression for g can be simplified considerably for the case of a 50% duty cycle. In defining this term, $R_{\rm dc}$ is the dc input resistance looking into $L1$. The simplified expression for g is

$$\begin{aligned} g(y=\pi/2,\phi,\psi) &= \frac{\sqrt{2}\,I_{\rm out}}{I_{\rm dc}} = \frac{\sqrt{2}\,V_{\rm out}}{R}\,\frac{R_{\rm dc}}{V_{\rm DD}} \\ &= \frac{\pi\sin(\phi+\psi) + 2\cos(\phi+\psi)}{2\cos\phi\sin(\phi+\psi) + (\pi/2)\cos\psi}. \end{aligned} \tag{8}$$

The analysis by Raab also derives a second expression h that is equal to the same ratio. This can be simplified in the same manner

$$\begin{aligned} h(y=\pi/2,\phi,\psi,B,R,\rho) &= \frac{\sqrt{2}\,V_{\rm out}}{R}\,\frac{R_{\rm dc}}{V_{\rm DD}} \\ &= \frac{\pi\cos(\phi+\psi) - 2\sin(\phi+\psi)}{\pi BR\rho - (\pi/2)\sin\psi + 2\cos\phi\cos(\phi+\psi)} \end{aligned} \tag{9}$$

Using (6) and (7), this becomes

$$\begin{aligned} h(y=\pi/2,\phi,\psi) &= \frac{\pi\cos(\phi+\psi) - 2\sin(\phi+\psi)}{\dfrac{8\sec\psi}{(4+\pi^2)} - \dfrac{\pi}{2}\sin\psi + 2\cos\phi\cos(\phi+\psi)}. \end{aligned} \tag{10}$$

From the same analysis, the dc input resistance can be found and rewritten using (7) as

$$\begin{aligned} R_{\rm dc}(y=\pi/2,\phi,g,R) &= \left(\frac{\pi^2}{8} - \frac{\pi}{4}g\cos\phi - \frac{1}{2}g\sin\phi\right)\left(1+\frac{\pi^2}{4}\right)R. \end{aligned} \tag{11}$$

Since g and h are equivalent, it is necessary to set them equal to each other and attempt to solve for ϕ as a function of ψ

$$\begin{aligned} \frac{\pi\sin(\phi+\psi) + 2\cos(\phi+\psi)}{2\cos\phi\sin(\phi+\psi) + (\pi/2)\cos\psi} &= \frac{\pi\cos(\phi+\psi) - 2\sin(\phi+\psi)}{\dfrac{8\sec\psi}{(4+\pi^2)} - \dfrac{\pi}{2}\sin\psi + 2\cos\phi\cos(\phi+\psi)} \end{aligned} \tag{12}$$

This equation can be solved graphically by plotting the intersection of both sides as a function of ϕ for a given ψ using a mathematics package for the PC. An analytical solution involving a cubic equation in $\tan\phi$ may also be pursued as described in [3] and [4]. Fortunately, with $y = \pi/2$, it is possible to obtain an exact closed-form solution

$$\phi(\psi) = \arctan\left(\frac{\pi}{2} - \frac{32+8\pi^2}{\pi^3 + 12\pi - 16\tan\psi}\right). \tag{13}$$

This function is periodic in π and is shown in Fig. 7. It can be used with (8) to calculate g. It can also be used with (11) and (8) to calculate $R_{\rm dc}/R$. Typically, ψ is located in the first quadrant of arctan (X/R) and ϕ is a negative number. The proper choice of ϕ from (13) can be confirmed with (8) if it produces a positive number for g.

The input and output powers are

$$P_{\rm in}(\psi, V_{\rm DD}, R) = V_{\rm DD}^2/R_{\rm dc} \tag{14}$$

and

$$P_{\rm out}(\psi, V_{\rm DD}, R) = \frac{g^2 R V_{\rm DD}^2}{2R_{\rm dc}^2}. \tag{15}$$

The drain efficiency can be calculated with

$$\eta(\psi) = \frac{P_{\rm out}}{P_{\rm in}} = \frac{g^2}{2}\,\frac{R}{R_{\rm dc}}. \tag{16}$$

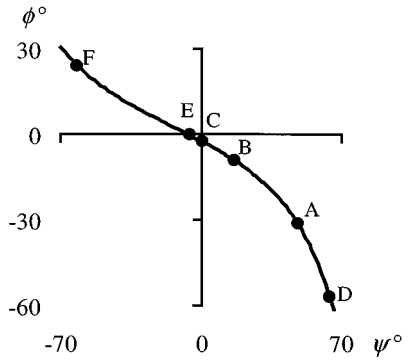

Fig. 7. Plot of ϕ versus ψ for $y = \pi/2$ and $B = B_{\rm opt}$.

C. Analytical Determination of Operating Points

Starting with point "A" (optimum operation), it has been shown [2] that ϕ is equal to $\arctan(-2/\pi) \cong -32.482°$ and $\psi = \arctan[(\pi^2/2 - 2)(\pi/8)] \cong 49.052°$. Had this not been established already, it is a straightforward matter to take the derivative of (16) with respect to ψ and set it equal to zero. A root-finder program can then be used to determine the desired answer, as there is more than one solution in the region of interest.

For point "B" (peak tuning), the derivative of (15) is determined with respect to ψ and set equal to zero. This task can be simplified by recognizing that the derivative of $g/R_{\rm dc}$ will suffice. Based on the simulation data, an initial estimate of $X/R = 0.303$ ($\psi = 16.9°$) is used, where $L2$ was 0.9975 of its optimum design value. The actual value for ψ was found to be 16.3467°.

Point "C" (series resonance) corresponds to $X/R = 0$. For point "D" (maximum efficiency at reduced output power), the procedure is similar to the approach for point "A." An estimate of $X/R = 2.171$ ($\psi = 65.3°$) is used. The actual value for ψ was found to be 64.3948°. A plot of (16) shows a theoretical efficiency of 100% for "A" and "D" (see Fig. 2). The slightly skewed response for the simulation curve is due to the use of a nonideal switch with $R_{\rm DSon} = 0.15\ \Omega$.

V. Results

The choice of load ratio (X/R) is independent of the choice for loaded Q (X_{L2}/R). Loaded Q does not play a direct role in the magnitude of the power-peaking effects observed in Figs. 2–5 or the values shown in Table I. Therefore, regardless of circuit Q, a class-E circuit that is peak-tuned will exhibit a theoretical increase in output power level to 1.55 of the original design value and a drop in efficiency to 90.7%. The wasted power will be dissipated in the FET. This assumes that the circuit Q is high enough to justify the assumption of sinusoidal load current without significant harmonic content. For the plots shown in Figs. 2 and 3, the loaded Q of the circuit merely scales the abscissa without affecting the ordinate axis.

There are two other operating regions of interest. Maximum input power (point "E") occurs when the output network is tuned to $X/R = -0.120\,75$ ($\psi = -6.88515°$, $\phi = 0°$), which is slightly capacitive. The input and output power levels become 1.81 and 1.41 of the original design values, respectively. The efficiency is 77.6%.

TABLE I
Parameters for Four Tuning Conditions

Parameter		Class-E OUTPUT NETWORK TUNING "C" Series-Resonance	"B" Peak-Tuning	"A" Optimum	"D" Max Eff at Reduced Pwr
Efficiency	Theoretical	81.8%	90.7%	100%	100%
	Simulation	79.4%	88.2%	97.8%	98.5%
	Implemented	65.6%	80.7%	90.1%	90.8%
Output Power (watts)	Theoretical	1.474	1.553	1.000	0.405
	Simulation	1.385	1.460	0.967	0.372
	Implemented	1.27	1.50	1.00	0.40
Input Power (watts)	Theoretical	1.803	1.712	1.000	0.405
	Simulation	1.744	1.656	0.989	0.378
	Implemented	1.93	1.86	1.11	0.44
X/R	Theoretical	0	0.2933	1.1525	2.0867
	Simulation	0.0000	0.3029	1.1520	2.1710
	Implemented	-	-	-	-
$\psi°$	Theoretical	0	16.3467	49.0524	64.3948
	Simulation	-0.0009	16.8493	49.0402	65.2681
	Implemented	-	-	-	-
$\phi°$	Theoretical	-2.5291	-9.2335	-32.4816	-57.5184
	Simulation	-2.5950	-9.4644	-32.0098	-58.7080
	Implemented	Tuned to -3	-16 +/- 2	-38 +/- 2	Tuned to -59
g	Theoretical	1.2541	1.3550	1.8621	2.9250
	Simulation	1.2569	1.3603	1.8548	3.0147
	Implemented	-	-	-	-
Rdc/R	Theoretical	0.9616	1.0124	1.7337	4.2777
	Simulation	0.9941	1.0476	1.7534	4.5936
	Implemented	0.90	0.93	1.56	3.94

The power dissipated in the switching device can be determined by subtracting (15) from (14). The worst case heat dissipation (point "F") occurs when the output network is tuned to $X/R = -1.7972$ ($\psi = -60.908°$, $\phi = +23.380°$), a net capacitive reactance. The input and output power levels become 1.30 and 0.42 of the original design values, respectively. The efficiency drops to 32%, while the device dissipation becomes 0.88 of the original output power level.

VI. Auxiliary Tuning Modification

Recall that maximum power transfer between source and load requires a complex-conjugate match. At dc, this makes the source resistance equal to the dc load resistance. Using this concept, the dc feed circuit to the class-E stage can be modified as shown in Fig. 8.

This feeds the circuit with double the supply voltage through a resistor $R_{\rm source}$ that is equal to the dc-input resistance (11) as seen by the original dc supply. Therefore, the amplifier is fed with the same voltage as before $(V_{\rm DD})$ at the same current as before $(I_{\rm dc})$. Therefore, the *maximum* possible input power is the design value $(P_{\rm in})$. The solid bold lines in Figs. 2–5 show the resulting change in circuit behavior. The maximum power and efficiency points are coincident at "A." The auxiliary circuit has less sensitivity to component variations, and $Q_{3\,\rm dB}$ is calculated to be 167 using the data of Fig. 3. The optimum value for $R_{\rm source}$ can be calculated using $\phi = \arctan(-2/\pi)$ and $g = \sqrt{1 + \pi^2/4}$ in (11). The result is

$$R_{\rm source} = R_{\rm dc} = \left(\frac{1}{2} + \frac{\pi^2}{8}\right) R \cong 1.7337R. \qquad (17)$$

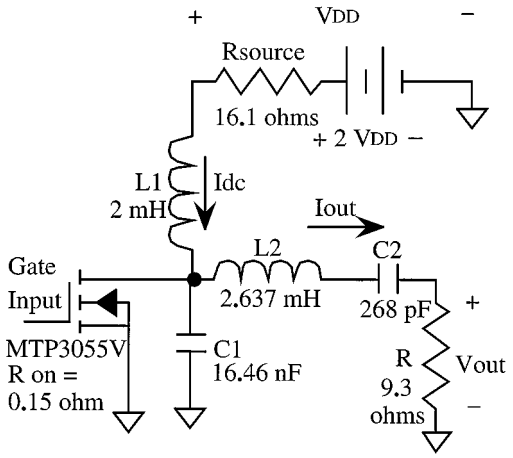

Fig. 8. Class-E topology with auxiliary circuit added.

Clearly, the addition of $R_{\rm source}$ reduces the drain efficiency by a factor of two, but a so-called lossless resistor can be synthesized to maintain high efficiency [8]. A simple passive alternative is to switch-in $R_{\rm source}$ during the tuning process only. The existing supply ($1V_{\rm DD}$) can be used to peak-tune the circuit at one-fourth of normal power. This offers a measure of protection against transistor overdissipation while the circuit is being adjusted.

VII. High-Q Implementation

A 1-W class-E transmitter was built using the topology of Figs. 1 and 8 at a frequency of 189.700 kHz with a loaded Q of 340. High Q is a consequence of using a small capacitance value for $C2$, considering the frequency of operation. Inductor $L2$ must become large per (5a) to compensate. It is interesting to note that the rms voltage across $L2$ (or $C2$) exceeds 1 kV for an output power of 1 W. $L2$ is an 80-turn air-wound coil on a polyethylene basket-weave form 20 cm in diameter using 200/44 litzendraht (200 insulated parallel woven strands of #44 gauge wire). It has a swinging link of a few turns to allow its value to be varied by ± 22 μH. The unloaded Q of $L2$ was measured to be greater than 730. Its RF resistance is 4.2 Ω. (An air core is preferred over a ferrite core to maximize the unloaded Q at rated current.) $C2$ is a 2-kV-rated air-variable capacitor set to 268 pF with an unloaded Q greater than 30 000. Its RF resistance is 0.1 Ω. Silvered mica capacitors are used for $C1$. The switch is a Motorola MTP3055V MOSFET with $C_{\rm DS}$ less than 180 pF and an on-resistance of less than 0.15 Ω. Component values were measured using a HP4194A impedance analyzer. In the implementation, the actual load resistance was 5.0 Ω and the resistances were summed together to obtain the 9.3 Ω used for the simulations. The circuit shown in Fig. 8 was peak-tuned for optimum operation at point "A," and the waveforms shown in Fig. 6 were obtained for this tuning condition. The second, third, and fourth harmonics at the RF load were measured to be -56.5, -70, and -84 dBc, respectively.

VIII. Conclusion

High-Q design equations have been verified by simulation and by implementation at low frequencies. A convenient expression (13) has been derived for ϕ as a function of ψ for the 50% duty-cycle case, with $B = B_{\rm opt}$ for a given R. Output power "peaking" occurs in all class-E amplifiers whenever the output network is tuned in the vicinity of $\phi = -9^\circ$ or the operating frequency is shifted slightly lower. This peaking effect will increase the output power to $\sim$1.5 times the design value and reduce the efficiency to less than 91%. This will occur regardless of the loaded Q of the circuit (assuming a sinusoidal load current). An auxiliary circuit has been discussed that allows the circuit to be peak-tuned to arrive at optimum class-E operation.

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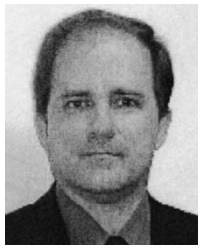

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