Calibratable Adaptive Antenna Combiner at 5.2 GHz with High Yield for Laptop Interface Card

Frank Ellinger, *Student Member, IEEE,* Rolf Vogt, and Werner Bächtold, *Fellow, IEEE*

***Abstract*—This paper presents a calibratable adaptive antenna combiner with three branches for high-performance radio local area network at 5.2 GHz. The system was mounted on a reinforced duroid substrate and enables the integration in a laptop interface card. Each branch consists of a bent stacked slot antenna, a low-noise-amplifier monolithic microwave integrated circuit (MMIC) with antenna/calibration switching and a vector modulator MMIC with an amplitude control range of 15 dB and 360° phase control range. The signals of the three branches are combined by an active adder MMIC. A calibration is proposed to significantly improve the phase and amplitude control resolution and the yield of the designed MMIC circuits, which were fabricated using a commercial GaAs process. Each branch has a maximum power gain of 16 dB, a noise figure of 3.3 dB, and a 1-dB output compression point of −4 dBm. The whole system draws less than 28 mA from a 2.7-V voltage supply. The total required MMIC chip size is 10.8 mm^2.**

***Index Terms*—Amplitude control, GaAs MESFET, HIPERLAN, MMIC, phase control, smart antennas, vector modulator.**

I. Introduction

THE high-performance radio local area network (HIPERLAN) standard at 5.2 GHz plays a growing role in the area of wireless LAN systems. Serious challenges are its high bit rate of 23.5 Mbit/s and its peer-to-peer approach, which allows direct communication between terminals without requiring a central base station. To counteract the time dispersive nature of the indoor radio channel, the use of adaptive antenna combining has been proposed [1]. It has been successfully shown in [2] that even arrays with only three or four active antennas can strongly reduce intersymbol interferences, resulting in a significant improvement of the bit error rate (BER). However, precise amplitude control elements and phase shifters with phase control ranges of 360° are required for this purpose to successfully compete with the performance of approaches using costly baseband equalizer techniques. This paper presents an adaptive antenna combiner with three branches, which has been mounted on a 2 in × 2 in × 0.1 in duroid substrate with reinforced backplane. Its size allows the integration in a laptop interface card, protruding out of a terminal (e.g., a laptop), as illustrated in Fig. 1. The Personal Computer Memory Card International Association (PCMCIA) standard is applied for this interface card. Each branch of the combiner consists of a bent stacked slot antenna (BSSA) [3], an LNA monolithic microwave integrated circuit (MMIC), and a vector-modulator MMIC for amplitude and phase control. The signals of the three branches are combined by an active signal adder MMIC.

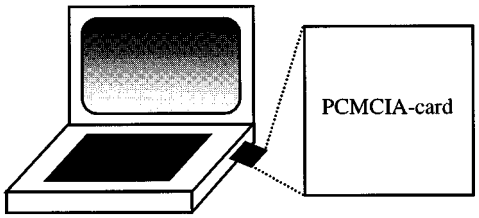

Fig. 1. Example of a PCMCIA card used for laptops.

Passive attenuators [4] and variable gain amplifiers (VGAs) [5] are frequently used to control the amplitude in adaptive antenna receivers. Reflective-type phase shifters [6] and switched high-pass/low-pass phase shifters [7] are among the most important techniques for phase shifting. In comparison to these components, vector modulators [8] are excellent alternatives and have been chosen for this system, because they are able to adjust both amplitude and phase in the same circuit, are well suited for monolithic integration, require only a relatively small chip area, and have the ability to provide gain. Our vector modulator uses VGAs, which provide large amplitude control ranges to enable continuous amplitude and phase control ranges of 15 dB and 360° by weighting and combining three vectors with phase offsets of 120°.

However, process tolerances, ambient temperature variations, and frequency dependences limit the precision of the required vectors, which are calculated in the baseband algorithm [9]. This algorithm uses the measured data of the received signal vectors of each branch and calculates the optimum vector coefficients of the branches for minimum BER of the system. Constant phase and amplitude errors, which are, for example, caused by the antenna, LNA, adder, and their interconnects have already been considered in these calculations and do not effect the BER. Relative errors, which are caused by the amplitude and phase control elements—in our case, the vector modulators, significantly degrade the BER. A calibration is proposed to circumvent these errors by feeding a switchable calibration signal into the LNA, which is located in front of the vector modulator, as illustrated in Fig. 2.

The Triquint TQTRx GaAs process, which provides MESFETs with gate lengths of 0.6 μm and inductors with a quality factor of approximately 20, is used for the monolithic-microwave integrated-circuit (MMIC) designs. Large- and

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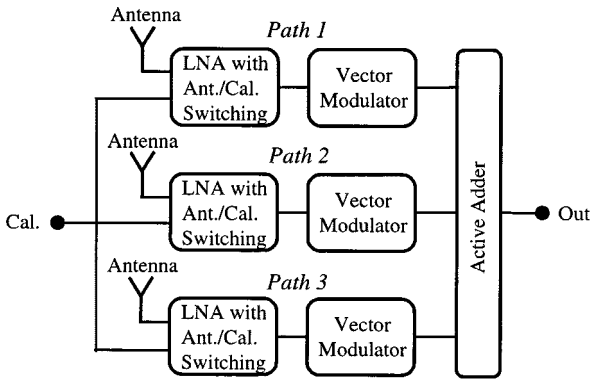

Fig. 2. Architecture of the adaptive antenna combiner with three branches. Cal.: calibration input.

small-signal simulations were performed with HP Libra using a modified TOM II MESFET model [10]. Noise behavior was simulated using measured noise figure data of the FETs.

II. LNA with Antenna/Calibration Switching

Single-pole double-throw (SPDT) switches, which require two control voltages, are frequently used to enable switching between two different signal channels. Two placements for such an SPDT switch are imaginable to enable the fed of a calibration signal for the vector modulator calibration: the SPDT switch could be placed in front of the LNA or between the LNA and the vector modulator. However, the resistive parasitics of the series FETs of an SPDT switch would especially degrade the noise performance of the system when located in front of the LNA, whereas the placement of an SPDT switch between the LNA and vector modulator would degrade the calibration precision. This is caused by the impedance change in front of the vector modulator from the LNA output impedance to the calibration input impedance, which effects the VGA characteristics of the vector modulator.

To circumvent these problems, we propose a cascode LNA with integrated antenna/calibration switching, as shown in Fig. 3. Cold deep-depletion FETs (G-FETs) are used to enable switching between the antenna and calibration signals with only one control voltage (V_{Switch}). A shunt FET with a gatewidth of 300 μm is located at the antenna input of the LNA to enable antenna to calibration isolation, whereas a series FET with a gatewidth of 20 μm enables calibration to antenna isolation. The common source circuit isolates the shunt FET from the calibration input, while the common gate circuit isolates impedance changes of the switching modes to ensure a constant LNA output impedance. The LNA calibration input is matched to 150 Ω to enable 50-Ω match of the overall calibration input of the system, which connects the three LNA calibration inputs together. The antenna input and output are reactively matched to 50 Ω. Enhancement FETs (E-FETs) with gatewidths of 100 μm are used to reach high gain, while consuming minimum dc current. *RC* feedback is applied to the common gate FET to improve RF stability and to make the circuit more broad band. The source of the common source FET is inductively degenerated to improve noise performance,

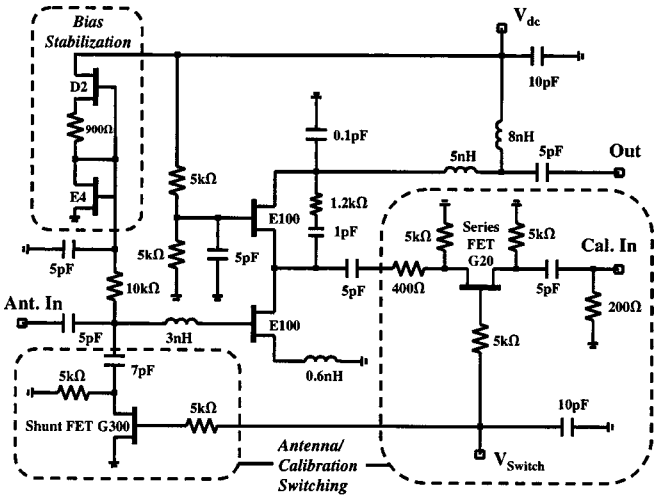

Fig. 3. Circuit schematic of the LNA with calibration/antenna switching, antenna mode ($V_{\mathrm{Switch}} = -3$ V, antenna: on, calibration: off). Calibration mode ($V_{\mathrm{Switch}} = 0$ V, antenna: off, calibration: on).

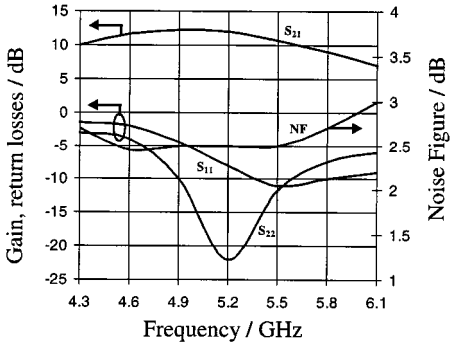

Fig. 4. Measured gain, noise figure, and input and output return loss of the LNA with antenna/calibration switching, switching mode: antenna on, calibration off ($V_{\mathrm{dc}} = 2.7$ V, $I_{\mathrm{dc}} = 2.6$ mA).

input matching, and intermodulation performance. The gates are biased by high-value resistors. The drain of the common gate FET is biased with an inductance and its gate is terminated with a large capacitor. A bias stabilization circuit is applied to the gate of the common source FET to decrease effects of threshold voltage variations and to ensure a nominal dc current of 2.6 mA. The bias stabilization circuit consists of an E-FET and a depletion FET (D-FET) with strong resistive feedback and consumes a dc current of 60 μA.

Fig. 4 shows the measured gain, noise figure, and return losses of the LNA in the antenna mode ($V_{\mathrm{Switch}} = -3$ V, antenna: on, calibration: off). At a supply voltage of 2.7 V, the gain is 12 dB and the noise figure is 2.5 dB. The 1-dB output compression point is -2 dBm and the input and output return losses are 7 dB (noise match) and 22 dB, respectively. The calibration to output isolation is 33 dB. In the calibration mode ($V_{\mathrm{Switch}} = 0$ V, antenna: off, calibration: on) the loss is 12 dB. The requirements for the noise performance in this mode are not demanding because a strong local calibration signal is used, providing a sufficient signal-to-noise ratio. The antenna to output isolation is 20 dB.

Fig. 5 shows a photograph of the bonded MMIC chip with a chip size of 1 mm $\times$ 0.9 mm.

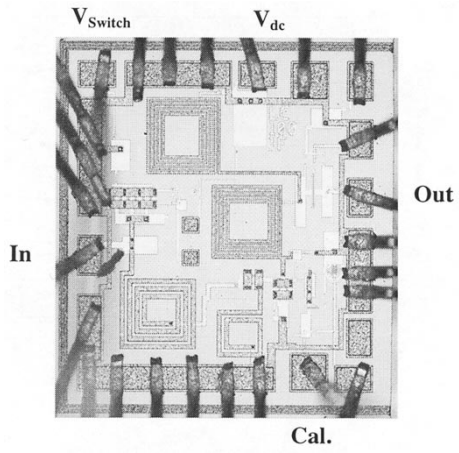

Fig. 5. LNA MMIC with antenna/calibration.

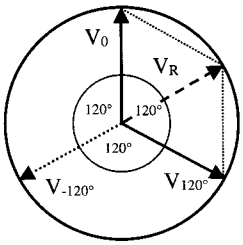

Fig. 6. Vector addition: every phase with amplitude V_R can be obtained by weighting the vectors V_0, V_{120° and V_{-120°.

III. Calibratable Vector Modulator

Usually four signal paths with phase offsets of 90° are used for vector modulators. To minimize chip size and control complexity, we use only three signal paths with phase offsets of 120°. Every phase between 0° and 360° with amplitude V_R can be obtained by weighting the amplitudes of the paths, as illustrated in Fig. 6.

The simplified circuit schematic of the vector modulator is shown in Fig. 7. Input and output are matched to 50 Ω. Low power-consuming E-FETs with gatewidths of 75 μm are used for the VGAs, which divide the input signal. Cascode configurations are applied because their variation of the input and output impedances versus gain is much smaller than in VGAs using single transistors [11], which is important to improve the quasi-ideal power divider/combiner function of the vector modulator over the whole amplitude range. The use of the proposed calibration (see the following section) would otherwise cause impedance variations, which would generate phase and amplitude errors. A further advantage of cascode circuits is that they provide large amplitude control ranges and high gain. The VGAs are reactively matched and the amplitude of the different phase paths can be controlled by varying the gate control voltages (V_{LP}, V_0, V_{HP}) of the common gate FETs. A bias stabilization circuit similar to the one used for the LNA is applied to the gates of the common source FETs to decrease effects of threshold voltage variations and to ensure a nominal dc current of 1.6 mA per path, when the corresponding control voltage is set for maximum gain.

The phase offsets of ±120° are generated by *LC* high- and low-pass structures. Simulations show insertion losses of lower than 2 dB within the frequency range between 4.8–5.8 GHz. The three paths are added by a modified Wilkinson combiner using lumped elements. Simulations show that this combiner has a loss of 6 dB per path and a port-to-port isolation of over 20 dB within the frequency range between 4.8–5.8 GHz.

Fig. 8 shows the measured gain and phase of each of the three paths versus frequency at maximum gain ($\mathrm{control\ voltage} = 1.5$ V), while the other two paths are switched off. Within 4.8 and 5.8 GHz, the losses of the paths are less than 0.7 dB and the phase offsets between the three paths are 120°. Fig. 9 shows the measured gain of each of the three paths versus control voltage at a frequency of 5.2 GHz. The amplitude control range of the VGAs is 33 dB. Due to this large gain control range, phase as well as amplitude can be controlled with this vector modulator. Fig. 10 shows the noise and compression performance of the vector modulator versus gain at 5.2 GHz, when one path is active and two paths are switched off (this is the worst case). The noise figure at maximum gain is 6 dB and is increasing with decreasing gain. Within the whole gain control range, the 1-dB input compression point is higher than −10 dBm. The maximum current consumption per path is 1.6 mA; thus, the maximum current consumption of the vector modulator is 3.2 mA from a supply voltage of 2.7 V.

Fig. 11 shows a photograph of the vector modulator MMIC; the chip size is 1.7 mm × 1.4 mm.

A. Calibration

A calibration signal can be fed as shown in Fig. 2. With the assumption of an ideal divider/combiner, we can assume that the different paths are isolated from each other. Thus, the output vector of the vector modulator can be calculated as a function of the vectors of each single path. We propose the following two-step calibration procedure.

Step 1) Measurement of the gain and phase versus control voltage of each of the three paths, while the other two paths are switched off.

Step 2) Calculation of the corresponding control voltages for a desired phase and amplitude by vector addition, using the data from step 1).

The baseband signal processor can be used for this task. If the transmitting frequency is changed or if the receiver has to adapt to temperature variations, the calibration procedure can be repeated.

To validate the proposed calibration procedure, measurements are compared with ideal calculations given by the calibration procedure. Fig. 12 shows the resulting phase and gain errors, which are, in particular, created by the nonideal divider/combiner function of the circuit. As expected, the errors increase with decreasing gain because the performance of the quasi-ideal divider is degrading. For a gain of 0 dB, the errors are below ±0.5 dB and ±6°, for a gain of −15 dB, the errors are below ±0.8 dB and ±9°. System simulations show that those precisions are well suited for smart antenna receivers [9]. Note that the requirements for the precision and for the

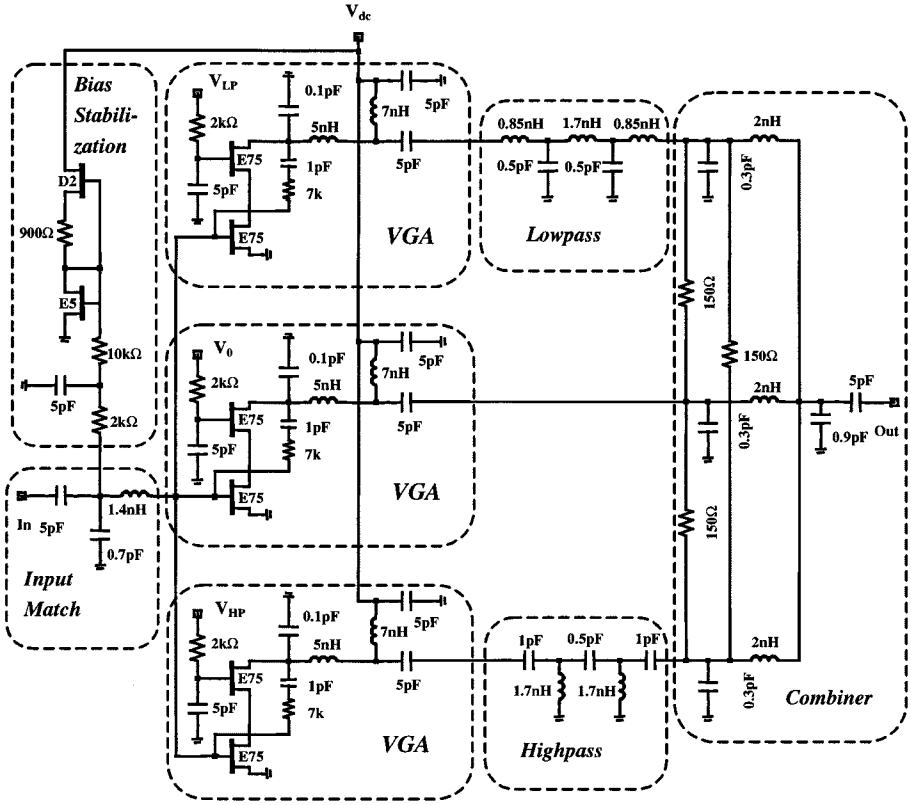

Fig. 7. Circuit schematic of the vector modulator.

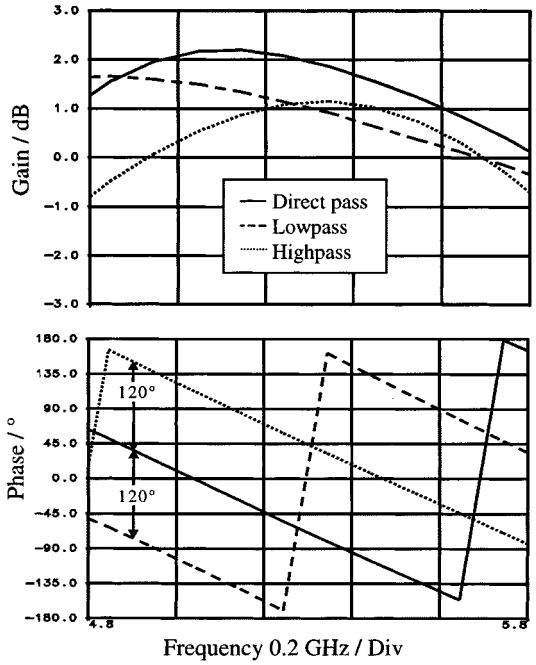

Fig. 8. Measured phase and gain of the individual paths of the vector modulator versus frequency at a control voltage of 1.5 V ($V_{\rm dc} = 2.7$ V, $I_{\rm dc} = 2$ mA).

noise fall with decreasing gain. If all paths are switched off, the attenuation is 33 dB. This mode is used to select the different branches of the system for calibration.

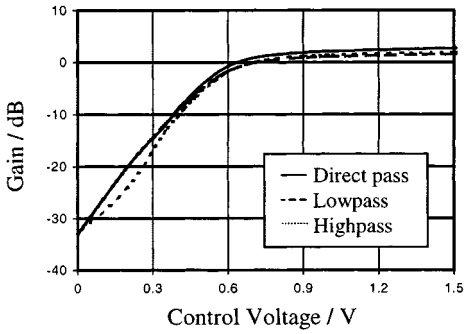

Fig. 9. Measured gain of each of the three paths of the vector modulator versus control voltage, while the other paths are switched off ($V_{\rm dc} = 2.7$ V, $f = 5.2$ GHz).

IV. Active Adder

Fig. 13 shows the simplified circuit schematic of the active adder, which combines the signals of the three branches of the system. The input signals ($I1$, $I2$, $I3$) are fed through the gates of the FETs, the signals are added by connecting the drains together. D-FETs with gatewidths of 100 μm are used, showing excellent large-signal performance, while consuming minimum dc current. The inputs and the output are reactively matched to 50 Ω. The gates are biased by resistors, which improve stability and make the circuit more broad band. The drains are biased by an inductor.

Fig. 14 shows the measured gain and the input and output return loss at a supply voltage of 2.7 V and a total current consumption of 10.8 mA. At 5.2 GHz, the gain is 4 dB, the 1-dB

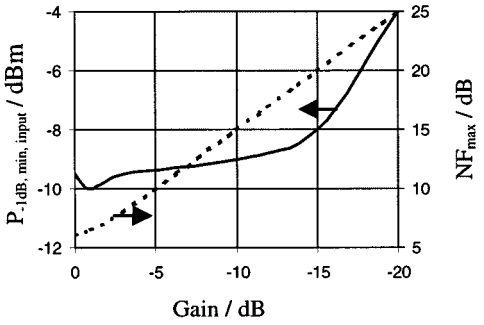

Fig. 10. Measured maximum noise figure ($\mathrm{NF}_{\max}$) and minimum 1-dB compression point at the input ($P_{-1\ \mathrm{dB},\ \min,\ input}$) versus gain of the vector modulator $V_{\mathrm{dc}} = 2.7$ V, $f = 5.2$ GHz.

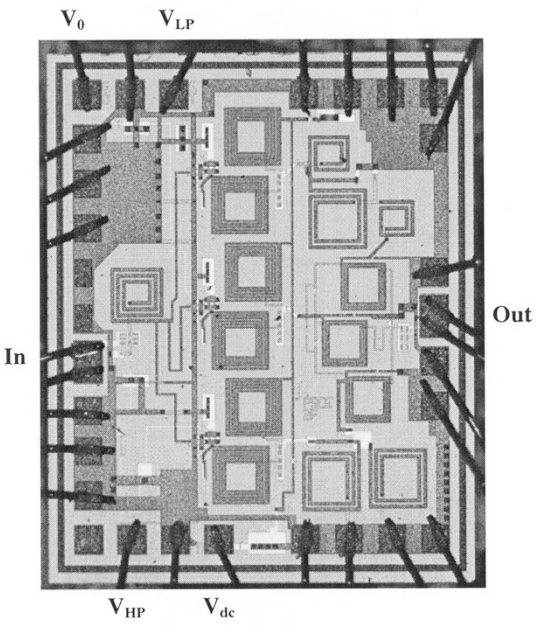

Fig. 11. Vector modulator MMIC (chip size is 1.7 mm × 1.4 mm).

output compression point per branch is 7 dBm and the input and output return losses are 10 and 27 dB, respectively.

Fig. 15 shows a photograph of the bonded adder MMIC chip, which has a size of 1 mm × 1 mm.

V. Adaptive Combiner

The MMIC chips were mounted on a duroid substrate with a dielectric constant of $\varepsilon_r = 10.2$ and a size of 2 in × 2 in × 0.1 in, as shown in Fig. 16. SMA connectors are mounted to enable RF measurements. A plug with several pins is mounted to feed the circuits with the ten required dc control voltages (nine for the vector modulators and one for antenna/calibration switching) and the supply voltage. The BSSAs [3] are mounted on the reinforced back metal of the substrate. The back metal is used as the common ground plane of the antennas, as shown in Fig. 17. Due to their compact size ($16 \times 8 \times 5.2$ mm^3), low costs (easily manufactured from one thin sheet of metal and tolerant to manufacturing inaccuracies), large bandwidth of 30%, high efficiency

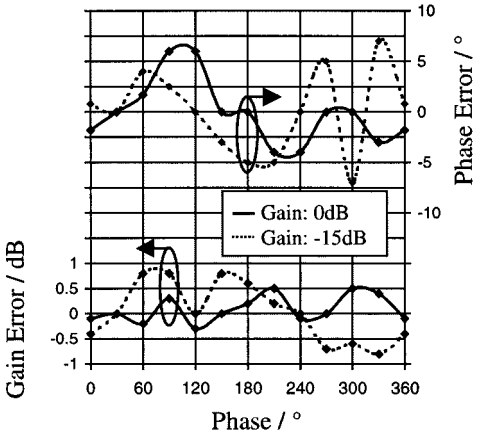

Fig. 12. Measured phase and gain error of the vector modulator at a gain of 0 dB (maximum gain) and −15 dB, respectively, versus expected phase, obtained using the calibration ($V_{\mathrm{dc}} = 2.7$ V, $f = 5.2$ GHz).

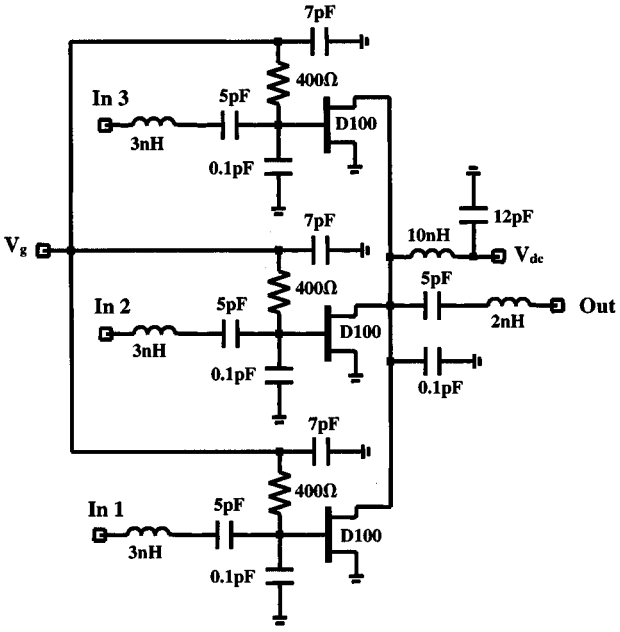

Fig. 13. Circuit schematic of the active adder, which combines the signals of the three branches.

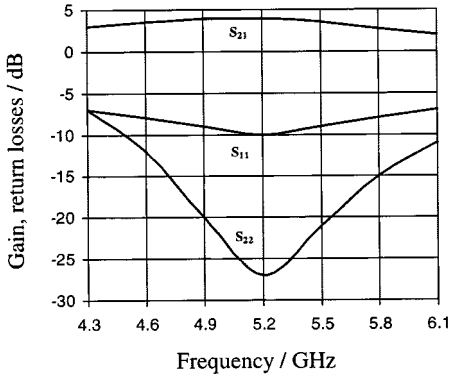

Fig. 14. Measured gain and input and output return loss of the active adder ($V_{\mathrm{dc}} = 2.7$ V, $V_G = -0.3$ V $I_{\mathrm{dc}} = 10.8$ mA).

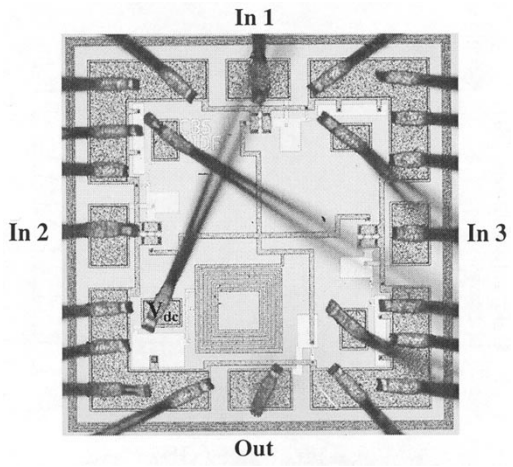

Fig. 15. Active adder MMIC (chip size is 1 mm × 1 mm).

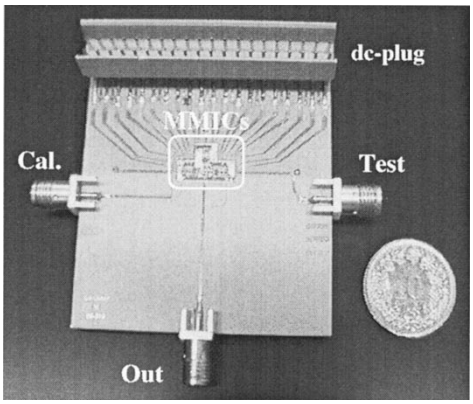

Fig. 16. Front of the adaptive combiner with three branches (size of the duroid substrate: 2 × 2 in.

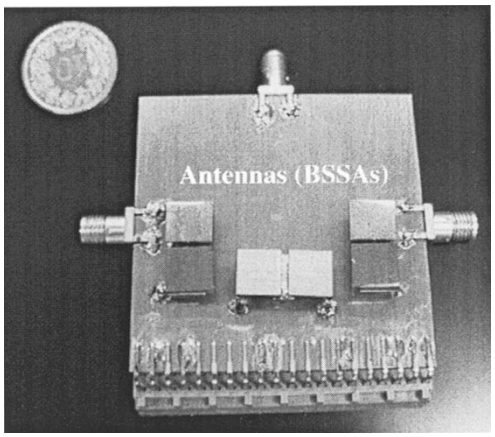

Fig. 17. Backside of the adaptive combiner with three branches.

of 90%, and an antenna gain of 4 dBi, these antennas excellently fulfill the requirements for wireless LAN applications.

Table I summarizes the performances of the system. Each branch has a maximum power gain of 16 dB, a noise figure of 3.3 dB, and an 1-dB output compression point of −5 dBm. Depending on the number of activated paths in the vector modulators, the minimum and maximum current consumption of the whole system using a 2.7-V supply is only 20.2 and 28.2 mA, respectively. Phase and gain control performances are reached, as described in Section III. The required GaAs chip size for the whole system is 11 mm^2.

TABLE I
SUMMARIZED PERFORMANCES OF THE ADAPTIVE COMBINER AT 5.2 GHz

Maximum power gain per branch	16dB
Antenna gain per branch	4dBi
Noise figure per branch	3.3dB
1dB output compression point per branch	-5dBm
Amplitude control range / max. attenuation per branch	15dB / 33dB
Phase control range per branch	360°
Max. amplitude errors per branch	±0.8dB
Max. phase errors per branch	±9°
Output return loss	25dB
Loss of the calibration signal	12dB
1dB calibration input compression point per branch	-5dBm
Supply voltage	2.7V
Min. / max. current consumption	20.2mA / 28.2mA
Size of the substrate	2in x 2in x 0.1in
Required GaAs MMIC chip size	~11mm^2
Total number of control voltages	10

VI. CONCLUSION

A calibratable adaptive antenna combiner with three branches for HIPERLAN at 5.2 GHz has been presented in this paper. The system was mounted on a reinforced duroid substrate and is well suited for PCMCIA card integration. It consists of three BSSAs and highly integrated MMIC circuits (three LNAs with calibration switching, three vector modulators for amplitude and phase control, and an active signal adder). A calibration is proposed to significantly improve the production yield, the operation bandwidth, and to compensate the effects of temperature variations. Due to its low power consumption and its low-cost design, the system is a potential alternative to approaches using costly baseband equalizer techniques.

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