# Rigorous Modeling of Packaged Schottky Diodes by the Nonlinear Lumped Network ($NL^2N$)–FDTD Approach

Gianluca Emili, Federico Alimenti, *Member, IEEE*, Paolo Mezzanotte, Luca Roselli, *Member, IEEE*, and Roberto Sorrentino, *Fellow, IEEE*

***Abstract*—Recently, a novel method has been proposed that allows general linear lumped networks to be incorporated within finite-difference time-domain (FDTD) simulators. In this paper, this method is extended in such a way as to represent two-terminal nonlinear lumped networks in a single FDTD grid cell. In particular, the extended method is applied to the rigorous modeling of packaged Schottky diodes. The implementation is first validated in the case of a diode connected to a voltage source. The SPICE simulator has been used to provide reference results. The same structure has also been used to establish the accuracy of the method. It has been demonstrated that such accuracy is significantly increased with respect to that of the conventional lumped-element–FDTD approach. Finally, the technique has been validated against measured results, showing a good agreement.**

***Index Terms*—FDTD method, packaging, Schottky diodes.**

## I. Introduction

The accurate design of millimeter-wave circuits and quasi-optical structures requires the use of simulators able to combine full-wave numerical methods with models of electronic devices. The first ones allow the description of the distributed (passive) part of the circuit, while the second ones are suitable for the representation of active nonlinear elements (diodes, transistors, etc.).

One of the most promising techniques developed to this purpose is the lumped-element–finite-difference time-domain (LE–FDTD) method [1], [2]. It is based on the assumption that the device dimensions are much smaller than the wavelength. From the geometrical point-of-view, the simulated structure is represented on a three-dimensional grid (spatial discretization), while lumped elements can be included between adjacent grid nodes. Thanks to many authors, LE–FDTD compatible models of the basic two-terminal devices (resistors, capacitors, inductors, diodes, etc.) and three-terminal devices (transistors, etc.) have been developed in the last years [3]. These circuit elements can be used as building blocks to form lumped networks or sub-circuits useful, for example, to describe the device-package interaction up to millimeter-wave frequencies.

The above approach has, however, the following drawback: each two-terminal element must be placed across a different cell edge. This means that the representation of any network is necessarily distributed over several grid cells, thus weakening the lumped-element assumption on which the method is based. As an example, let us consider a resistor of value $R$ represented either in a single cell or along $N$ cell edges connected in series, each loaded with a resistor of value $R/N$. Although these two networks are equivalent from the circuit point-of-view, they behave differently when inserted in the finite-difference time-domain (FDTD) simulator.

Another problem is that a unique topology does not exist for the distributed network. In the above example, different topologies can be obtained playing with the edge orientations within the three-dimensional FDTD grid. Furthermore, the $N$ resistors could be chosen of different values $R_i$, with $i = 1, \ldots, N$, the only requirement being $\sum_i^N R_i = R$.

The inaccuracy associated with the distribution of the lumped network over the FDTD grid increases with the number of circuit elements constituting the network (number of cells over which the network is distributed). This effect cannot easily be predicted because of the nonunique topology.

To solve the above problems, several strategies have been proposed. In [4], the device–wave interaction is modeled through equivalent current sources and state equations. Alternatively, it is possible to incorporate a general linear two-terminal network in a single FDTD cell. This can be done by the so called lumped-network (LN)–FDTD method that has recently been developed [5].

In this work, the LN–FDTD approach is extended in such a way as to represent a two-terminal network, composed by linear and nonlinear elements, in a single FDTD cell. The new method, referred to as the nonlinear lumped network ($NL^2N$)–FDTD method, has been developed and applied to the rigorous modeling of packaged Schottky diodes.

Using a simple structure composed by a voltage source connected to the packaged diode, it has been demonstrated that the proposed method significantly increases the accuracy with respect to the conventional LE–FDTD technique.

## II. Method

The $NL^2N$–FDTD method will be described in the case of the Schottky diode illustrated in Fig. 1(a). In this figure, the intrinsic Schottky junction $D$ is connected to other circuit elements, modeling the package parasitics. In particular, $R$ is the

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The authors are with the Dipartimento di Ingegneria Elettronica e dell'Informazione, Università di Perugia, I-06125 Perugia, Italy (e-mail: alimenti@diei.unipg.it).

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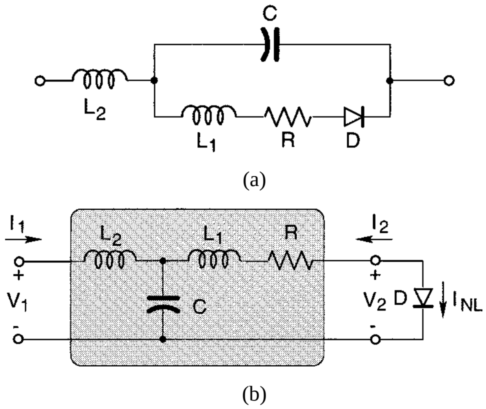



Fig. 1. Schottky diode models. Parasitics: $R = 6\ \Omega$, $C = 0.08$ pF, $L_1 = 1.3$ nH, $L_2 = 1.0$ nH. SPICE parameters: $I_0 = 46$ nA, $\tau_d = 0$ s, $C_{J0} = 0.18$ pF, $\phi_0 = 0.5$ V, $m = 0.5$, $F_c = 0.5$.

chip resistance, $L_1$ is the bonding wire inductance, $L_2$ is the lead inductance, and $C$ is the package capacitance. The typical values of these parameters are quoted in the caption of Fig. 1.

To incorporate the packaged Schottky diode in a single FDTD cell, the model of Fig. 1(a) is segmented in a linear two-port network terminated with the intrinsic diode $D$, as shown in Fig. 1(b). Following [5], the admittance matrix of the linear network in the Laplace domain

$$[Y] = \frac{1}{D(s)} \begin{bmatrix} L_2Cs^2 + RCs + 1 & -1 \\ -1 & L_1Cs^2 + 1 \end{bmatrix}$$
$$D(s) = L_1L_2Cs^3 + RL_1Cs^2 + (L_1 + L_2)s + R \tag{1}$$

is converted into the $Z$-domain using the bilinear transformation [6, p. 415]. The resulting admittance matrix representation in the $Z$-domain is given by

$$\hat{I}_p(z) = \sum_{q=1}^{2} \hat{Y}_{pq}(z)\hat{V}_q(z) \tag{2}$$

where

$$\hat{Y}_{pq}(z) = \frac{\sum_{r=0}^{M} c_r^{pq} z^{-r}}{1 + \sum_{r=0}^{M} d_r z^{-r}} \tag{3}$$

where $p, q = 1, 2$ are the port indexes. The coefficients $c_r^{pq}$ and $d_r$ are quoted in Tables I and II, respectively. Exploiting the property $z^{-r}\hat{F}(z) \leftrightarrow F^{n-r}$, the finite difference form of (2) is easily obtained as follows:

$$I_1^{n+1} = \sum_{r=0}^{3} c_r^{11} V_1^{n-r+1} + \sum_{r=0}^{3} c_r^{12} V_2^{n-r+1} - \sum_{r=1}^{3} d_r I_1^{n-r+1}$$
$$I_2^{n+1} = \sum_{r=0}^{3} c_r^{21} V_1^{n-r+1} + \sum_{r=0}^{3} c_r^{22} V_2^{n-r+1} - \sum_{r=1}^{3} d_r I_2^{n-r+1}. \tag{4}$$

TABLE I
$c_r^{pq}$ COEFFICIENTS

| $r$ | $c_r^{11}$ | $c_r^{12} = c_r^{21}$ | $c_r^{12}$ |
|---|---|---|---|
| 0 | $-\Delta t^3 - 2\,RC\,\Delta t^2 - 4\,L_2\,C\,\Delta t$ | $\Delta t^3$ | $-\Delta t^3 - 4\,L_1\,C\,\Delta t$ |
| 1 | $-3\,\Delta t^3 - 2\,RC\,\Delta t^2 + 4\,L_2\,C\,\Delta t$ | $3\,\Delta t^3$ | $-3\,\Delta t^3 + 4\,L_1\,C\,\Delta t$ |
| 2 | $-3\,\Delta t^3 + 2\,RC\,\Delta t^2 + 4\,L_2\,C\,\Delta t$ | $3\,\Delta t^3$ | $-3\,\Delta t^3 + 4\,L_1\,C\,\Delta t$ |
| 3 | $-\Delta t^3 + 2\,RC\,\Delta t^2 - 4\,L_2\,C\,\Delta t$ | $\Delta t^3$ | $-\Delta t^3 - 4\,L_1\,C\,\Delta t$ |

TABLE II
$d_r$ COEFFICIENTS

| $r$ | $d_r$ |
|---|---|
| 0 | $-R\,\Delta t^3 - 2\,(L_1 + L_2)\,\Delta t^2 - 4\,R\,L_1\,C\,\Delta t - 8\,L_1\,L_2\,C$ |
| 1 | $-3\,R\,\Delta t^3 - 2\,(L_1 + L_2)\,\Delta t^2 + 4\,R\,L_1\,C\,\Delta t + 24\,L_1\,L_2\,C$ |
| 2 | $-3\,R\,\Delta t^3 + 2\,(L_1 + L_2)\,\Delta t^2 + 4\,R\,L_1\,C\,\Delta t - 24\,L_1\,L_2\,C$ |
| 3 | $-R\,\Delta t^3 + 2\,(L_1 + L_2)\,\Delta t^2 - 4\,R\,L_1\,C\,\Delta t + 8\,L_1\,L_2\,C$ |

To connect the circuit of Fig. 1(b) to the FDTD grid nodes, the following relationships are considered:

$$V_1^n = E_x^n(\mathbf{r}_{E_x})\Delta x$$
$$I_1^n = J_{\ell x}^n(\mathbf{r}_{E_x})\Delta y \Delta z \tag{5}$$

where $\mathbf{r}_{E_x}$ denotes the spatial position at the Yee's cell of $E_x$ and the diode is assumed to be oriented along the $x$-axis.[1] Using (5) in (4), one obtains

$$J_{\ell x}^{n+1}(\mathbf{r}_{E_x})\Delta y \Delta z = c_0^{11} E_x^{n+1}(\mathbf{r}_{E_x})\Delta x + c_0^{12} V_2^{n+1} + \alpha_x^n(\mathbf{r}_{E_x})$$
$$I_2^{n+1} = c_0^{21} E_x^{n+1}(\mathbf{r}_{E_x})\Delta x + c_0^{22} V_2^{n+1} + \beta_x^n(\mathbf{r}_{E_x}) \tag{6}$$

where $\alpha_x^n(\mathbf{r}_{E_x})$ and $\beta_x^n(\mathbf{r}_{E_x})$ represent the memory of the circuit

$$\alpha_x^n(\mathbf{r}_{E_x}) = \sum_{r=1}^{3} \left[ c_r^{11} E_x^{n-r+1}(\mathbf{r}_{E_x})\Delta x + c_r^{12} V_2^{n-r+1} - d_r J_{\ell x}^{n-r+1}(\mathbf{r}_{E_x})\Delta y \Delta z \right]$$
$$\beta_x^n(\mathbf{r}_{E_x}) = \sum_{r=1}^{3} \left[ c_r^{21} E_x^{n-r+1}(\mathbf{r}_{E_x})\Delta x + c_r^{22} V_2^{n-r+1} - d_r I_2^{n-r+1} \right]. \tag{7}$$

Inserting the first of (6) into the discretized Ampère–Maxwell equation

$$E_x^{n+1}(\mathbf{r}_{E_x}) = E_x^n(\mathbf{r}_{E_x}) + \frac{\Delta t}{\epsilon} \left[\nabla \times \mathbf{H}\right]_x^{n+(1/2)} (\mathbf{r}_{E_x}) - \frac{\Delta t}{2\epsilon} \left[ J_{\ell x}^{n+1}(\mathbf{r}_{E_x}) + J_{\ell x}^n(\mathbf{r}_{E_x}) \right] \tag{8}$$

and using the following definitions:

$$q_x = 1 + \frac{\Delta x \Delta t c_0^{11}}{2\epsilon \Delta y \Delta z}$$
$$\gamma_x = -\frac{1}{q_x} \frac{\Delta t c_0^{12}}{2\epsilon \Delta y \Delta z}$$
$$\delta_x^n(\mathbf{r}_{E_x}) = -\frac{1}{q_x} \left[ \frac{\Delta t}{2\epsilon \Delta y \Delta z} \alpha_x^n(\mathbf{r}_{E_x}) - E_x^n(\mathbf{r}_{E_x}) - \frac{\Delta t}{\epsilon} \cdot \left[\nabla \times \mathbf{H}\right]_x^{n+(1/2)} (\mathbf{r}_{E_x}) + \frac{\Delta t}{2\epsilon} J_{\ell x}^n(\mathbf{r}_{E_x}) \right] \tag{9}$$

[1] $\mathbf{r}_{E_x} = (i_\ell + (1/2), j_\ell, k_\ell)$ means that the diode is located between the nodes: $P \equiv (i_\ell, j_\ell, k_\ell)$ and $Q \equiv (i_\ell + 1, j_\ell, k_\ell)$.

a relationship between the electric field at the Yee's cell and the voltage across the Schottky junction is obtained as follows:

$$E_x^{n+1}(\mathbf{r}_{E_x}) = \gamma_x V_2^{n+1} + \delta_x^n(\mathbf{r}_{E_x}). \tag{10}$$

The latter quantity can be obtained from the termination condition of port 2 on the nonlinear element

$$I_2^{n+(1/2)} = \frac{I_2^{n+1} + I_2^n}{2} = -I_{NL}^{n+(1/2)}. \tag{11}$$

where $I_{NL}$ is the current flowing through the diode. Such a current can be computed in terms of the diode voltage $V_2$ and of its time derivative. After the temporal discretization, the diode current can be written as

$$I_{NL}^{n+(1/2)} = f\left(V_2^{n+1}, V_2^n\right) \tag{12}$$

where $f$ is a nonlinear function (see the Appendix). This function allows the termination condition (11) to be expressed by

$$I_2^{n+1} = -2f\left(V_2^{n+1}, V_2^n\right) - I_2^n. \tag{13}$$

Inserting (13) and (10) in the second equation of (6), a nonlinear equation in the unknown $V_2^{n+1}$ is obtained as follows:

$$2f\left(V_2^{n+1}, V_2^n\right) + \left[c_0^{21}\Delta x\gamma_x + c_0^{22}\right]V_2^{n+1} + \left[c_0^{21}\Delta x\delta_x^n(\mathbf{r}_{E_x}) + \beta_x^n(\mathbf{r}_{E_x}) + I_2^n\right] = 0. \tag{14}$$

Such an equation is solved numerically, at each time step, with the Newton–Raphson algorithm [7, pp. 355–360]; the diode voltage $V_2^{n+1}$ is then used in (10) to evaluate the electric field $E_x^{n+1}(\mathbf{r}_{E_x})$ at the lumped-element cell.

## III. Results

The NL$^2$N–FDTD approach has been validated against SPICE simulations and experiments. In all the reported examples, the same Schottky diode has been considered. In particular, the HSMS8202 diode pair has been used. Such diodes are mounted in a series configuration and are encapsulated in an SOT23 package with three leads. The large-signal and package parameters are quoted in the caption of Fig. 1.

### *A. SPICE Validation*

In order to provide a validation of the proposed approach and to establish its level of accuracy, a very simple structure has been considered and simulated. This structure is reported in Fig. 2 and consists of a sinusoidal generator (internal resistance $R_s$) connected to the packaged Schottky diode ($P$ in the figure). The voltage across the diode ($V_1$ in the figure) has been evaluated with three different approaches.

First, the SPICE simulator has been applied to the problem for the computation of $V_1$. This result has been assumed as a reference since the circuit is treated as a purely lumped one by the simulator.

The second approach is based on the LE–FDTD method [3] and requires a discretization of the circuit in Fig. 2. In this case,

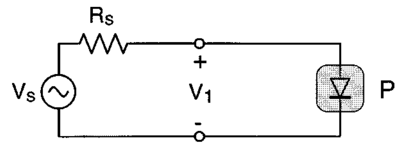



Fig. 2. Structure used for the accuracy test of the proposed models. In the figure, $P$ is the packaged Schottky diode, $V_s = 5$ V, $R_s = 50\ \Omega$, and $f = 1.0$ GHz.

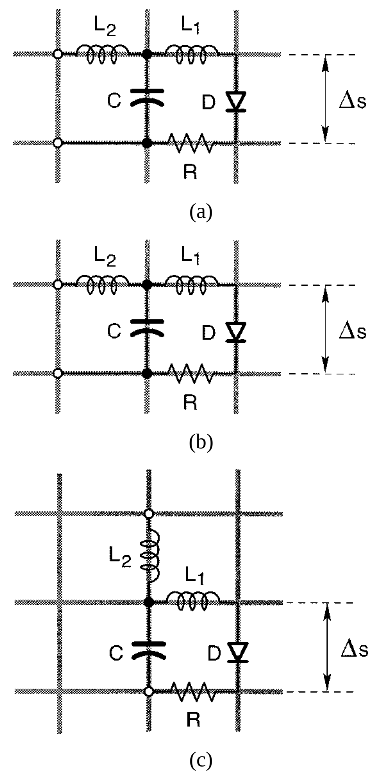
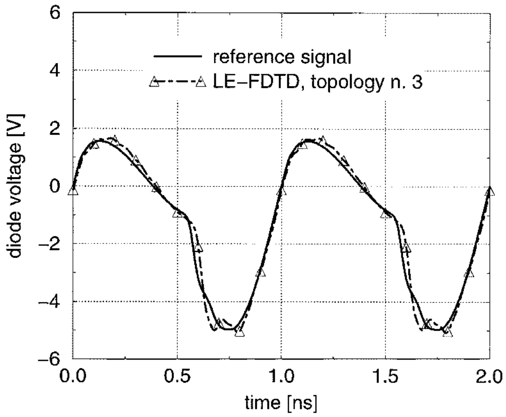



Fig. 3. LE–FDTD models of the packaged Schottky diode.

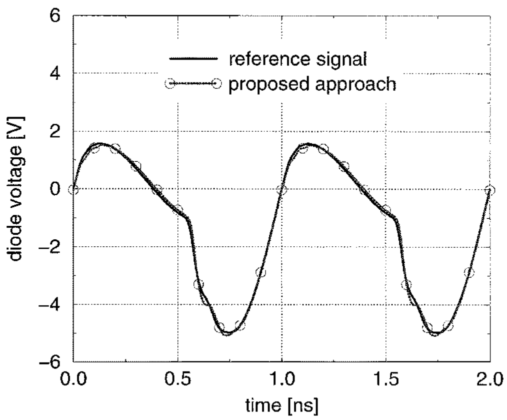
the various elements of the diode package must be placed at different nodes of the FDTD mesh, as shown in Fig. 3, for three particular cases. Such a technique, besides not leading to a unique topology, destroys the lumped nature of the diode equivalent circuit; thus leading to significant inaccuracies, as will be discussed later.

The NL$^2$N–FDTD method developed in Section II is finally adopted to study the problem. It is important to underline that, with this approach, the packaged diode is incorporated into a single FDTD cell.

The results of these simulations are illustrated in Fig. 4 where the rectified voltage $V_1$ is represented versus the time. In particular, Fig. 4(a) shows the signal computed with the LE–FDTD (topology 3 in Fig. 3) approach, while in Fig. 4(b), the NL$^2$N–FDTD data are reported. From the observation of this figure, it is apparent that the NL$^2$N–FDTD method is more accurate than the LE–FDTD one. Both LE–FDTD and NL$^2$N–FDTD analyses have been carried out using the same discretization grid and time step. The former is composed by cubic cells of side $\Delta s$ while, for the latter, the stability limit value is used; these parameters are quoted in the caption of Fig. 4. The simulated circuit is at the center of a $N_x \times N_y \times N_z = 30 \times 30 \times 30$ cells computational domain.




(a)




(b)

Fig. 4. Stationary voltage across the diode. Simulation parameters: $f = 1.0$ GHz, $\Delta s = 1.0$ mm, $\lambda/\Delta s = 300$, $\Delta t = 1.9$ ps. The reference signal has been been obtained with SPICE.

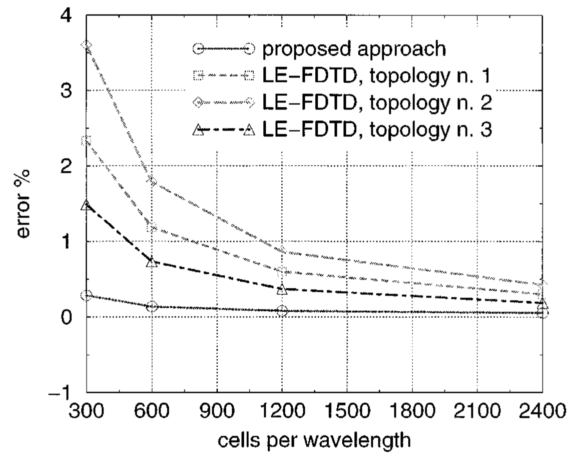


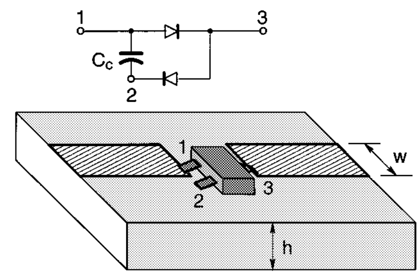

Fig. 5. Percentage error versus the number of cells per wavelength: comparison between LE–FDTD and proposed ($NL^2N$–FDTD) approaches. The error is computed in terms of the rms diode voltage; the reference rms value is obtained with SPICE.

Such a domain is terminated with perfectly matched layer (PML) absorbing boundary conditions.

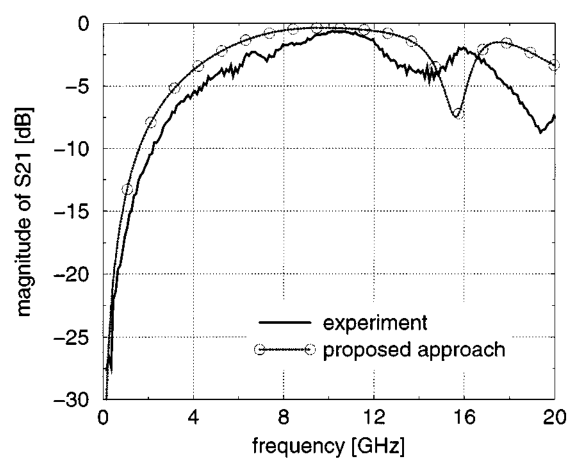
The accuracy of $NL^2N$–FDTD and LE–FDTD diode models has been determined in terms of the rectified voltage rms value, assuming that obtained with SPICE as a reference (equal to 2.598 V). The percentage error with respect to such a parameter is reported in Fig. 5 versus the number of cells per wavelength (parameter $\lambda/\Delta s$). This error has been computed for both the proposed approach ($NL^2N$–FDTD approach) and the LE–FDTD technique; the latter is applied using all the topologies of Fig. 3. From the analysis of Fig. 5 emerges that the convergence rate of the $NL^2N$–FDTD method is greater than that of the LE–FDTD method. Moreover, the error associated with the conventional LE–FDTD models is strongly dependent on the particular topology; the maximum error is associated with topology 2, which is distributed over nine cell edges.

### B. Experimental Validation

The second structure considered consist of a Schottky diode mounted across a microstrip gap. The three-dimensional FDTD method has been adopted for the analysis of this structure; geometrical and discretization parameters are reported in the caption of Fig. 6.




(a)




(b)

Fig. 6. Series-mounted Schottky diode. FDTD parameters: $\Delta x = 0.2$ mm, $\Delta y_{\min} = 0.1$ mm, $\Delta z = 0.3$ mm, $\Delta t = 0.28$ ps. Microstrip dimensions: $h = 0.8$ mm, $w = 1.8$ mm, $\epsilon_r = 3.38$.

The experimental results have been carried out connecting only one of the two diodes available in the package. The coupling between this diode and the remaining one has been modeled by an additional lumped capacitor incorporated in the FDTD mesh. The location of this capacitor is shown in Fig. 6(a) and its value is $C_c = 0.06$ pF. The results are shown in Fig. 6(b); both calculations and measurements are obtained in the small signal (zero biasing) condition. The agreement between simulation and experiment is good.

## IV. Conclusions

In this paper, a new method has been proposed that allows the incorporation of general lumped networks, composed by linear and nonlinear elements, in a single FDTD grid cell. The method, referred to as the NL$^2$N–FDTD method, has been applied to the particular case of the large-signal model of a packaged Schottky diode. For the validation of the NL$^2$N–FDTD method, a simple structure composed by a voltage source connected to the packaged diode has been considered and simulated. The reference time-domain results have been obtained using the SPICE commercial simulator. It has been demonstrated that not only the proposed method leads to a significant accuracy increasing with respect to the conventional LE–FDTD technique, but also that the accuracy of the latter is strongly dependent by the particular topology used to represent the package equivalent circuit. Finally, the proposed method has been applied to the computation of the scattering parameters of a Schottky diode in series to a microstrip line. It is shown that the results provided by the NL$^2$N–FDTD method are in good agreement with the measurements.

## Appendix

The $I$–$V$ characteristic of the Schottky diode has been assumed equal to that of the p-n diode. The diode has been modeled as in [3] with the transition time $\tau = 0$. The diode current is given by

$$I_{NL} = I_0 \left[e^{(V_2/\eta V_T)} - 1\right] + C_J(V_2)\frac{dV_2}{dt} \tag{15}$$

where $V_2$ is the diode applied voltage, $I_0$ is the inverse saturation current, $\eta$ is the junction emission coefficient, $V_T \approx 25$ mV is the thermal voltage at $T = 293$K, and $C_J$ represents the capacitance associated with the junction. The latter is due only to the width modulation of the junction space–charge region ($\tau = 0$) and is expressed by

$$C_J(V_2) = \begin{cases} C_{J0}\left[1 - \dfrac{V_2}{\Phi_0}\right]^{-m}, & V_2 < F_c\Phi_0 \\ \dfrac{C_{J0}}{F_2}\left[F_3 + \dfrac{mV_2}{\Phi_0}\right], & V_2 \geq F_c\Phi_0. \end{cases} \tag{16}$$

In (16), $m$ is a coefficient related to the doping profile ($m = 0.5$ for abrupt junctions), $\Phi_0$ is the junction built-in voltage, $C_{J0}$ is the zero-bias junction capacitance, and $F_c$ is a suitable constant. $F_2$ and $F_3$ can be detrmined as follows:

$$\begin{aligned} F_2 &= [1 - F_c]^{1+m} \\ F_3 &= 1 - [1 + m]F_c. \end{aligned} \tag{17}$$

The temporal discretization of the diode current equation (15) gives

$$I_{NL}^{n+\frac{1}{2}} = I_0\left[e^{(V_2^{n+1}+V_2^n/2\eta V_T)} - 1\right] + C_J\left(\frac{V_2^{n+1}+V_2^n}{2}\right) \cdot \frac{V_2^{n+1} - V_2^n}{\Delta t} \tag{18}$$

and, thus, can be expressed as shown in Section II.

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**Gianluca Emili** was born in Foligno, Italy, in 1974. He received the Laurea degree (*cum laude*) in electronic engineering from the University of Perugia, Perugia, Italy, in 1999, and is currently working toward the Ph.D. degree at the University of Perugia, Perugia, Italy.

His research interests concern the inclusion of the NL$^2$N into the FDTD method.

Mr. Emili is a member of the Associazione Dottori de Ricerca Italiani (ADI), the Italian Ph.D. students Association.

**Federico Alimenti** (S'91–A'97–M'93) was born in Foligno, Italy, in 1968. He received the Laurea degree (*cum laude*) and the Ph.D. degree from the University of Perugia, Perugia, Italy, in 1993 and 1997 respectively, both in electronic engineering.

In 1993, under a scholarship from Daimler-Benz Aerospace, Ulm, Germany, he was with the Microwave and Millimeter-Wave Department. In 1996 he a Guest Scientist at the Lehrstuhl für Hochfrequenztechnik, Technical University of München, Munich, Germany. In 1997, he visited the Technical University of München, under the Vigoni Programme. Since 1993, he has been with the Department of Electronic and Information Engineering, University of Perugia. His research interests concern the FDTD simulation of microwave and millimeter-wave devices, the study of monolithic-microwave integrated-circuit (MMIC) interconnection and packaging technologies and the design, realization, and measurement of high-frequency circuits.

Dr. Alimenti has been a reviewer for the IEEE Microwave and Guided Wave Letters since 1997. He was the recipient of the 1996 Young Scientist Award presented by the URSI

**Paolo Mezzanotte** was born in Perugia, Italy, in 1965. He received the Laurea degree in electronic engineering from the University of Ancona, Ancona, Italy, in 1991 for his thesis on FDTD analysis of the gigahertz transverse electromagnetic (GTEM) cell and the Ph.D. degree from the University of Perugia, in 1997.

Since 1992, he has been involved with FDTD analysis of microwave structures in cooperation with the Department of Electronic and Information Engineering, University of Perugia. In November 1999, he became a Research Assistant in the same department. His main field of interest is the application of numerical methods to the study of components and structures for microwave and millimeter-wave circuits.

Dr. Mezzanotte is a reviewer for the IEEE Microwave and Guided Wave Letters and the IEEE Transactions on Microwave Theory and Techniques.

**Luca Roselli** (M'93) was born in Florence, Italy, in 1962. He received the Laurea degree in electronic engineering from the University of Florence, Florence, Italy, in 1988.

From 1988 to 1991, he was with the University of Florence, where he was involved with surface acoustic wave (SAW) devices. In November 1991, he joined the Department of Electronic and Information Engineering, University of Perugia, Perugia, Italy, as a Research Assistant, where, since 1994, he has taught the "Electronic Devices" course. His research interests include the design and development of microwave and millimeter-wave active and passive circuits by numerical techniques.

Dr. Roselli has been a reviewer for the IEEE MICROWAVE AND GUIDED WAVE LETTERS (since 1996) and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (since 1998). In 1998, he became a Technical Committee member of the Electrosoft Conference, European Microwave Conference, and the IEEE Microwave Theory and Techniques Symposium.

**Roberto Sorrentino** (M'77–SM'84–F'90) received the Doctor degree in electronic engineering from the University of Rome "La Sapienza," Rome, Italy, in 1971.

In 1971, he joined the Department of Electronics, University of Rome "La Sapienza," where he became an Assistant Professor in 1974. He was also "Professore Incaricato" at the University of Catania (1975–1976), the University of Ancona (1976–1977), and the University of Rome "La Sapienza" (1977–1982), where he then was an Associate Professor (1982–1986). In 1983 and 1986, he was a Research Fellow at The University of Texas at Austin. From 1986 to 1990, he was a Professor at the Second University of Rome "Tor Vergata." Since November 1990, he has been a Professor at the University of Perugia, Perugia, Italy, where he was the Chairman of the Electronic Institute, Director of the Computing Center, and is currently the Dean of the Faculty of Engineering. His research activities have been concerned with electromagnetic-wave propagation in anisotropic media, interaction with biological tissues, and mainly with the analysis and design of microwave and millimeter-wave passive circuits. He has contributed to the planar-circuit approach for the analysis of microstrip circuits and to the development of numerical techniques for the modeling of components in planar and quasi-planar configurations. He is an Editorial Board member for the *International Journal of Numerical Modeling* and the *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*.

Dr. Sorrentino is currently an Editorial Board member for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.