An Improved Deep Submicrometer MOSFET RF Nonlinear Model with New Breakdown Current Model and Drain-to-Substrate Nonlinear Coupling

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***Abstract*—An improved deep submicrometer (0.25 μm) MOSFET radio-frequency (RF) large signal model that incorporates a new breakdown current model and drain-to-substrate nonlinear coupling was developed and investigated using various experiments. An accurate breakdown model is required for deep submicrometer MOSFETs due to their relatively low breakdown voltage. For the first time, this RF nonlinear model incorporates the breakdown voltage turnover trend into a continuously differentiable channel current model and a new nonlinear coupling circuit between the drain and the lossy substrate. The robustness of the model is verified with measured pulsed *I–V*, S-parameters, power characteristics, harmonic distortion, and intermodulation distortion levels at different input and output termination conditions, operating biases, and frequencies.**

***Index Terms*—Admittance, analog circuits, avalanche breakdown, capacitance, coupling circuit, harmonic distortion, intermodulation distortion (IMD), modeling, MOSFETs, pulse measurements, resistance, silicon, simulation.**

I. Introduction

THE need for a high-volume, low-cost, and mature technology for wireless communications has propelled increasing use of silicon MOS technology at radio frequency (RF) and microwave frequency. During the past decade, the requirement for high-level circuit integration and higher operating frequencies has motivated prominent advancements in commercial silicon MOS technologies [1]–[3]. The significant improvement of the cutoff frequency (f_T) and the maximum oscillation frequency $(f_{\max})$ has enabled higher frequency of operation and better noise performance. These improvements make silicon MOS technologies attractive for the implementation of RF front ends for mobile telecommunication.

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To design MOS analog circuits that operate at high frequency and low bias voltage, the RF circuit designer needs a reliable and accurate nonlinear device model. Most of the RF nonlinear modeling research for the past two decades has been performed on GaAs MESFETs [4], [5]. Initial ideas for empirical RF nonlinear modeling of silicon MOSFETs have been derived from techniques applied to GaAs MESFETs. As the gate length moves toward the deep submicrometer regime, the characteristics of the device at RF frequencies cannot be accurately modeled using classical approaches such as MOS9 [6] and BSIM3 [7] without incorporating a large number of empirical fitting parameters and additional external circuit elements. This is because conventional short channel models have generally been developed from empirical extensions of physical long channel models.

In addition to the accuracy of the model for the fundamental frequency, the prediction of harmonics and intermodulation distortions should be accurate for the design of multicarrier RF front ends. Most of the well-known problems with earlier empirical MOSFET RF nonlinear models were related to discontinuities in transconductance and output conductance at the boundary between linear and saturation region or between weak and strong inversion conditions. These problems can be resolved by using a single continuously differentiable expression for the drain current for all regions of operation. Several empirical RF nonlinear models have been proposed for silicon MOSFETs with different gate lengths [8], [9]. However, these focused on nonlinear channel current and nonlinear terminal charge modeling. Recently, several models incorporated second-order effects, such as self-heating or breakdown effects in submicrometer RF power MOSFETs [10] and LDMOS devices [11] for power amplifier applications.

However, not much attention has been paid to the second-order effects in deep submicrometer nonlinear MOSFET models at RF and microwave frequencies. As the gate length decreases to the deep submicrometer or ultra-sub-micrometer regime, second-order effects such as breakdown behavior and substrate coupling effects become more important for high-frequency and low-bias operation. We propose an improved deep submicrometer MOSFET RF nonlinear model that incorporates, for the first time, the breakdown voltage turnover behavior in a channel current model

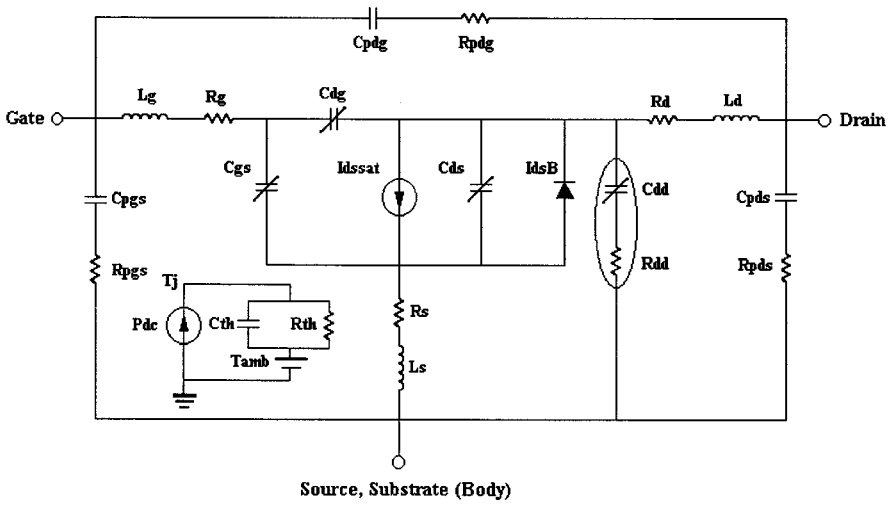

Fig. 1. Equivalent circuit of the proposed deep submicrometer common-source n-MOSFET (10 finger × 25 μm) nonlinear model with new breakdown model and nonlinear substrate coupling. The substrate has electrical connection to the source. The dashed line surrounds the nonlinear coupling network.

with infinite order of continuity. The operating bias point of these devices for today's market demands is expected to be close to the nominal breakdown voltage. Due to the proximity between the nominal drain to source breakdown voltage and the applied bias voltage, a breakdown model that accurately characterizes the breakdown behavior is required to predict large signal operation.

In addition, the output conductance is also affected by the nonlinear capacitance coupling between the drain and the lossy substrate. This model also incorporates a new drain-to-substrate nonlinear coupling network for the accurate prediction of harmonics and intermodulation distortions (IMDs). All the dc and ac characteristics of the device are given by continuously differentiable single-piece expressions. The developed model has been implemented in HP MDS using a symbolic defined model (SDD). Harmonic balance simulation results of the model exhibit good correlation with measured dc, ac, power characteristics, and IMD obtained by load pull measurements at L and C frequency bands.

II. Nonlinear Model

The MOSFET, whose substrate is connected to the source, is widely used for RF power amplifications. The three-terminal model of MOSFET is simple and easy to develop. We have developed a three-terminal nonlinear MOSFET model that is sufficient for RF power amplifier development. The equivalent circuit of the proposed nonlinear model is shown in Fig. 1. This model includes a new breakdown current $I_{\rm dsB}$ with breakdown voltage turnover behavior and a new nonlinear coupling network consisting of a series connection of $C_{\rm dd}$ and $R_{\rm dd}$ between the drain and lossy substrate. This nonlinear substrate coupling is one of the difficulties in MOSFET nonlinear modeling as the operation frequency goes up. The dashed line in Fig. 1 surrounds the nonlinear coupling network. This model also includes temperature dependent nonlinear channel current $I_{\rm dssat}$ and nonlinear capacitance models such as drain-to-gate capacitance $C_{\rm dg}$, gate-to-source capacitance $C_{\rm gs}$, and drain-to-source capacitance $C_{\rm ds}$. The nonlinear channel current and capacitance models have been implemented using continuously differentiable nonlinear models. The pad parasitic elements are represented by the pad capacitances $C_{\rm pdg}$, $C_{\rm pgs}$, and $C_{\rm pds}$ and resistances $R_{\rm pdg}$, $R_{\rm pgs}$, and $R_{\rm pds}$. These pad parasitics are not negligible due to the coupled lossy silicon substrate [12].

A. Nonlinear Channel Current Model

The equation for the drain current is based on the nonlinear channel current model [13] with continuous derivatives with respect to the bias voltages. This channel current equation was previously extended to a temperature-dependent model to incorporate thermal behavior such as self-heating and ambient temperature effects in power MOSFETs [10]. This model [10] focused on building a temperature-dependent channel current model that ensures the continuity of all its derivatives, because the prediction of IMD and harmonics is strongly related to the channel current continuity. This model is summarized by the following equations:

$$V_{\rm gst1}(V_{\rm gs},V_{\rm ds}) = V_{\rm gs} - ({\rm VTO} + \gamma V_{\rm ds}) \tag{1}$$

$$V_{\rm gst}(V_{\rm gs},V_{\rm ds}) = {\rm VST}\ln\left[\exp\left(\frac{V_{\rm gst1}}{\rm VST}\right)+1\right] \tag{2}$$

$$\beta_{\rm eff} = \frac{\beta}{(1+\mu crit\ V_{\rm gst}^{\rm GMEXP})} \tag{3}$$

$$I_{\rm dssat}(V_{\rm gs},V_{\rm ds}) = \beta_{\rm eff}(V_{\rm gst})^{\rm VGEXP}(1+\lambda V_{\rm ds}) \cdot \tanh\left(\frac{\alpha V_{\rm ds}}{V_{\rm gst}^{\rm SATEXP}}\right) \tag{4}$$

$$\Delta T_j = R_{\rm th}P_{\rm dis} + (T_a - T_a^*) \tag{5}$$

$$\beta = \beta_o + \beta_T \Delta T_j \tag{6}$$

$$\gamma = \gamma_o + \gamma_T \Delta T_j. \tag{7}$$

The model parameters are α, β, γ, λ, VTO, VST, $\mu crit$, GMEXP, and SATEXP. Using (2), a discontinuity in derivatives of the drain current expression can be avoided even around the subthreshold conduction region. Equation (3) is used to represent the mobility degradation of the carrier with gate bias voltage $V_{\rm gs}$. The nonlinear channel current model is based on

the hyperbolic tangent function in (4). The gate voltage dependence of velocity saturation is represented by SATEXP.

The temperature dependence of the channel current can be modeled using β and γ, which are expressed in (6) and (7) as first-order functions of the increase in channel temperature. $R_{\rm th}$[°C/W] is the thermal resistance and $P_{\rm dis}$ is the dc power consumption caused by dc biasing voltage. ΔT_j represents the increase in channel temperature. T_a is the ambient temperature at the operating condition, while T_a^* represents the ambient temperature at the time when the device is modeled. The nonlinear channel current model can be slightly modified from [10] to get generalized temperature dependence by adding linear temperature dependent parameters λ, α, VTO, $VB_{\rm on}$, and extrinsic resistances. However, a simple yet sufficiently accurate model for the operation temperature region of interest can be achieved without including all these temperature-dependent parameters.

B. New Breakdown Current Model

For circuit design and reliability analysis, an accurate expression of breakdown current is important. Deep submicrometer MOSFET transistors may be operated at bias points very close to their drain-to-source breakdown voltage. The gate-oxide material limits the maximum allowable electric field on the gate, while the drain-to-source breakdown voltage is dominated by process and device parameters. The drain breakdown can be caused by impact ionization [14], [15] or by the parasitic bipolar transistor [16]. Either infinite multiplication or finite multiplication with positive feedback through the substrate can generate the avalanche breakdown on the drain side of the MOSFET [17].

The difference between these two breakdown modes is the dependence of the breakdown voltage on the gate bias voltage. For the infinite multiplication mode of breakdown, the drain-to-source breakdown voltage increases as the gate bias increases. On the other hand, for the finite multiplication mode, the drain-to-source breakdown voltage decreases as the drain saturation current increases. This trend is physically investigated in [17] and called breakdown voltage turnover or turnaround of breakdown voltage. For accurate performance prediction of deep submicrometer MOSFET transistors operating at low voltage and high frequency, this breakdown voltage turnover behavior should be represented in the channel current model.

To incorporate breakdown voltage turnover behavior in the continuous channel current model [10], a new breakdown model based on [11] is developed. The breakdown starting point of drain-to-source voltage $V_{\rm ds}$ is assigned to $VB_{\rm on}$. Equation (8) represents the breakdown voltage turnover trend with gate bias voltage. The variation of breakdown current shape is expressed by (9). These two equations have a saturation mechanism using the tanh function to help the convergence of nonlinear simulators. This continuous model can predict $VB_{\rm on}$ and breakdown current shape accurately as a function of $V_{\rm gs}$. The new breakdown model is summarized as follows:

$$\begin{aligned} VB_{\rm on}(V_{\rm gs}) = VB_{\rm bd}(A_0+\tanh(A_1-A_2(V_{\rm gs}-VB_{\rm min}) \\ +A_3(V_{\rm gs}-VB_{\rm min})^2 \\ -A_4(V_{\rm gs}-VB_{\rm min})^3)) \end{aligned} \tag{8}$$

$$VB_{\rm shape}(V_{\rm gs}) = A_5(A_6+\tanh(-(V_{\rm gs}-A_7))) \tag{9}$$

$$\begin{aligned} VB1_{\rm on}(V_{\rm gs},V_{\rm ds}) = A_8(V_{\rm ds}-(VB_{\rm on}+A_9)) \\ +A_{10}\,\frac{V_{\rm ds}}{(VB_{\rm on}+A_{11})} \end{aligned} \tag{10}$$

$$IdsB(V_{\rm gs},V_{\rm ds}) = I_{\rm bd}\exp(VB_{\rm shape}VB1{\rm on}). \tag{11}$$

Equation (11) is the breakdown current model with infinite derivatives and breakdown voltage turnover trend. The fifteen parameters $A_0 \sim A_{11}$, $VB_{\rm bd}$, $VB_{\rm min}$, and $I_{\rm bd}$ are model parameters for the new breakdown current model. The minimum value of drain-to-source breakdown starting voltage can be chosen for the initial value of $VB_{\rm min}$ in (8). To make it easier to extract the model parameters of total nonlinear channel current, we separate the channel current into two components: the saturation and the breakdown current components. Using this separation method, we can exclude the coupling between the model parameters of the two current components during extraction. The total nonlinear channel current model is represented as (12), combining (4) and (11)

$$\begin{aligned} \boldsymbol{I}_{\rm ds} = &\text{ Saturation Current Component } (\boldsymbol{I}_{\rm dssat}) \\ &+ \text{ Breakdown Current Component } (\boldsymbol{I}_{\rm dsB}). \end{aligned} \tag{12}$$

C. Drain-to-Substrate Nonlinear Coupling Model

As the operation frequency increases, the high-frequency drain signal couples to the lossy substrate that can be modeled as a reversed biased p-n junction capacitance and substrate resistance. The coupling between the drain and the lossy substrate affects the output conductance in the high frequency regime. Efforts have been made to model the effect of the substrate as an external network [18], [19]. However, sufficient attention was not paid to the nonlinear behavior of the substrate coupling. The drain-to-substrate junction capacitance has a reverse-biased p-n diode characteristic for normal active device operation. The source-to-substrate junction also has a reverse-biased p-n diode characteristic.

In this work, we have focused on the drain-to-substrate nonlinear coupling because the electrical connection between the source and the substrate minimizes the effects of the bias-dependent substrate nonlinear coupling. This coupling can be modeled by using the bias-dependent capacitance and the resistance through the lossy substrate. This nonlinear behavior affects the device output conductance more for a low-resistivity substrate compared to a high-resistivity substrate due to the lossy substrate. We used sample devices on a low-resistivity substrate and modeled the substrate-coupling network using the nonlinear capacitance and the resistance.

We also modeled nonlinear capacitances such as drain-to-gate capacitance $C_{\rm dg}$, gate-to-source capacitance $C_{\rm gs}$, and drain-to-source capacitance $C_{\rm ds}$ using continuous functions similar to the equations in [20]. Equation (13) represents the $C_{\rm dd}$ capacitance model, and B_0–B_3 are the fitting parameters. The other nonlinear capacitances are modeled using (14)–(16). The parameters C_0–C_5, D_0–D_5, and E_0–E_5 are model parameters to describe the nonlinear behavior of the bias dependent capaci-

TABLE I
RF PERFORMANCE AND SMALL SIGNAL EQUIVALENT CIRCUIT PARAMETERS OF THE FABRICATED DEEP SUBMICROMETER (0.25 μm) n-MOSFET WITH TEN-FINGER AND 25-μm GATE WIDTH

DC bias condition		V_{gs}=1.6 V, V_{ds}=2.5 V	
f_T(GHz)		28	
f_{MAX}(GHz)		24	
F_{min}(dB)		0.54 at 4.4 GHz	
R_n(Ω)		31	
G_{ass}(dB)		13	
Γ_{opt}		0.734 ∠43.2°	
Rd (Ω)	5.1	Cdg (fF)	68
Rg (Ω)	9.2	Cds (fF)	157
Rs (Ω)	4.8	Cdd (fF)	175
Lg (pH)	72	Rdd (Ω)	273
Ld (pH)	43	Cpgs (fF)	45.7
Ls (pH)	57	Rpgs (Ω)	22
τ (pS)	2.9	Cpds (fF)	48.7
gm (S)	0.137	Rpds(Ω)	20
Rds (Ω)	90	Cpdg (fF)	4.4
Cgs (fF)	356	Rpdg (Ω)	398

tances. These equations are also continuous functions to help the convergence of the nonlinear simulator

$$C_{dd}(V_{ds}) = B_0((1+\tanh(B_1V_{ds}+B_2V_{ds}^2+B_3V_{ds}^2)) \tag{13}$$

$$C_{dg}(V_{ds},V_{gs}) = C_0(1+\tanh(C_1V_{gs}+C_2V_{gs}^2)) \cdot (1-\tanh(C_3V_{ds}+C_4V_{ds}^2+C_5V_{ds}^2)) \tag{14}$$

$$C_{gs}(V_{ds},V_{gs}) = D_0(1+\tanh(D_1+D_2V_{gs}+D_3V_{gs}^2)) \cdot (1+\tanh(D_4+D_5V_{ds})) \tag{15}$$

$$C_{ds}(V_{ds},V_{gs}) = E_0(1+\tanh(E_1V_{gs}+E_2V_{gs}^2)) \cdot (1-\tanh(E_3V_{ds}+E_4V_{ds}^2+E_5V_{ds}^3)). \tag{16}$$

III. MODEL PARAMETER EXTRACTION

A. RF Performance of n-MOSFET

Deep submicrometer n-MOSFETs were fabricated on a low-resistivity (10 Ω-cm) substrate. Devices with different gate widths and number of fingers were fabricated using National Semiconductor's 0.25-μm twin-well CMOS process on 8-in wafers. For nonlinear model development of the deep submicrometer devices, we chose a ten finger and 25-μm gate width n-MOSFET with common source configuration and substrate connected to source to disable back gate effects. The RF performance and small signal model parameters of this sample are summarized in Table I. The cutoff and maximum oscillation frequencies of this device demonstrate the feasibility of silicon MOS technologies for RF and microwave applications. The device noise performance was characterized using an ATN NP5 system. The values of high-frequency noise parameters such as minimum noise figure $(F_{\min})$, equivalent noise resistance (R_n), and minimum noise input matching point $(\Gamma_{\rm opt})$ are also suitable for implementation of RF and microwave receiver front ends.

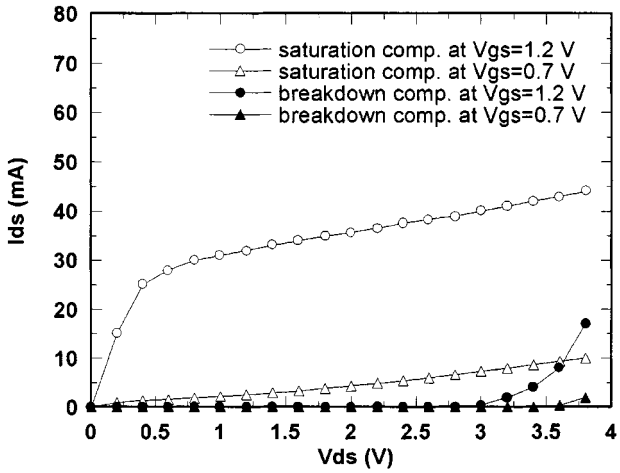

Fig. 2. The extracted saturation and breakdown current components of the measured pulse *I–V* curves at two different V_{gs}.

B. Channel Current and New Breakdown Model Extraction

The drain current is measured using an on-wafer dual-pulse *I–V* measurement system with zero dc bias offset ($V_{gs} = 0$ V, $V_{ds} = 0$ V) for the drain channel current model. The bias trap effects on dynamic *I–V* curves have been well studied for MESFET and high electron mobility transistor devices [21]. Based on the pulse *I–V* measurements, it was found that there were no bias trap effects on dynamic *I–V* characteristics of the measured MOSFETs. The pulse measurement setup is based on the pulse *I–V* measurement system developed in [10]. A short pulse was used to measure *I–V* characteristics. We used 400-ns pulsewidth for the gate side and 200-ns pulsewidth for the drain side with less than 1% of duty cycle. The pulsewidth is chosen to measure isothermal current–voltage characteristic, and the duty cycle is chosen to ensure the thermal stability of the sample device. Therefore, this pulsewidth is much shorter than the nominal thermal time constant of MOSFETs [22].

A pulsed breakdown measurement technique for MESFETs has been presented for nondestructive and isothermal breakdown measurement in [23]. Using on-wafer dual-pulse *I–V* measurements, we have measured the dual-pulse *I–V* curves of the n-MOSFETs, including breakdown region, and have developed a new continuous breakdown current model that incorporates the breakdown voltage turnover behavior. Due to the high thermal conductivity of the silicon substrate, the low-voltage operation, and the medium sample device size, the saturation components of the pulsed *I–V* agreed well with those of static *I–V* curves.

To develop an accurate breakdown model, we have separated the measured pulse *I–V* into saturation current and breakdown current components, which are shown in Fig. 2. The breakdown components are extracted from a comparison between the pulse

TABLE II
SUMMARY OF THE PARAMETERS OF SATURATION CURRENT COMPONENT OF THE TOTAL CHANNEL CURRENT

VTO	γ	*VST*	β	*ucrit*	*GMEXP*	*VGEXP*	λ	α	*SATEXP*
0.81	-0.066	0.07	0.1233	0.02	0.0011	1.1	0.0054	5.6075	0.055

TABLE III
SUMMARY OF THE PARAMETERS OF BREAKDOWN CURRENT COMPONENT OF THE TOTAL CHANNEL CURRENT

VB_{bd}	VB_{min}	I_{db}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
5.85	0.4	3E-5	0.8	0.025	0.94	0.75	0.15	13.2	1.4	1.7E-3	0.62	0.67	1.31	0.85

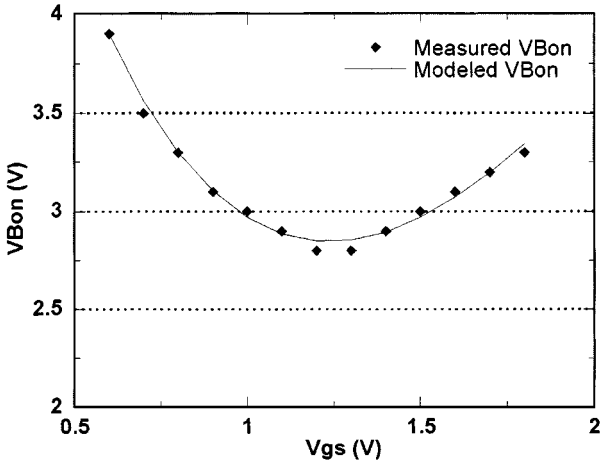

Fig. 3. The measured and modeled breakdown current turn-on voltage ($VB_{\rm on}$) turnover trend with $V_{\rm gs}$ bias voltage.

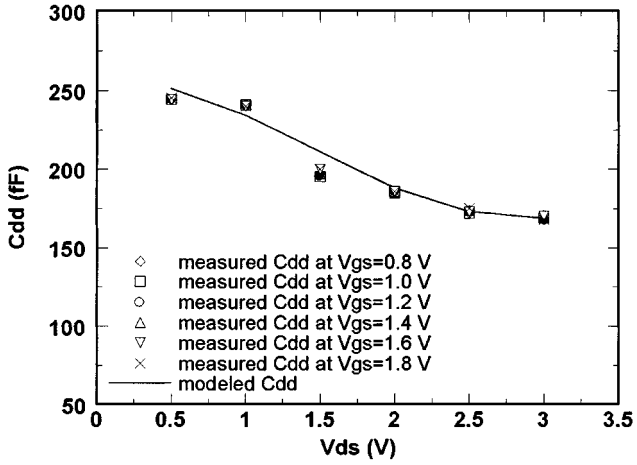

Fig. 4. Extracted and modeled nonlinear drain-to-substrate coupling capacitance $C_{\rm dd}$.

I–V and the saturation components extrapolated beyond each breakdown voltage. The open circles and triangles represent the saturation current components, and the closed circles denote the breakdown current components at two different gate voltages. Because this separation method prevents the coupling of the parameters of the two current components during model extraction, this approach makes it easier to extract the total nonlinear channel current parameters. The drain bias point corresponding to the starting point of the breakdown current is designated as $VB_{\rm on}$. The measured and modeled $VB_{\rm on}$ are shown in Fig. 3, and the trend of this voltage has a negative slope at low gate voltages but positive slope at high gate voltages. This breakdown voltage turnover was modeled using (8). All model parameters in (9) and (10) can be extracted using the measured pulse *I–V* curves after extracting the parameters of (8). The parameters of the saturation current component are summarized in Table II. Table III shows the parameters of the breakdown current component in the total nonlinear channel current.

C. Nonlinear Substrate Coupling and Nonlinear Capacitance Extraction

The bias-dependent S-parameters of the deep submicrometer MOSFETs were measured using an HP8510C network analyzer with a bias source and a monitor. During parameter extraction, parasitic resistances are assumed to be independent of bias. Using the bias-dependent S-parameters, including zero bias measurement, the drain-to-substrate capacitance is extracted at each bias point using the parasitic extraction method presented in [24] and optimized for wide-band tuning to fit measured S-parameters to the equivalent circuit model from 0.1 to 10 GHz. To describe the decrease of the output resistance at RF and microwave frequencies, drain-to-substrate resistance and drain-to-substrate coupling capacitance are incorporated in the equivalent circuit model. After getting small signal equivalent circuit parameters at a certain bias point, the bias-dependent parameters can be obtained by fitting procedures with multibias S-parameters using the values of bias-independent parameters.

The extracted drain-to-substrate coupling capacitance has bias dependence. The plot of the extracted and modeled coupling capacitance is shown in Fig. 4. Using (13), this nonlinear trend has been modeled by a drain-to-substrate nonlinear coupling capacitance as a function of drain bias. The modeled $C_{\rm dd}$ is combined with substrate lossy resistance to build an output nonlinear coupling network as shown in Fig. 1. The other nonlinear capacitances are modeled using (14)–(16). Fig. 5(a)–(c) shows the extracted and modeled nonlinear capacitances $C_{\rm dg}$, $C_{\rm gs}$, and $C_{\rm ds}$. Fig. 6 shows the drain-to-source nonlinear resistance $R_{\rm ds}$ in the small signal MOSFET modeling at each bias point. The total channel current $I_{\rm ds}$ ($I_{\rm dssat}$ and $I_{\rm dsB}$) in the large signal model in Fig. 1 can be equivalently modeled as a

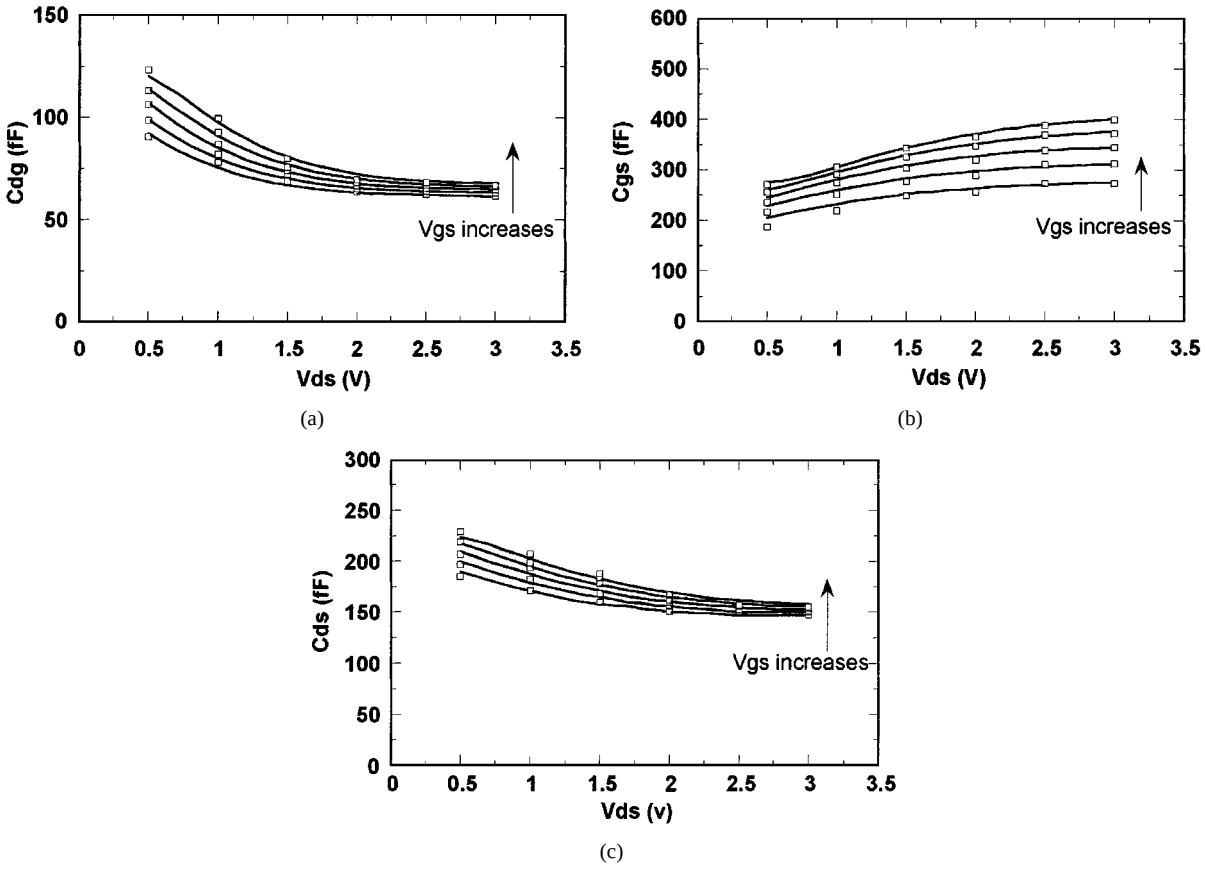

Fig. 5. Extracted and modeled (a) drain-to-gate nonlinear capacitance $C_{\rm dg}$, (b) gate-to-source nonlinear capacitance $C_{\rm gs}$, and (c) drain-to-source nonlinear capacitance $C_{\rm ds}$, $V_{\rm gs}$ sweep from 0.8 to 1.6 V with 0.2 V step.

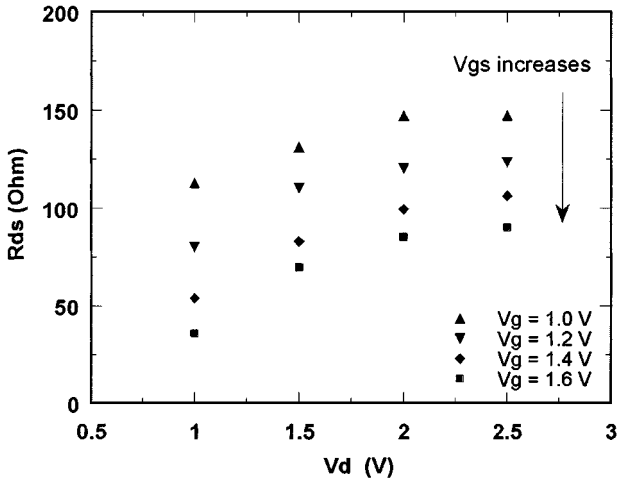

Fig. 6. Extracted nonlinear drain to source resistance $R_{\rm ds}$.

voltage-dependent current source $(g_m v_{\rm gs})$ and drain-to-source nonlinear resistance $R_{\rm ds}$ at small signal conditions. Therefore, the nonlinear behavior of $R_{\rm ds}$ is implicitly incorporated in the total channel current $I_{\rm ds}$ implemented using the SDD in nonlinear simulators.

IV. Model Verification

The robustness of the improved deep submicrometer MOSFET nonlinear model was tested at various termination conditions, biases, and frequencies. Fig. 7 shows the modeled and measured pulse *I–V* including the breakdown region. The open circle shows the measured pulse *I–V*, and the solid line represents the modeled curves. The closed squares denote the breakdown voltage turnover trend in the pulse *I–V*. The breakdown voltage turnover trend is also well described as the gate bias increases. The model shows good correlation with the measured pulse *I–V* even in the breakdown region.

Small signal operation of the developed nonlinear model is verified with the bias-dependent S-parameters. The measured and modeled S-parameters of 10 (finger) $\times$ 25 μm n-MOSFET are shown in Fig. 8. This is a comparison between measured and modeled S-parameters at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2.5$ V. S_{11} and S_{22} are plotted on the lower half of the Smith chart, and S_{21} and S_{12} are plotted on the upper half of the polar plot. The measured data and simulation results show good agreement from 0.1 to 10 GHz. Especially, the output conductance variation with the operation frequency is well predicted up to 10 GHz by the output nonlinear coupling network incorporated into the developed nonlinear model.

We performed load pull measurements, including IMD, using an ATN LP2 load pull system. The measured and simulated fundamental power and harmonics are shown in Fig. 9. The proposed nonlinear model incorporating a new breakdown model and substrate coupling shows good agreement with the measured data. As a comparison, the model without the breakdown model and substrate coupling has been simulated and compared with the measured data. This latter simulation shows a max-

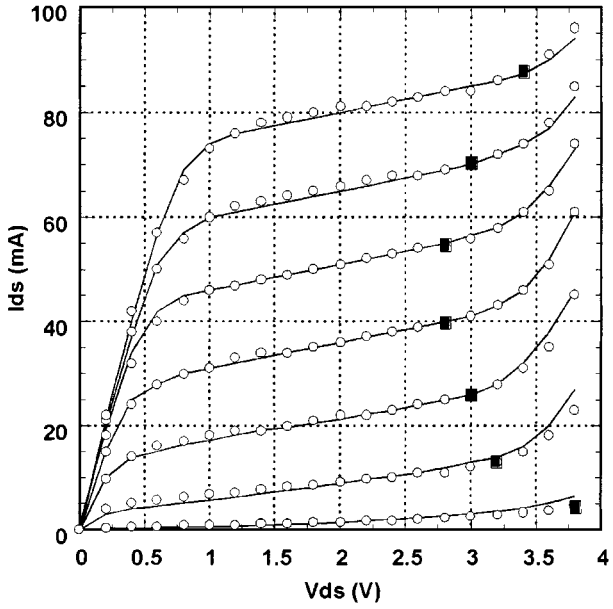

Fig. 7. Measured (circle) and modeled (solid) pulse *I–V* including breakdown current ($V_{\rm gs}$: 0.6–1.8 V, step: 0.2 V). Mark denotes the breakdown current turn-on voltage ($VB_{\rm on}$).

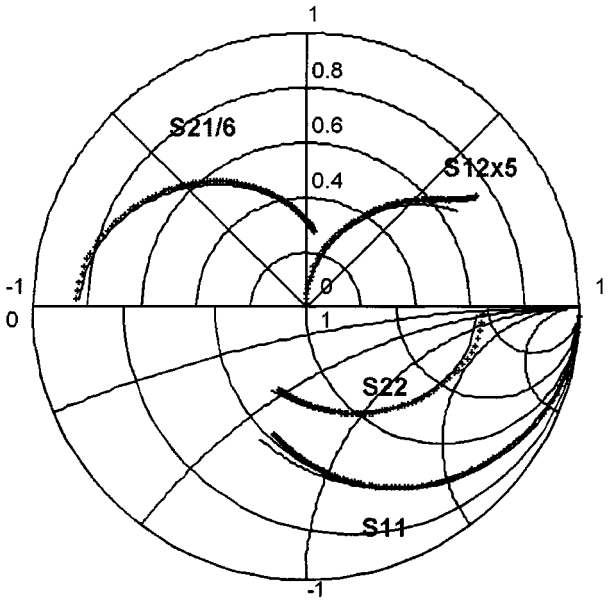

Fig. 8. Comparison of measured (cross) and modeled (solid line) S-parameters at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2.5$ V, $f = 0.1$–10 GHz.

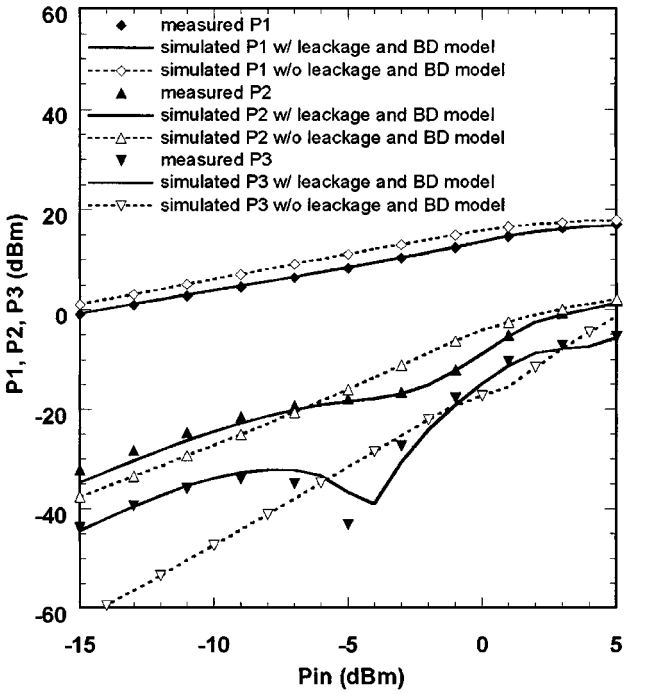

Fig. 9. Comparison of measured fundamental output power (P1), second (P2) and third harmonics (P3), and simulated data with proposed breakdown and substrate coupling model and without these models at $V_{\rm gs} = 1.3$ V and $V_{\rm ds} = 3$ V, frequency = 4.4 GHz, input termination $0.64\angle 80°$, and output termination $0.26\angle 133°$.

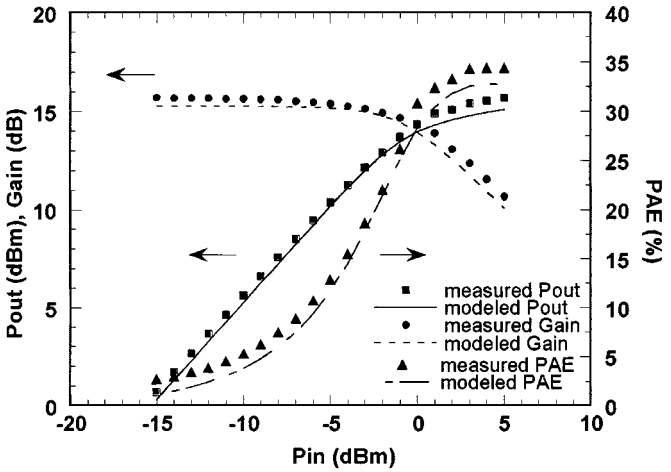

Fig. 10. $P_{\rm out}$, gain, and PAE measured and simulated at $V_{\rm gs} = 1.3$ V and $V_{\rm ds} = 2$ V, frequency $= 4.4$ GHz, input termination $0.66\angle 75.9°$, and output termination $0.28\angle 132°$.

imum 1.5 dB difference in the fundamental output power, a 5 dB difference in the second harmonics, and a 15 dB difference in the third harmonics at 4.4 GHz. As the results have shown, the breakdown current model and substrate coupling are critical for accurate prediction of power characteristics of deep submicrometer MOSFETs. The 4.4 GHz measured and modeled $P_{\rm out}$, gain, and power-added efficiency (PAE) at $V_{\rm gs} = 1.3$ V, $V_{\rm ds} = 2$ V is shown in Fig. 10. The termination condition of this comparison is tuned for maximum output power with the conjugate input termination. The model predicts the power output, gain, and efficiency from small signal operation to well past power compression. These comparisons show that the developed model correlates well with the measured power characteristics at different termination conditions and bias points.

To verify the model prediction capability of the harmonics and intermodulation distortions, we measured the harmonics and intermodulation distortion using the ATN LP2 system. Fig. 11 shows the measured and modeled intermodulation distortions at 4.4 GHz with different gate biases and 0 dBm input power level. The fundamental output power and third- and fifth-order intermodulation distortions are measured at 50 Ω termination and 2 V drain bias. The fundamental output power and third-order intermodulation distortion correlate well

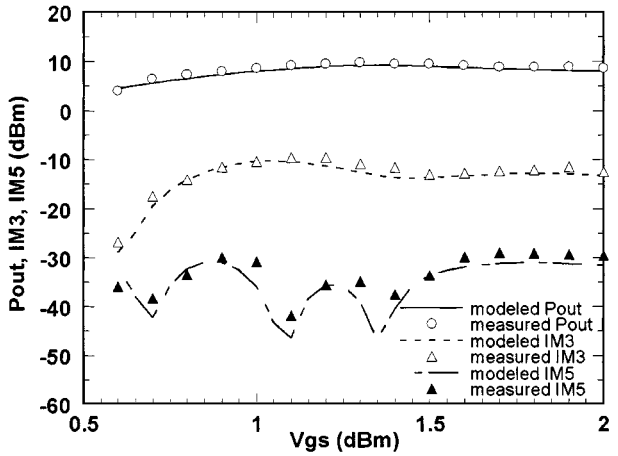

Fig. 11. Fundamental output power ($P_{\rm out}$), IM3, and IM5 measured and simulated by the proposed model using 4.4 GHz and 4.401 GHz, $V_{\rm gs}$ sweep from 0.6 to 2.0 V and $V_{\rm ds} = 2$ V, 50 Ω input and output termination, and 0 dBm input power condition.

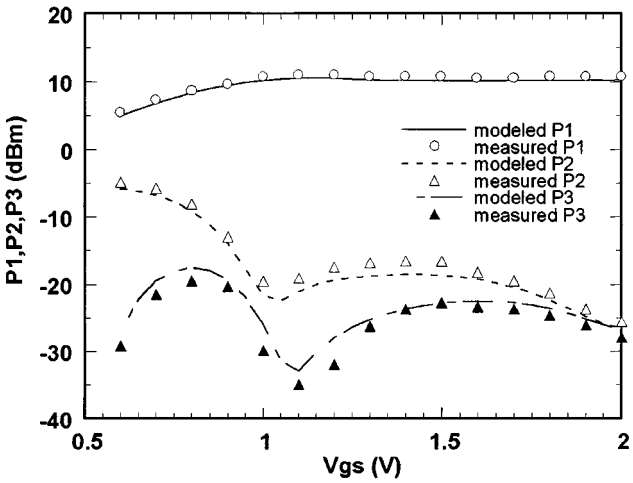

Fig. 12. Fundamental output power (P1) and second (P2) and third harmonics (P3) measured and simulated by the proposed model at 4.4 GHz, $V_{\rm gs}$ sweep from 0.6 to 2.0 V and $V_{\rm ds} = 2.5$ V, 50 Ω input and output termination, and 0 dBm input power condition.

with the measured data, and the modeled fifth intermodulation distortion corresponds reasonably with the measured data between $V_{\rm gs} = 0.6$ V and $V_{\rm gs} = 2$ V.

Fig. 12 shows the measured and modeled harmonics at 4.4 GHz with different gate biases and 0 dBm input power level. The fundamental output power and second and third harmonics are measured at 50 Ω termination condition and 2.5 V drain bias voltage. The fundamental and second harmonics correlate well with the measured data, and the modeled third harmonics correspond reasonably with the measured data between $V_{\rm gs} = 0.6$ V and $V_{\rm gs} = 2$ V. The modeled IMD results using 1-MHz offset and the modeled harmonics from the developed nonlinear model also show good agreement with the measured data at different termination conditions and bias points.

V. Conclusion

An improved deep submicrometer MOSFET RF nonlinear model, incorporating a new breakdown current model and drain-to-substrate nonlinear coupling, has been developed and investigated extensively using various measurements. For the first time, the breakdown voltage turnover behavior has been incorporated in a continuously differentiable channel current model to predict nonlinear operation accurately around the soft breakdown region. Based on a philosophy of the separation of saturation and breakdown components of the nonlinear channel current, we decoupled the model parameters of the two components to enable easy parameter extraction. Frequency dependence of the output admittance is accurately modeled by including a new drain-to-substrate nonlinear coupling network. The robustness of the new nonlinear deep submicrometer MOSFET model has been comprehensively verified through load pull measurements, including IMD and harmonics, at various termination conditions and biases.

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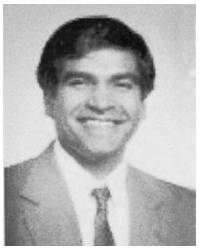

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