# 42% High-Efficiency Two-Stage HBT Power-Amplifier MMIC for W-CDMA Cellular Phone Systems

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***Abstract*—This is the first paper to report on a high-efficiency two-stage heterojunction-bipolar-transistor power-amplifier monolithic microwave integrated circuit (MMIC) for 1.95-GHz wide-band code-division multiple-access (W-CDMA) cellular phone systems. Power amplifiers for W-CDMA systems are required to operate at high efficiency and high linearity over a wide range of output power levels. To obtain high efficiency at low output power ($P_{\rm out}$) as well as at the required maximum $P_{\rm out}$, and obtain a high linearity at the maximum $P_{\rm out}$, we chose near-class-B operation. To improve linearity at a medium $P_{\rm out}$ range, we suppressed the gain distortion resulting from near-class-B operation by using an adaptive biasing technique. The MMIC exhibited a power-added efficiency of 42%, the highest ever reported, a gain of 30.5 dB, and an adjacent channel leakage power ratio at a 5-MHz offset frequency of −38 dBc at a $P_{\rm out}$ of 27 dBm under a supply voltage of 3.5 V with 3.84-Mcps hybrid phase-shift keying modulation.**

***Index Terms*—Amplifier distortion, code-division multiple access, HBT, MMIC power amplifiers.**

## I. Introduction

WIDE–BAND code-division multiple-access (W-CDMA) systems have been receiving a lot of attention as one of the third-generation mobile communication standards intended for global roaming and high-speed data access. W-CDMA systems use a wider frequency spectrum for a higher data transmission rate than that of a system any other current standard, thereby resulting in a requirement for power amplifiers that have a lower adjacent channel leakage power ratio (ACLR), i.e., higher linearity. The efficiency of power amplifiers is also a key requirement. Power amplifiers in W-CDMA systems are required to operate at high efficiency over a wide range of output power levels because the output power of power amplifiers changes dynamically depending on their distance from a base station, and their normal power range during operation is about 10 dB lower than the maximum output power ($P_{\rm out}$). However, the high linearity requirement of W-CDMA systems increases the backoff of output power from its peak value along with a resulting drop in efficiency. Furthermore, the efficiency of power amplifiers decreases rapidly as output power decreases, resulting in low overall efficiency in systems such as W-CDMA having a wide dynamic range of output power.

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To improve efficiency of power amplifiers at low output power levels, the utility of a dc–dc converter as a bias supply was reported in [1]–[3]. To control supply voltage in response to the input signal power by the dc–dc converter, the amplifiers can achieve high efficiency at low output power levels. However, this technique is not very suitable for handset transmitters in cellular phone systems since the size of a monolithic-microwave integrated-circuit (MMIC) chip increases by integrating the dc–dc converter.

To realize both high linearity and high efficiency in power amplifiers, linearization techniques such as pre-distortion have recently been utilized [4]–[6]. The distorted input signal generated by the pre-distortion circuit can cancel amplifier nonlinearity and, thus, the backoff of output power can be reduced and efficiency can improve. However, this technique is very sensitive to amplifier transfer characteristics, such as their temperature and frequency dependence, and is, therefore, not suited for the mass production of amplifiers.

Methodology is described to improve efficiency over a wide range of output power levels while maintaining high linearity. In addition, the power performance of a high efficiency and high linearity heterojunction-bipolar-transistor (HBT) power-amplifier MMIC is described. The MMIC does not use a dc–dc converter or a pre-distortion circuit and, thus, is suited for the mass production of low-cost amplifiers for mobile communication handsets.

## II. Device Fabrication

We used InGaP/GaAs HBTs for a power amplifier because of their high efficiency and high linearity [5]. Fig. 1 shows a cross-sectional schematic of the HBT. The structure of the fabricated InGaP/GaAs HBT grown by MOCVD consists of an $n^+$-InGaAs cap layer, n-GaAs cap layer, n-InGaP emitter layer doped with silicon to a carrier density of $3 \times 10^{17}$ cm$^{-3}$, $p^+$-GaAs base layer doped with carbon to a carrier density of $3 \times 10^{19}$ cm$^{-3}$, n/i-GaAs collector layer, and $n^+$-GaAs sub-collector layer [7].

A WSi emitter electrode was sputtered on the $n^+$-InGaAs cap layer. A Pd/Zn/Pt/Au base electrode was evaporated onto the n-InGaP emitter layer. The base ohmic contact was formed through the thin emitter layer by annealing. This device structure, in which the emitter–base heterojunction is completely covered by the emitter layer, prevents surface recombination on the base and provides high operational reliability. Furthermore,

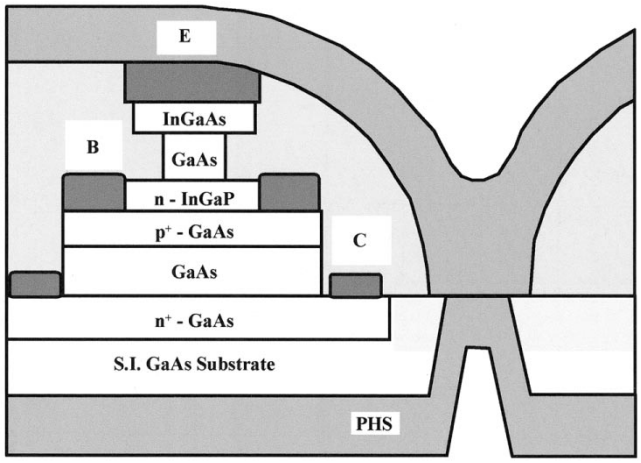



Fig. 1. Cross-sectional view of InGaP/GaAs HBT.

after an AuGe/Au collector electrode was deposited on the subcollector layer, an NiCr resistor, a metal–insulator–metal (MIM) capacitor, and a spiral inductor were formed with two levels of metal. To achieve HBT thermal stability, thick Au plating is used as the second level of metal. Subsequently, after the front-side process is complete, the wafer was thinned and the plated heat sink (PHS) structure was formed. An Au layer was plated on the backside, which was connected to the emitter electrode through via holes.

## III. DC and RF Characteristics

DC and RF measurements were performed on the fabricated HBT with an emitter size of $2 \times 20$ $\mu$m. The collector–emitter offset voltage is 80 mV, which is lower than that of AlGaAs/GaAs HBTs by 0.1–0.3 V. This low offset voltage is caused by the smaller conduction band discontinuity of the InGaP/GaAs emitter–base heterojunction, and it is suitable for operation at low voltages and high efficiency. The collector–emitter breakdown voltage at an open base $\mathrm{BV_{ceo}}$ is 14 V. The $f_T$ and $f_{\max}$ are 40 and 110 GHz, respectively, at a collector current density of $4 \times 10^4$ A/cm$^2$ and a collector bias voltage of 3.5 V. The mean time to failure (MTTF) of our HBTs is $1\times 10^6$ h at a collector current density of $6 \times 10^4$ A/cm$^2$ and a junction temperature of 150 °C [8].

## IV. MMIC Circuit Design

The MMIC circuit was designed using the extracted EEBJT2 large-signal transistor parameter on Libra, a nonlinear microwave circuit simulator. Fig. 2 shows the circuit configuration of a two-stage HBT power-amplifier MMIC. The MMIC consists of a high-pass input matching circuit, driver-stage HBT with an emitter size of $2 \times 20$ $\mu$m $\times$ 10 fingers, high-pass interstage matching circuit, and power-stage HBT with an emitter size of $3 \times 20$ $\mu$m $\times$ 40 fingers. The driver stage and the power-stage HBTs have external base bias resistances of $R_{\mathrm{bex1}}$ and $R_{\mathrm{bex2}}$, respectively. Fig. 3 shows a photograph of the two-stage HBT power-amplifier MMIC.

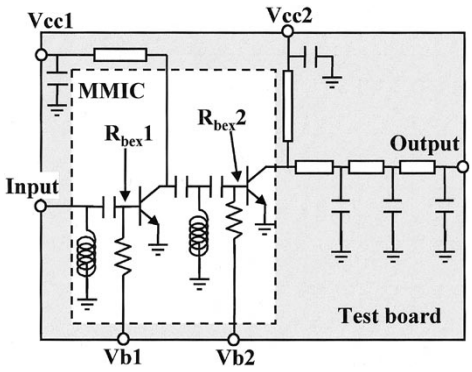



Fig. 2. Two-stage HBT power-amplifier MMIC (diagram).

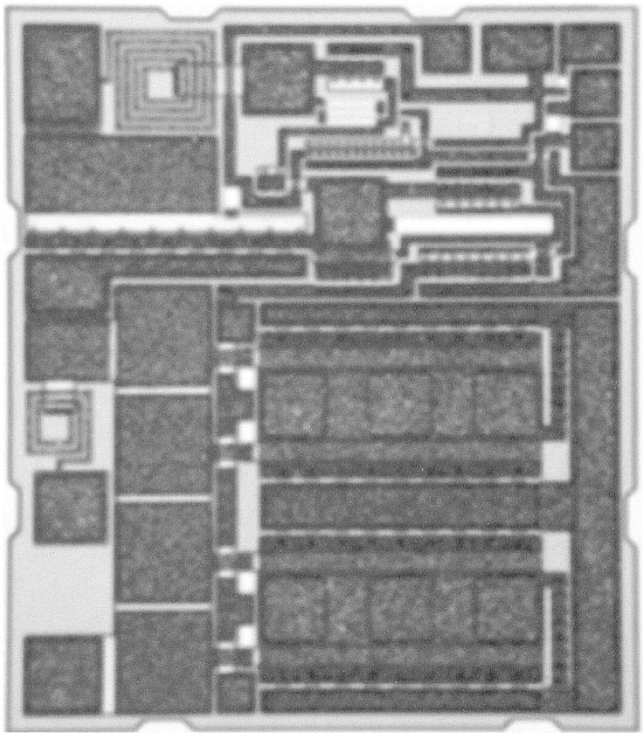


Fig. 3. Two-stage HBT power-amplifier MMIC (photograph).

## V. Analysis of ACLR Behavior under Near-Class-B Operation

W-CDMA systems require highly efficient operation over a wide range of output power levels for power amplifiers. We first analyzed the amplifier operation class dependence of power-added efficiency (PAE) for two-stage HBT power-amplifier MMIC. Fig. 4 shows measured results of PAE dependence on $P_{\mathrm{out}}$ with two quiescent bias conditions. The collector currents of the driver stage and the power stage are 10 and 20 mA, respectively, for near-class-B operation, and 30 and 100 mA, respectively, for class-AB operation. PAE under near-class-B operation is higher than PAE under class-AB operation in the entire range of $P_{\mathrm{out}}$. Under near-class-B operation, the MMIC exhibited a PAE of 42% at the required maximum $P_{\mathrm{out}}$ of 27 dBm and a PAE of 13% at a practical $P_{\mathrm{out}}$ of 17 dBm, which is 10 dB lower than the maximum $P_{\mathrm{out}}$. Meanwhile, under class-AB operation, PAE is 38% at 27 dBm and 8% at

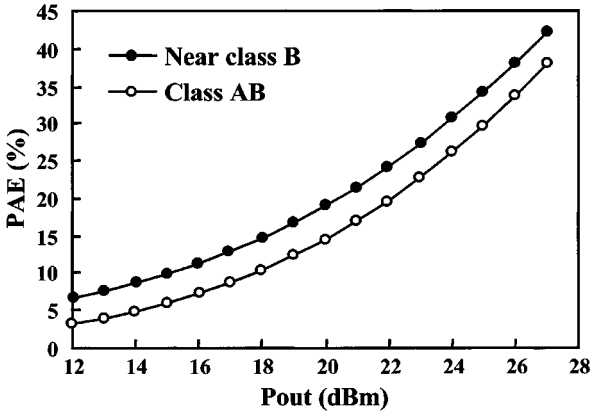
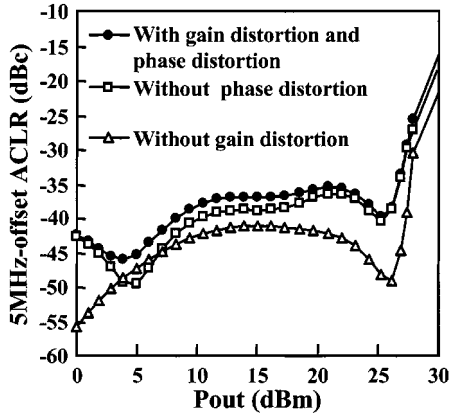
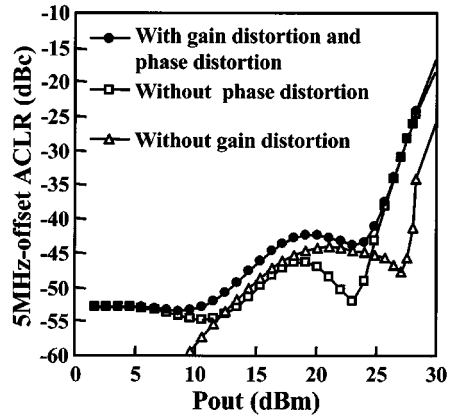



Fig. 4. Measured PAE of MMIC with two bias conditions.




(a)




(b)

Fig. 5. (a) Circuit simulation results for ACLR of MMIC at near-class-B operation. (b) Circuit simulation results for ACLR of MMIC at class-AB operation.

17 dBm. Near-class-B operation is better for higher efficiency at a low $P_{\rm out}$ as well as at the maximum $P_{\rm out}$.

High linearity, i.e., better ACLR, is another key requirement of W-CDMA systems. ACLR is related to amplifier nonlinearity, i.e., gain distortion and phase distortion. The behavior of ACLR under near-class-B operation is discussed below. Fig. 5(a) shows circuit simulation results for the ACLR of the two-stage HBT power-amplifier MMIC under near-class-B operation. As a comparison with the results under near-class-B operation, corresponding simulation results under class-AB

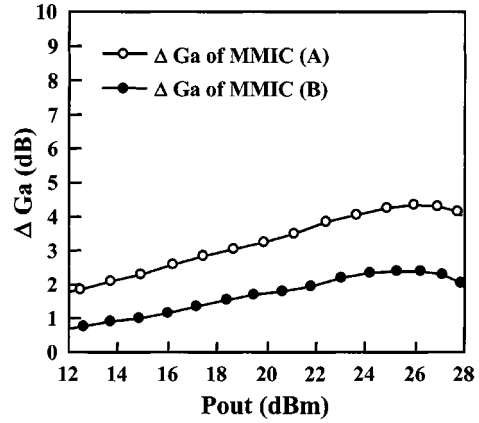



Fig. 6. Measurement results of dependence of $\Delta {\rm Ga}$ on $P_{\rm out}$.

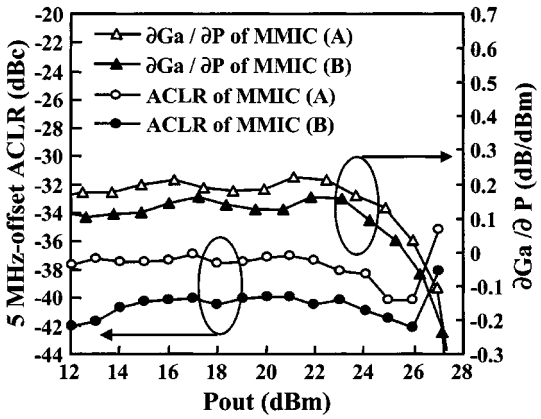



Fig. 7. Measurement results of dependence of $\partial {\rm Ga}/\partial P$ and ACLR on $P_{\rm out}$.

operation are shown in Fig. 5(b). According to the circuit simulations, the behavior of ACLR over a wide $P_{\rm out}$ range is dominated by gain distortion under near-class-B operation, while the behavior of ACLR at a medium $P_{\rm out}$ range is primarily dominated by phase distortion under class-AB operation. Similar ACLR behavior in FET is also reported [9]. Under near-class-B operation, base and collector bias currents increase along with increases in input power, leading to a change in amplifier operation class from B to AB. This enhancement of bias current results in gain expansion, namely, gain distortion, which causes ACLR degradation under near-class-B operation. To improve ACLR under near-class-B operation, we prevented gain distortion in a medium $P_{\rm out}$ range by utilizing an external base bias resistance $R_{\rm bex}$, as shown in Fig. 2. The voltage drop of $R_{\rm bex}\times$ base current substantially suppresses the increase in collector bias current, as well as base bias current. The driver and power stages are self-biased by the voltage drop of $R_{\rm bex}\times$ base current. In other words, $R_{\rm bex}$ suppresses the change of amplifier operation class from B to AB. As a result, gain expansion decreases and ACLR improves. Under near-class-B operation, this adaptive biasing technique is effective at improving the linearity of HBT amplifiers, but it is not effective for FETs because a small amount of gate current causes no voltage drop of $R_{\rm bex}\times$ gate current.

We examined two MMICs, paying close attention to the relationship between gain distortion and ACLR under near-class-B operation. The difference between the MMICs was $R_{\rm bex}$ only.

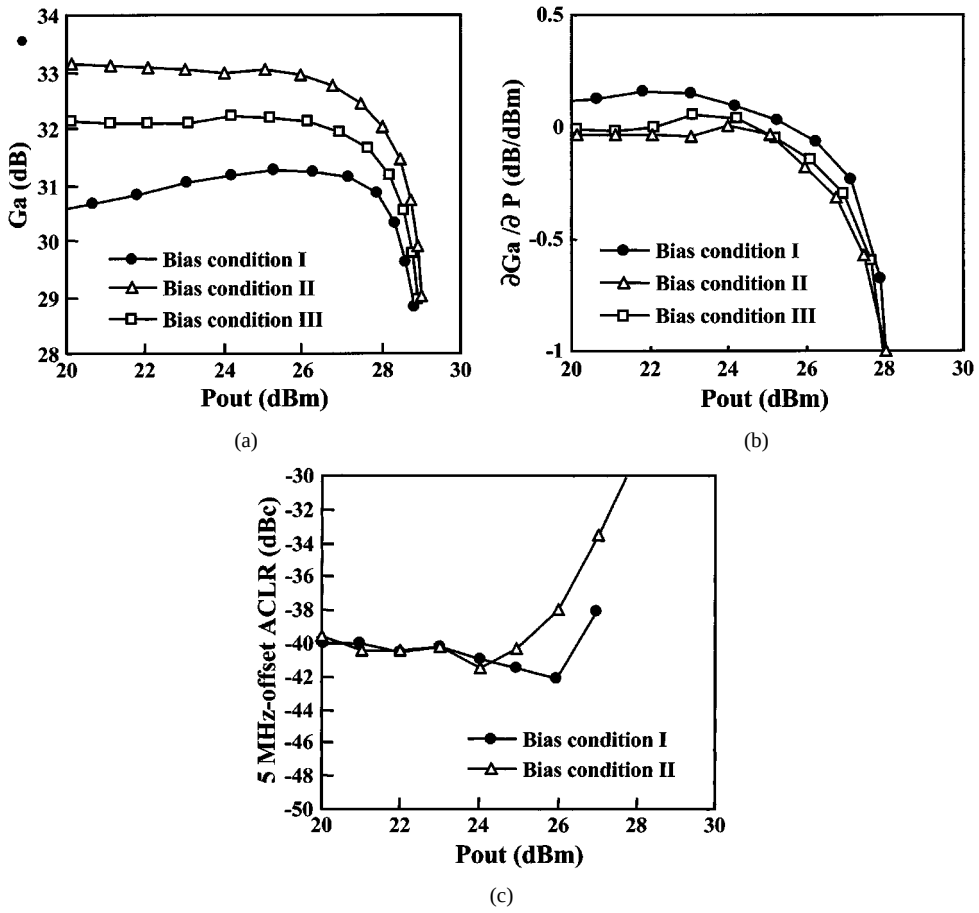



Fig. 8. (a) Measured MMIC gain behaviors near required maximum $P_{\rm out}$ of 27 dBm. (b) Dependence of $\partial {\rm Ga}/\partial P$ on $P_{\rm out}$. (c) Dependence of the measured ACLR on $P_{\rm out}$.

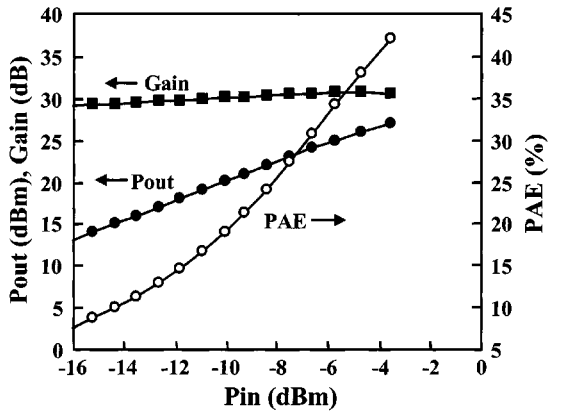
The driver stage has $R_{\rm bex1}$ values of 10 Ω in MMIC (A) and 100 Ω in MMIC (B). The power stage has $R_{\rm bex2}$ values of 2.5 Ω in MMIC (A) and 25 Ω in MMIC (B). Fig. 6 shows measured results of the dependence of gain distortion $\Delta {\rm Ga}$ on $P_{\rm out}$. The MMICs are biased near-class B. The quiescent collector currents are 10 mA for the driver stage and 20 mA for the power stage. Both MMICs exhibited gain expansion due to near-class-B operation. However, the $\Delta {\rm Ga}$ of MMIC (B) is smaller than that of MMIC (A) because the larger $R_{\rm bex}$ value strongly suppresses gain expansion. Fig. 7 shows the dependence of the slope of gain versus $P_{\rm out}$, $\partial {\rm Ga}/\partial P$, and ACLR on $P_{\rm out}$. The $\partial {\rm Ga}/\partial P$ of MMIC (B) is closer to zero than that of MMIC (A) in a medium $P_{\rm out}$ range. The results indicate that $\partial {\rm Ga}/\partial P$ dominates ACLR behavior in near-class-B operation, which agree with the circuit simulation results. The suppression of $\partial {\rm Ga}/\partial P$ attributed to the larger $R_{\rm bex}$ value results in the lower ACLR values of MMIC (B).

## VI. Analysis of ACLR Dependence on an Amplifier Operation Class

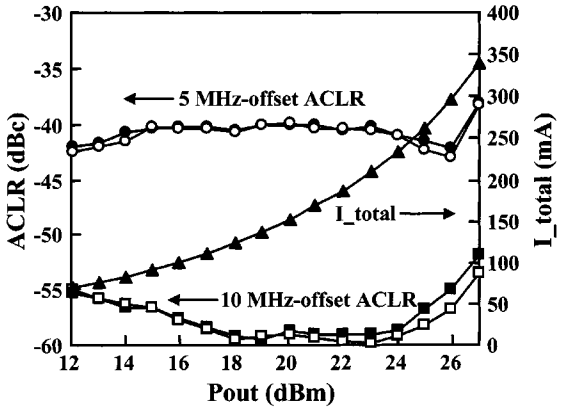
Next, we analyzed the ACLR dependence on amplifier operation class at around the maximum $P_{\rm out}$ required by the system. To increase efficiency at the required maximum $P_{\rm out}$, the output matching circuit is regularly adjusted to match the impedance near optimal efficiency while maintaining acceptable linearity. Fig. 8(a)–8(c) shows the measured gain, $\partial {\rm Ga}/\partial P$, and ACLR behaviors of the two-stage amplifier MMIC at around the required maximum $P_{\rm out}$ of 27 dBm with three quiescent bias conditions. The output matching circuit has been adjusted to matched impedance near optimal efficiency. Bias condition I is near-class B, II is class AB, and III is between I and II. At a low $P_{\rm out}$ value, gain becomes greater as the bias condition changes from near-class B (I) to class AB (II). However, a larger gain causes the decrease of the output power level at which gain starts compressing. Under class-AB operation, gain compression occurs at a lower $P_{\rm out}$ value than that under near-class-B operation, resulting in the behavior of $\partial {\rm Ga}/\partial P$. At the required maximum $P_{\rm out}$ of 27 dBm, $\partial {\rm Ga}/\partial P$ under near-class-B operation (I) is closer to zero than $\partial {\rm Ga}/\partial P$ under class-AB operation (II), and ACLR under near-class-B operation (I) is smaller than ACLR under class-AB operation (II). These results indicate that $\partial {\rm Ga}/\partial P$ dominates ACLR at the maximum $P_{\rm out}$ and near-class-B operation is desirable for improving ACLR at the maximum $P_{\rm out}$, as well as for obtaining a high PAE over a wide $P_{\rm out}$ range.

## VII. Power Performance of Two-Stage HBT Amplifier MMIC

Fig. 9(a) and (b) shows W-CDMA power performance for the two-stage HBT power amplifier MMIC (B) having a larger $R_{\rm bex}$ value. Performance was measured with a 3.84-Mc/s HPSK signal at 1.95 GHz and a supply voltage of 3.5 V. The quiescent




(a)




(b)

Fig. 9. (a) $P_{\rm out}$ gain and PAE versus $P_{\rm in}$ of MMIC (B). (b) ACLR and total current $I_{\rm total}$ versus $P_{\rm out}$ of MMIC (B).

collector currents are as low as 10 mA for the driver stage and 20 mA for the power stage, signifying near-class-B operation.

By utilizing a large $R_{\rm bex}$ value, $\Delta{\rm Ga}$ and $\partial{\rm Ga}/\partial P$ of the MMIC are suppressed. The MMIC achieves a high PAE of 42% and a gain of 30.5 dB with a low ACLR of $-38$ dBc at a $P_{\rm out}$ of 27 dBm. The MMIC also achieves a PAE of 13% with an ACP of $-40$ dBc at a practical $P_{\rm out}$ of 17 dBm, which is 10 dB lower than the maximum $P_{\rm out}$. Use of the adaptive biasing technique and biasing of amplifier for near-class-B operation has realized the high-efficiency and high-linearity power-amplifier MMIC.

The MMIC is expected to be inexpensive because it does not require an additional circuit such as a dc–dc converter, which increases chip size. In addition, the MMIC is theoretically not sensitive to fluctuations of frequency since no pre-distortion circuit is used. Therefore, the MMIC is suitable for a mass-produced low-cost amplifiers in mobile communication handsets.

## VIII. Conclusion

A high-efficiency and high-linearity two-stage HBT power-amplifier MMIC utilizing an adaptive biasing technique for W-CDMA cellular phone systems has been achieved. The external base bias resistance suppresses both the gain distortion $\Delta{\rm Ga}$ and the slope of gain versus $P_{\rm out}$, $\partial{\rm Ga}/\partial P$, which are the results of near-class-B operation. The suppression of $\partial{\rm Ga}/\partial P$ results in a low ACLR value over a wide $P_{\rm out}$ range at near-class-B operation. Moreover, near-class-B operation has been clearly shown to be desirable to improve both efficiency over a wide $P_{\rm out}$ range and linearity at the maximum $P_{\rm out}$ required by the system. The MMIC exhibited a high PAE of 42%, the highest ever reported, a gain of 30.5 dB, and a 5-MHz offset ACLR of $-38$ dBc under a $P_{\rm out}$ of 27 dBm and supply voltage of 3.5 V. The MMIC also exhibited a PAE of 13% with an ACP of $-40$ dBc at a practical $P_{\rm out}$ of 17 dBm, which is 10 dB lower than the maximum $P_{\rm out}$.

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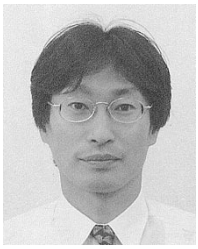

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