Low-Phase-Noise Low-Power IC VCOs for 5–8-GHz Wireless Applications

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***Abstract*—A set of fully integrated voltage-controlled oscillators (VCOs) in the 5–8-GHz frequency range has been designed and manufactured in Si bipolar and Si/SiGe-heterojunction-bipolar-transistor technology. A minimum phase noise of −100 dBc/Hz at 100-kHz off carrier was measured for 2-V supply voltage and 16 mW of power consumption. SiGe VCOs give considerably better phase-noise performance than Si bipolar VCOs for the technologies investigated herein, using similar topologies.**

***Index Terms*—Heterojunction bipolar transistors, inductors, integrated circuits, microwave radio communication, phase noise, silicon, voltage controlled oscillator.**

I. Introduction

VOLTAGE-controlled oscillators (VCOs) are critical building blocks in all communication transceivers. Constraints on phase noise and tuning range are particularly demanding when aiming at fully integrated solutions for wireless applications. A considerable amount of research has been devoted to integrate VCOs in the 0.8–2.5-GHz region, and impressive results have indeed been obtained [1]–[8]. Integrated solutions for cordless standards such as digital European cordless telecommunication (DECT) are already at hand, but for more stringent standards where the constraints on spectral purity are higher, e.g., global system for mobile communication (GSM), requirements are harder to meet. Distributed high-data-rate wireless local area networks (WLANs) are becoming increasingly popular, especially in the 5-GHz bands. Due to the shorter wavelengths in these bands, the necessary geometry to realize integrated reactive devices shrink to dimensions such that fully integrated solution with acceptable quality factors are more feasible. Si-based solutions appear to be dominating in this frequency range [9]–[12].

However, frequency generation at communications bands in excess of 5 GHz is gaining in importance, e.g., for line-of-site microwave communication, satellite communication, and multipoint distribution services. Si/SiGe heterojunction bipolar transistor (HBT) devices have shown excellent potential for these applications and for fiber-optics communication up to 40 GHz [11]–[17]. However, the effort to utilize this technology in wireless communication applications is yet to accelerate. In the higher frequency bands, today, GaAs seems to be the predominant technology [18]–[25]. As an attempt to investigate the potential for Si/SiGe technologies in wireless applications, this paper presents a set of fully integrated low-phase-noise VCOs for use in 5–8-GHz band applications.

TABLE I
BASIC DATA FOR THE TECHNOLOGIES USED IN THIS PAPER

Process Parameter	SiGe Temic	Si Ericsson
f_T (GHz)	50	23
f_{max} (GHz)	50	38
Beta	200	85
V_A (V)	50	20
R_B (kΩ/□)	1.5	6
BV_{CE0} (V)	3.5	5.1
1/f (kHz)	1	35
Sub. (Ωcm)	20	1
Metals	2	4
Isolation	junct.	trench

II. Technology

The VCOs presented in this paper, were manufactured in TEMIC Semiconductor's production Si/SiGe HBT technology [26] or in Ericsson Microelectronics' Si bipolar process.

In TEMIC's technology, the n-p-n devices offer a peak f_T and $f_{\max}$ of 50 GHz, a base–emitter forward voltage drop $(V_{\rm BE})$ of 0.75 V (enabling low supply voltages), and a base pinch resistance of 1.5 kΩ/square. Furthermore, there are two layers of interconnect, several resistor configurations, and nitride capacitors. The technology has already been used to develop several products for wireless applications.

Ericsson's trench isolated Si bipolar process is a well-characterized technology, but as indicated in Table I, offers considerably lower cutoff frequencies. It has an f_T of about 23 GHz and an $f_{\max}$ of about 38 GHz. Moreover, it offers four metal layers, with the topmost layer optionally 3-μm thick, making it suitable for high quality (Q) factor inductor design. On the other hand, the substrate resistivity is much lower than that of TEMIC's (Table I).

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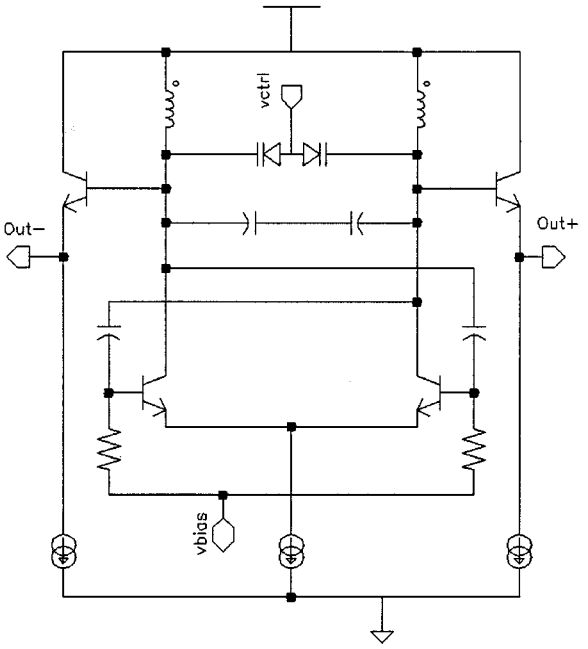

Fig. 1. Simplified schematics of the VCO core.

III. Circuit Design

A differential topology using emitter-coupled pairs with cross-coupled feedback was used to realize the VCOs (Fig. 1). To increase the range of voltage swings in the resonator, without having the transistors entering saturation, either capacitors or emitter followers were used in the feedback path. With respect to setting the dc-operating point of the circuit, two types of designs were made: one using only resistors for current control (type I) and one using transistor-based current sources (type II).

For the SiGe VCOs, the base–emitter junction of the n-p-n–Si/SiGe HBT was used as a varactor diode for tuning of the oscillators, whereas for the Si-based VCOs, a dedicated varactor structure was used. The Q factor of the varactor–diode configuration was simulated to be around 25 at 5 GHz.

Inductor geometry was carefully optimized to achieve high-Q factors without introducing additional masks and processing steps [27]. The highly doped channel stop layer was thus removed from under the inductors to reduce the losses associate with these layers. Additional improvement in the inductor Q factor is achieved by reducing the losses associated with the low resistivity of the silicon substrate. Currents in the inductor strips induce both transverse (between the strips) and longitudinal (along the strips) currents in the substrate. The losses due to these substrate currents are reduced by optimizing the layout of the inductor [28].

This is demonstrated in the example shown in Fig. 2 of a single-turn inductor on a 0.6-Ωcm silicon substrate. In this example, the SiO_2 layer thickness is 5.0 μm and the thickness of the Al strip is 3.0 μm. Q factors reaches a maximum at a certain spacing, i.e., s, between the strips (see inset in Fig. 2). For a given substrate resistivity, oxide thickness, and frequency, this spacing corresponds to an optimum canceling (balancing) of opposing substrate currents, induced by the strips of the inductor.

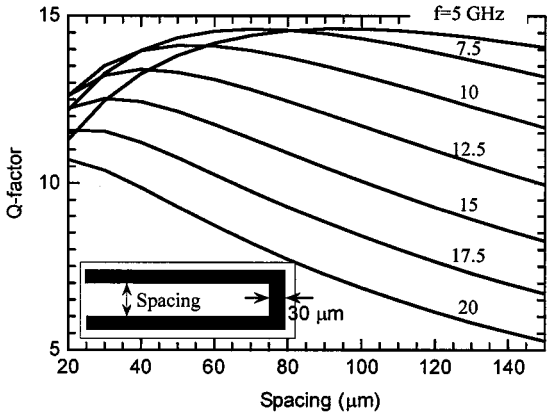

Fig. 2. Simulated Q factor of single turn coil versus strip spacing.

For a spacing larger than the optimum spacing, the Q factor decreases due to the poor balancing of longitudinal currents. For a spacing smaller than the optimum spacing, the Q factor decreases as a result of the increased negative mutual inductance (cf. $Q = \omega L(M)/R$, where L is the inductance including, mutual inductance, M, and R is the series resistance).

Simulation of inductors, including that shown in Fig. 2, was performed in commercially available software (Agilent Momentum). To prove the concept, a large number of optimized test inductors and other passive components have been fabricated and evaluated [29].

Phase noise was simulated and optimized using the periodic steady-state analysis in Cadence SpectreRF, where a linearized noise analysis is performed around a periodically varying operating point. Occasionally the simulations were compared to simulations made in Agilent MDS, taking the worst of mixing and modulation noise. Phase noise was found to agree to within 3 dB between the simulation methods. Pushing factors were also simulated in SpectreRF, by varying the supply voltage and observing the change in oscillation frequency.

Special attention was paid to making the layout of the differential circuits as symmetrical as possible. This is clearly visible in the die photographs of Fig. 3. Furthermore, the inductor layout and their placement relative to the core of the VCO was carefully evaluated. The channel stop layer was thus removed under and around the entire resonator, except in a small area around the varactors. The distance between the inductors was also optimized using the concept of canceling substrate currents. Most of the resonator was surrounded by a sheet of grounded metal to ensure good ground conditions at the center of the differential inductors. The ground metal was kept at a distance of about 100 μm from the resonator to minimize its influence.

IV. Results

The VCOs were wire bonded onto a Cu/Duroid/Brass substrate. A fixture was used to connect the signal and hold the substrate (Fig. 4). Single-ended measurements were performed on one of the differential signals, while the other was terminated by a 50-Ω surface-mounted resistor on the substrate. Twice the

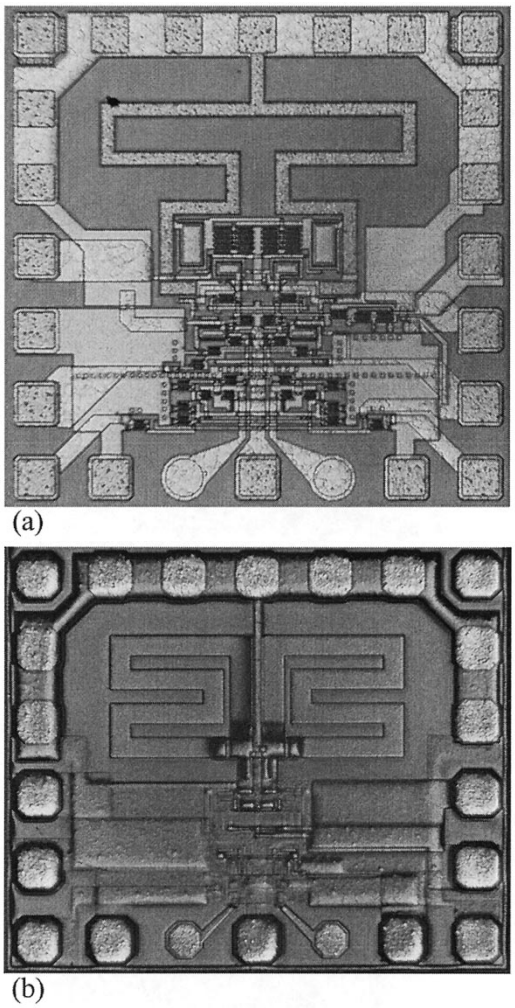

Fig. 3. Die photograph of two of the VCOs, exemplifying two different inductor layouts. (a) 7-GHz SiGe VCO measuring 1×1 mm^2. (b) 6-GHz Si VCO measuring 1×0.85 mm^2.

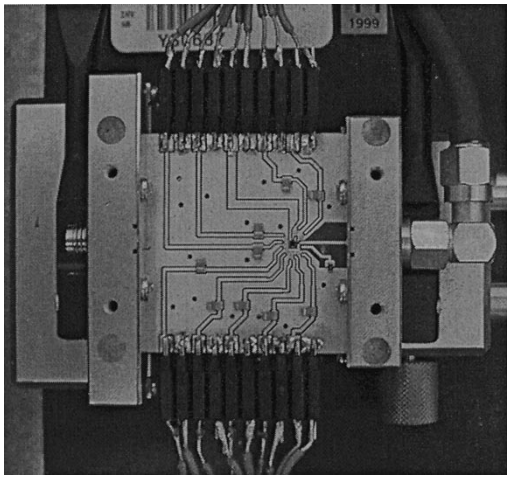

Fig. 4. VCO mounted on measurement substrate and placed in fixture.

TABLE II
SUMMARY OF PERFORMANCE FROM SINGLE-ENDED MEASUREMENTS OF THE DIFFERENT VCOs IN THIS PAPER

VCO	SiGe Type I	SiGe Type II	Si Type I	SiGe Type I
Frequency (GHz)	4.63 - 4.90	4.60 - 4.93	5.59 - 5.94	7.09 - 7.73
Bias (V)	2.0	2.8	3.8	5.0
P_{diss} (mW)	46	152	153	420
P_{diss}^{core} (mW)	16	47	67	110
P_{out}(dBm)	-13	-10	-9	-6
$\mathcal{L}_{100kHz}$ (dBc/Hz)	-100	-94	-90	-88
Pushing (MHz/V)	10	-	100	175
Simulated inductor Q	12	12	17	14
F.O.M [33] (dBc/Hz)	-181	-171	-167	-165

output power, compared to what is given below, is thus available in differential form. In addition, the noise floor is, according to simulations, ~2 dB lower for the differential output than for the single ended. The whole setup is placed in a shielded box with coaxial cable connections to dc supplies and measurement system.

Two different measurement systems were used, a conventional 26-GHz spectrum analyzer with phase-noise option and a Europtest PN9000 dedicated phase-noise measurement system, based on the delay-line discriminator technique. The two measurement systems gave phase-noise results identical to within 2 dB for frequency offsets greater than 70 kHz. For lower offsets, the delay-line technique provides more reliable results.

Best measurement results for the different oscillators are summarized in Table II.

For a first set of type-I SiGe VCOs, a free-running frequency of 4.8 GHz was achieved at 2.0-V supply voltage. The power dissipation was measured to be 46 mW, including buffer amplifiers and the 50-Ω driver. The core of the VCO, including the output emitter followers, consumed only 16 mW of power. The phase noise of the oscillator, under these operating conditions, was measured to be -100 dBc/Hz at 100-kHz off carrier (Fig. 5). The phase-noise performance exhibit little or no sensitivity to supply voltage variations within ± 0.15 V. The variation of the oscillation frequency, during the same experiment, was measured to 10 MHz/V (pushing). When tuning the oscillator within 300 MHz, the phase-noise variation was less than 2 dB. The noise floor was not reached in the measurements, but noise seems to keep falling beyond the -140 dBc/Hz measured at 10-MHz off carrier.

For type-II SiGe VCOs operating at the same frequency, the best operating conditions were achieved already at 2.8-V supply voltage. The phase noise was measured to be 6 dB higher than that of type-I VCOs. The measured power consumption for the VCO core was, in this case, measured to be 47 mW. The difference in phase-noise performance was reasonably well predicted by simulations.

Another set of SiGe VCOs was designed for considerably higher free-running frequencies. Three different VCOs operating at frequencies in the range of 6.0–8.1 GHz were thus demonstrated. These oscillators, all of type I, exhibit somewhat worse phase-noise performance than the 4.8-GHz versions, as exemplified by a 7.5-GHz free-running frequency oscillator in Table II. On the other hand, the tuning range was designed to be

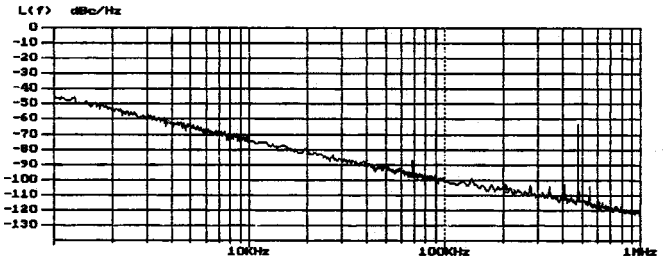

Fig. 5. Phase noise of 2.0-V 4.8-GHz VCO. The spurious signals around 500 kHz are due to ground loops and have subsequently been removed.

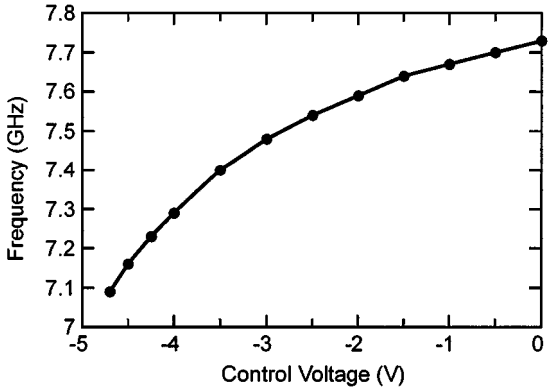

Fig. 6. Tuning performance of a 7.5-GHz VCO.

twice as large, i.e., 600 MHz (Fig. 6). Also, in the feedback of these VCOs, capacitors were used as opposed to the 4.8-GHz VCOs, where emitter followers were used.

Finally a 5.8-GHz type-I VCO was designed in the Si bipolar technology. The topology of this VCO was made identical to the topology of the type-I 4.8-GHz SiGe VCO to facilitate comparison between the technologies. This VCO had a measured phase noise of -90 dBc/Hz at 100-kHz off carrier, significantly worse than the corresponding SiGe VCO. The VCO was originally designed to operate at 3.3 V. The circuit performed reasonably well at 3.3 V, but phase-noise performance was improved by 2 dB if the supply voltage was increased to 3.8 V. At this bias condition, the power consumption is much higher than that of the corresponding SiGe VCO.

V. Discussion

The type-I and type-II 4.8-GHz SiGe VCOs differ only in their implementation of current sources. Therefore, we attribute the significantly higher phase noise of type-II VCOs to originate from the parasitic base–collector and collector–substrate capacitance in the current source transistor of these VCOs. These capacitors allow some of the high-frequency switching voltages present at the emitters of the VCO-core transistors to modulate the current sources, at excess phase conditions, thereby introducing additional phase noise. Simulations showed that the noise sources in the current sources themselves only have a minor impact on VCO phase noise.

The large difference in phase noise between the type-I SiGe 4.8-GHz VCO and the type-I Si 5.8-GHz VCO, despite their identical topology, is quite interesting. First, the slight frequency difference would as a rough estimate account for only 1.6 dB of the observed 10-dB difference in phase noise, using the $20\log(f_2/f_1)$ noise multiplication factor.

A reason for the differing phase noise could be the much higher $1/f$ corner frequency of the Si bipolar process used. Of course, using a single $1/f$ corner frequency extracted from measurements of total output low frequency noise, as a general measure of low frequency noise is not correct, since this is transistor size and bias current dependent. Nevertheless, it is useful as a rough measure of technology performance. However, simulations indicated a much smaller difference in phase noise than measured, i.e., -100 dBc/Hz for the SiGe VCO and -97 dBc/Hz for the Si VCO at 100-kHz off carrier.

Another difference between the SiGe and Si technologies is the substrate resistivity that influences the Q value of inductors and capacitors. However, simulations and preliminary measurements of separate resonator structures, indicate only small differences in Q values (12–15). Nevertheless, substrate coupling between components in the VCO may have an influence on phase-noise performance. However, at this time, we have not been able to perform reliable simulations including these effects.

For the VCOs presented in this paper, there seems to be a correlation between the high pushing factor and high phase noise. A high pushing factor indicates a high sensitivity to disturbances. Since disturbances are difficult to take into account in simulations, a possible increase in phase noise due to this sensitivity may not necessarily be observed in simulations. The reason for the varying pushing factors is not yet fully understood, but simulations give pushing factors that are within 50% of the measured values.

In comparing the 5.8-GHz Si VCO with the 7.5-GHz SiGe VCO a much smaller difference in phase noise between the technologies is observed. However, in the 7.5-GHz SiGe VCO, capacitive feedback was used, whereas in the Si VCO, emitter follower feedback was used. In the comparison between the 4.8-GHz SiGe VCO and the 7.5-GHz SiGe VCO, which differ mainly in the topology of the feedback, it is obvious that the emitter follower feedback gives the lowest phase noise. We have also confirmed this observation in other VCO designs. Therefore, the relevant comparison is between the 4.8-GHz SiGe VCO and 5.8-GHz Si VCO, having identical topologies.

There are two reasons for the higher power consumption required for the Si VCOs to reach optimal performance as compared to the SiGe VCOs. One reason is the higher V_{BE} required to turn on the Si transistor, which, in turn, requires a higher operating voltage. The other reason is the higher biasing current density required to reach the same operating frequency for the Si transistors compared to the SiGe transistors. Taken together, these two effects amount to a considerable difference in power consumption.

From Table II, it can be concluded that the dc–RF conversion efficiency in a 50-Ω system is quite poor. However, the VCOs designed here are primarily intended to be integrated with other circuits, like mixers, dividers, or limiters. These circuits would have fairly high input impedance and mainly requires a reasonable voltage swing. The output of a VCO with on-chip load

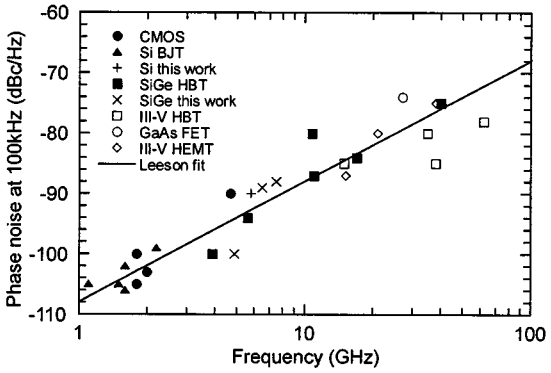

Fig. 7. Literature comparison on phase noise of fully integrated VCOs [1]–[13], [15], [18]–[25]. All data have been normalized to an offset frequency of 100 kHz, using the formula $[\pounds(100\text{ kHz}) = \pounds](f_{\text{offset}}) - 20\log(100/f_{\text{offset}})$ where f_{offset} is the offset frequency (in kilohertz) where phase noise was measured. The solid line represents a fit assuming a slope of 20 dB per decade.

could thus be taken directly from the output emitter followers in the VCO core or possibly through a single buffering stage. The power consumption of the VCO core is thus a more meaningful figure-of-merit (FOM) than the dc-RF conversion efficiency.

The correlation between phase-noise simulations and measurements is within 7 dB at 100-kHz offset frequency. Part of the problem in predicting phase-noise performance, is the difficulty in modeling inductors, capacitors, transmission lines, and pads. In particular, it is difficult to predict the substrate resistance in the presence of substrate inhomogeneities, e.g., due to the blocking of channel stop layers in different parts. Another uncertainty lies in the modeling of low-frequency noise, especially for small offset frequencies. Using a single noise current source in the base–emitter junction to model low-frequency noise, as is done in the SPICE models used here, is an oversimplification, which may add additional uncertainties in the simulations. However, our experience in using more advanced low-frequency noise models, does not show any appreciable differences in phase noise at these offset frequencies.

The crossover from -30- to -20-dB/decade slope in the phase noise versus frequency curve occurs around 30 kHz off carrier, in the SiGe VCOs reported in this paper. This is quite far from the very low $1/f$ corner frequency f_c in the range of 1 kHz reported for this technology [26]. This indicates that f_c does not appear to be the correct parameter to use in Leeson's formula [30] for phase noise, as has been pointed out previously [31].

In Fig. 7, the phase-noise performance of the VCOs presented in this paper is compared to results presented in literature over a large frequency range [1]–[13], [15], [18]–[25]. Only best results of completely integrated VCOs using regular processing techniques were included in the comparison. To aid the comparison on VCOs at different frequencies, a straight line of 20 dB/decade has been fit to the data. Such a frequency dependence of phase noise can be expected from Leeson's formula if indirect frequency dependencies in the Q and effective noise figure are ignored.

Two interesting observations can be made from Fig. 7. First, the results presented in this paper are among the best in relation to its frequency range, all technologies counted. Second, there is no clearly discernible difference in phase-noise performance between the different technologies. Of course such a comparison should be done with great care since operating frequencies, tuning ranges, and power consumption varies between the oscillators. It should also be noted that Si/SiGe bipolar technologies, in general, have the best low-frequency noise performance, whereas III–Vs, in general, have inductors with higher Q value. Nevertheless, the large number of data in Fig. 7 indicates no obvious differences in the overall phase-noise performance between the technologies. This observation tends to favor CMOS VCOs in the lower frequency bands and Si/SiGe VCOs in the higher frequency bands since these are, generally, the least expensive technologies in their frequency bands, respectively.

To benchmark VCOs in different frequency bands and with different power consumption, a FOM given by

$$\text{FOM} = \pounds_{\text{meas}}(f_{\text{offset}}) - 20 * \log(f_{\text{osc}}/f_{\text{offset}}) + 10 * \log(P_{\text{diss}}/1\text{ mW})$$

has been proposed [32]. Here, $\pounds_{\text{meas}}(f_{\text{offset}})$ is the measured phase noise at a frequency offset f_{offset} from the center frequency f_{osc}, and P_{diss} is the VCO power dissipation in milliwatts. Using this definition for the type-I 4.8-GHz SiGe VCO, a FOM of -181 dBc/Hz is obtained. This is, to our knowledge, the best FOM ever published [11], [32] for a fully integrated VCO, using a commercial integrated-circuit (IC) technology.

The FOM of the type-II 4.8-GHz SiGe VCO is -171 dBc/Hz. Although, considerably higher than that of type I, it is still competitive. For the 5.8-GHz Si VCO, the FOM is -167, and for the 7.5-GHz SiGe oscillator, the FOM is -165 dBc/Hz.

It should be noted that the FOM used here does not take tuning range into account. Since there is a tradeoff between the phase-noise performance and tuning range, large tuning-range VCOs, like the 7.5-GHz VCO presented here, are somewhat unfavorably judged.

VI. Conclusion

State-of-the-art performance for low-phase-noise low-power, fully integrated VCOs in the 5–8-GHz frequency range has been achieved. SiGe is thus a suitable technology for frequency generation in wireless applications in this frequency range. For the VCOs reported in this paper, the best SiGe VCOs exhibited considerably lower phase noise than the Si VCOs. It is at this point not possible to conclude if this is due to transistor performance or due to differences in substrate resistivity. By comparing the results obtained in this paper and a large set of literature data on fully integrated VCOs, it is concluded that no clear difference in phase-noise performance can be observed between Si- and III–V-based VCOs.

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