# Suppression of Leakage Resonance in Coplanar MMIC Packages Using a Si Sub-Mount Layer

Sung-Jin Kim, *Student Member, IEEE*, Ho-Sung Yoon, *Student Member, IEEE*, and Hai-Young Lee, *Member, IEEE*

***Abstract*—In this paper, we examined the parasitic leakage resonance of coplanar monolithic microwave and millimeter-wave integrated circuits (MMICs) by the finite-difference time-domain calculations and experiments. The results show that leakages from coplanar MMICs become significantly resonant in finite substrates and packaging enclosures. In order to avoid the leakage resonance, a resonance suppression method using a doped-Si sub-mount layer is proposed and experimented in a frequency range from 0.5 to 40 GHz. The resonance suppression scheme is verified by measuring the $S$-parameters of the fabricated conductor-backed coplanr waveguides having an Si sub-mount layer of different resistivities (1 m$\Omega \cdot$cm, 15 $\Omega \cdot$cm, and 4 k$\Omega \cdot$cm). The leakage resonance can be completely suppressed using the typical 15-$\Omega \cdot$cm Si sub-mount layer.**

***Index Terms*—Conductor-backed coplanar waveguides, coplanar waveguides, leaky wave, MMICs, parallel-plate mode, resonance, silicon.**

## I. Introduction

MODERN microwave and millimeter-wave communication systems such as automotive radars, high-speed wireless LANs, and local-multipoint-distribution-service (LMDS) systems strongly demand low-cost and high-performance integrated circuits and modules [1], [2]. Circuits and modules based on the coplanar waveguide (CPW) are cost-effective and high-performance solutions for those high-frequency systems because they need no backside processing and have compatibility with flip-chip packaging [3].

However, the coplanar devices can suffer from parasitic problems of leakage, coupling, and resonance at their packaging level. For example, a packaged CPW is incidentally modified into a conductor-backed coplanar waveguide (CBCPW) by the package ground plane. The CPW mode becomes leaky by coupling to the parasitic parallel-plate (PP) modes [4]. The leakage in the form of the PP modes reflects at the finite substrate walls and results in substrate resonance and multiple-modes interference [5]. Moreover, electrically large substrates become radiative by the fringing fields at the substrate edges [6]. Shorting vias, low dielectric-constant layers, and suspended structures have been proposed in order to suppress the PP modes [7]–[9]. However, a variety of geometrical discontinuities at last generate incidental leakages in monolithic microwave and millimeter-wave integrated circuits (MMICs) and hybrid modules [10].

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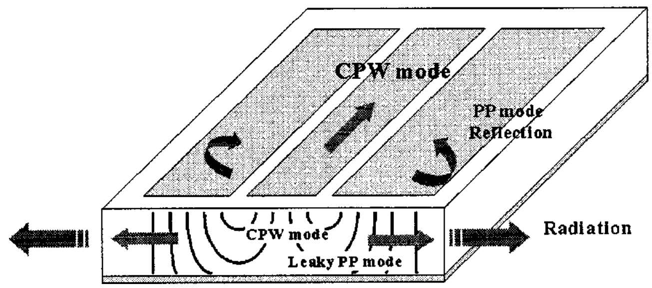



Fig. 1. Substrate reflections and radiations of a finite CBCPW through the PP modes.

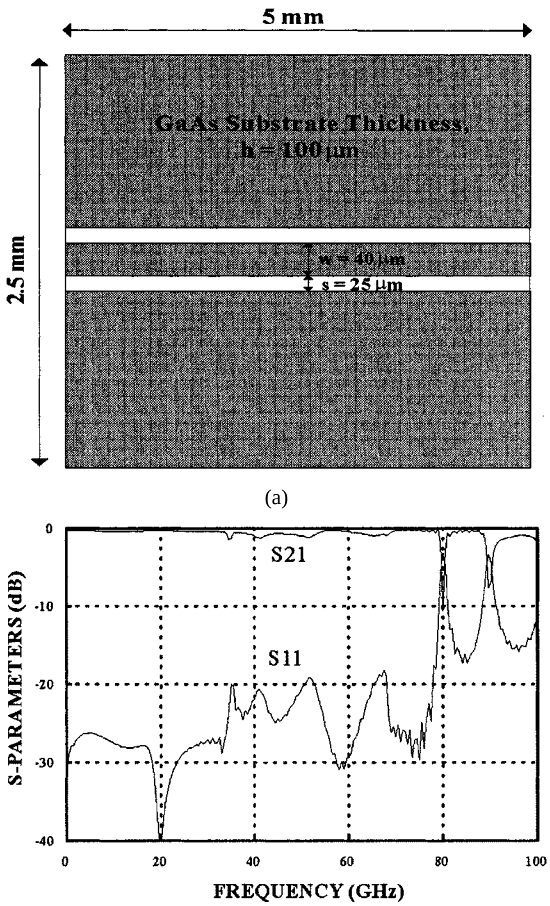
In this paper, the parasitic leakage effects in a CBCPW and in a packaged CPW (CPW in a metal cavity) are examined by the finite-difference time-domain (FDTD) calculations and experimental characterizations of the fabricated GaAs CPWs. We propose the insertion of a doped-silicon (Si) sub-mount layer underneath the CBCPW substrate in order to suppress the leakage resonance. The proper resistivity of the Si is estimated by calculating the surface impedance of the doped-Si layers. The resonance suppression scheme is experimentally verified by characterizing the GaAs CBCPWs with a 500-$\mu$m-thick Si having different resistivities (heavily doped: 1 m$\Omega \cdot$cm, lightly doped: 15 $\Omega \cdot$cm, and high resistivity: 4 k$\Omega \cdot$cm). The results show that the insertion loss of the conventional CBCPW is severely increased by leakage resonance in the finite substrate. However, the parasitic effect can be greatly reduced by using the lightly doped Si (15 $\Omega \cdot$cm) in the microwave and millimeter-wave frequencies.

## II. Substrate and Package Resonance of CBCPW

### A. Substrate Resonance

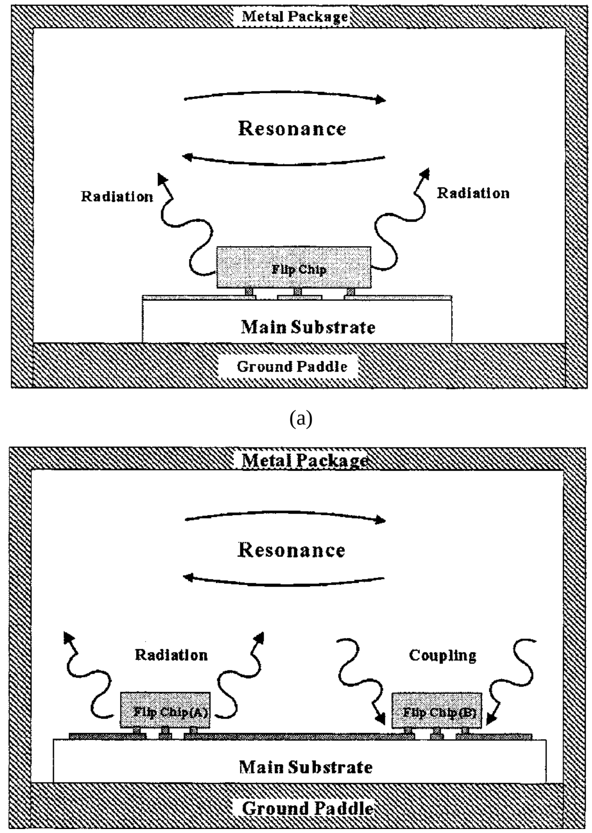
Fig. 1 shows the substrate reflections and radiations of a finite CBCPW by coupling to the parasitic PP mode. This configuration can be easily found in face-up coplanar devices or in main substrates of multichip modules (MCMs). The PP modes propagate into various directions, reflect at finite substrate walls and, consequently, resonate in a finite substrate cavity. The resonating PP modes recouple to and interfere with the propagating CPW mode.

Fig. 2(a) is the top view of a typical CBCPW on a 100-$\mu$m-thick semiinsulating GaAs substrate for the FDTD calculation [11]. The FDTD method is applied by enclosing the device in a three-dimensional perfectly matched layer (PML) box with small openings for the CPW mode excitations. The conductor loss is ignored by assuming a perfect electric




(b)

Fig. 2. Typical CBCPW on a finite GaAs substrate. (a) Top view. (b) Calculated $S$-parameters.




(b)

Fig. 3. Package resonance of the packaged CPWs. (a) Single-chip package resonance. (b) Multichip's package resonance.

conductor (PEC) for the computational efficiency. The signal linewidth ($w = 40$ $\mu$m) and the slot width ($s = 25$ $\mu$m) are chosen for 50-$\Omega$ characteristic impedance $(Zo)$. The CBCPW device is 2.5-mm wide and 5-mm long.

In Fig. 2(b), the scattering $(S)$ parameters are calculated at the CPW ports up to 100 GHz. Above 35 GHz, the $S_{21}$ fluctuates due to the multiple resonances of the coupled PP modes. The insertion and reflection losses of the CPW mode significantly increase at 80 GHz and the severe radiation can be observed by calculating the power loss $(1 - [S_{11}]^2 – [S_{21}]^2)$. The finite CBCPW becomes radiative by the CPW ground planes similar to radiating patch antenna [10]. The radiation can cause an additional package resonance of the coplanar devices housed in conducting enclosures.

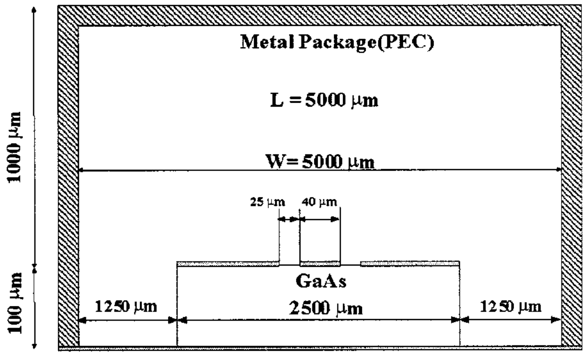
### *B. Package Resonance*

Electrically large CBCPWs become radiative by the fringing fields at the substrate edges. The fringing fields radiate in the forms of the patch modes fed by the parasitic PP modes. These radiated fields resonate in the package cavity and couple to the other devices. Fig. 3 shows two cases of the package resonance, i.e., single-chip package resonance in Fig. 3(a) and multichips package resonance in Fig. 3(b). The devices experience a package resonance in addition to the substrate resonance. The package resonance exhibits lower resonant frequencies than the substrate resonant frequencies because of the larger dimensions. MCMs interconnecting many coplanar flip-chips use very large main substrates and, hence, the severe resonant effects can be observed at lower frequencies.

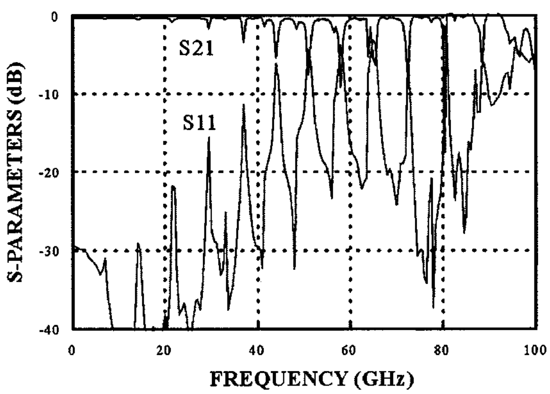
Fig. 4(a) is a packaged CBCPW for the FDTD calculation. The device is enclosed in a three-dimensional PEC cavity with small openings for the CPW mode excitations. The CBCPW has the same dimensions as Fig. 2(a) and the coplanar ground planes are separated from the package walls by 1250 $\mu$m. Fig. 4(b) shows the calculated $S$-parameters. Highly resonating cavity modes are periodically observed at the frequencies where the $S_{21}$ falls deeply. The package resonance is more significant than the substrate resonance above 20 GHz where the substrate radiation becomes significant. The radiation strongly excites the discrete cavity modes [12].

## III. SUPPRESSION OF PACKAGE AND SUBSTRATE RESONANCE

We have found that the leakage of CBCPWs becomes significantly resonant in the finite substrates and in the closed packages in Section II. In order to avoid the parasitic resonance, microwave and millimeter-wave coplanar circuits require accurate control of many dimensional parameters or the leakage suppression schemes. Absorbing materials can be a simple and effective way to suppress the resonance without significantly deteriorating the performance of the coplanar MMICs and modules [13], [14]. Proper dimensional parameters and arrangement of the absorbing materials can be found from the field analysis.




(a)




(b)

Fig. 4. Leakage resonance of the packaged CBCPW. (a) Side view. (b) Calculated $S$-parameters.

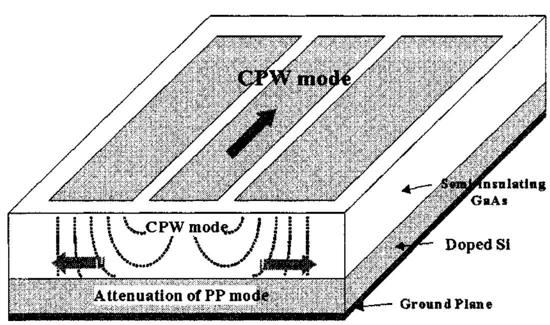



Fig. 5. Suppression of resonant leakage using an Si sub-mount layer.

It is well known that common doped-Si substrates for CMOS integrated circuits are highly lossy in microwave and millimeter-wave applications [15]. However, we could take advantages of the lossy nature to absorb the leakages. In this paper, we insert a doped-Si sub-mount layer underneath the CBCPW substrate in order to suppress the leakage resonance. The absorbing layer scheme is shown in Fig. 5. The lossy Si layer attenuates and absorbs the leakages in the form of the parasitic PP modes. The optimum doping level or resistivity of the Si layer should be estimated without significant deterioration of the CPW mode at a given substrate height. The

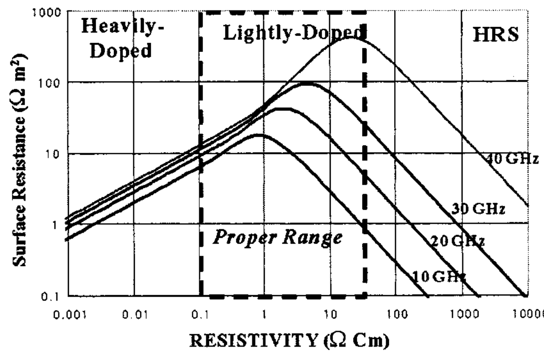
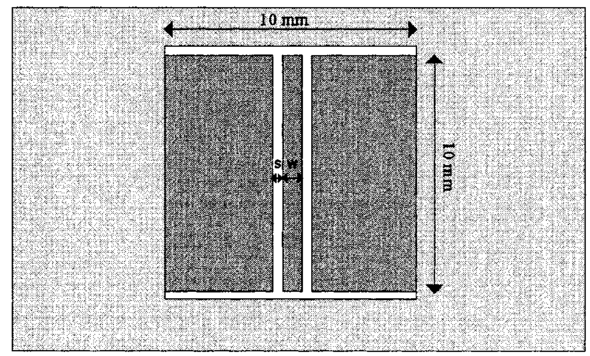
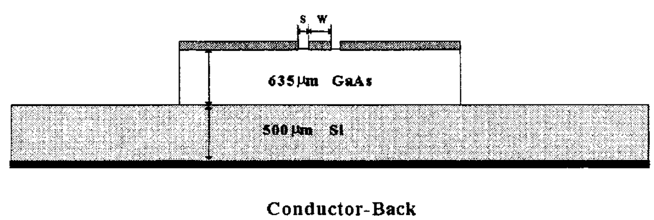



Fig. 6. Surface resistance of a 500-$\mu$m-thick Si layer according to the resistivity and frequency.




(a)




(b)

Fig. 7. Fabricated GaAs CBCPW having a doped Si sub-mount layer. (a) Top view. (b) Side view.

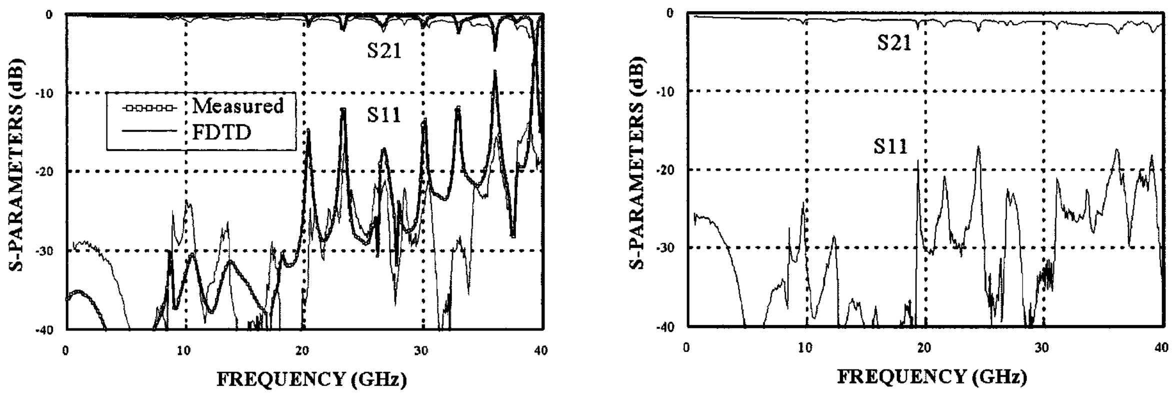
following surface impedance has been derived for a lossy PP mode propagating along the Si layer [16]:

$$Z_S = R_S + jX_S = -\frac{\sqrt{j\omega\mu_O(\sigma + j\omega\varepsilon)}}{\sigma + j\omega\varepsilon} \Bigg/ \left(\frac{1 + e^{2\sqrt{j\omega\mu_0(\sigma+j\omega\varepsilon)}}}{1 - e^{2\sqrt{j\omega\mu_0(\sigma+j\omega\varepsilon)}}}\right)$$

$$\sigma(S/m) = \frac{100}{\rho(\Omega \cdot Cm)}$$

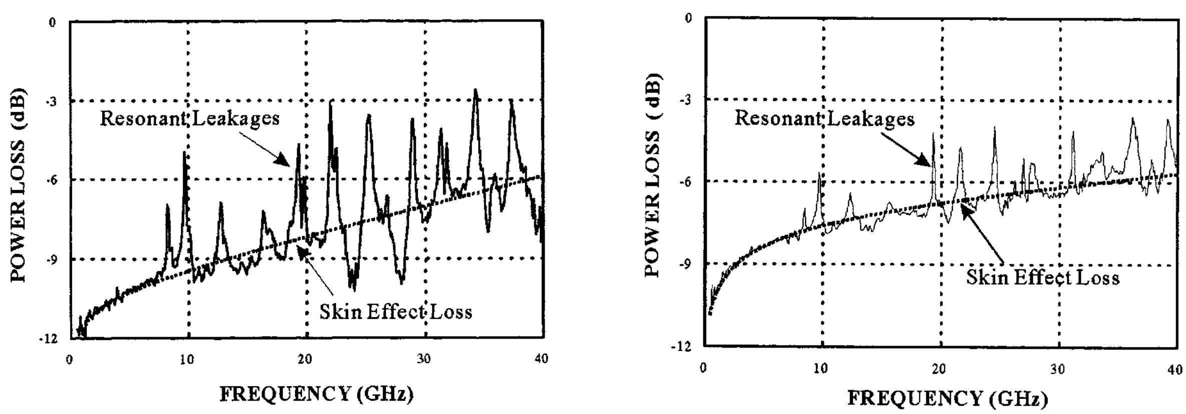
where $Z_S$ and $\varepsilon$ are the surface impedance and permittivity of the Si layer, respectively.

In Fig. 6, the surface resistance is calculated as a function of the frequency and the resistivity for a 500-$\mu$m-thick Si layer. The surface resistance is directly proportional to the attenuation of the PP mode. The typical resistivity from 0.1 to 20 $\Omega \cdot$cm, lightly doped, is the most effective range for attenuating the leaky PP modes.




(a) (b)

Fig. 8. Measured and calculated $S$-parameters of the conventional CBCPWs. (a) $w = 100\ \mu$m, $s = 70\ \mu$m. (b) $w = 70\ \mu$m, $s = 40\ \mu$m.




(a) (b)

Fig. 9. Total loss obtained from the measured $S$-parameters of: (a) $w = 100\ \mu$m, $s = 70\ \mu$m and (b) $w = 70\ \mu$m, $s = 40\ \mu$m.

## IV. Fabrication and Measurement

We fabricated a CPW on a 635-$\mu$m-thick semiinsulating GaAs substrate without wafer thinning and backside metallization. Two strip widths ($w = 100$, 70 $\mu$m) and two slot widths ($s = 70$, 40 $\mu$m) are chosen for the $Zo = 50\ \Omega$. The Cr (200 Å)/Au(1 $\mu$m) deposition followed by a liftoff process is performed on the finite (10 mm × 10 mm) GaAs substrate. The devices are placed on a ground plane of an on-wafer probing station and measured using coplanar probes from 0.5 to 40 GHz. The ground plane behaves as the package ground and, hence, the CPW is modified into a CBCPW.

For the case of the proposed structure, the fabricated GaAs CPW is then attached on a 500-$\mu$m-thick Si using a nonconductive epoxy and placed on the ground metal, as shown in Fig. 7. Three typical resistivities are selected for the Si sub-mount layer; 15 $\Omega \cdot$cm for lightly doped Si, 1 m$\Omega \cdot$cm for heavily doped Si, and 4 k$\Omega \cdot$cm for high-resistivity Si (HRS).

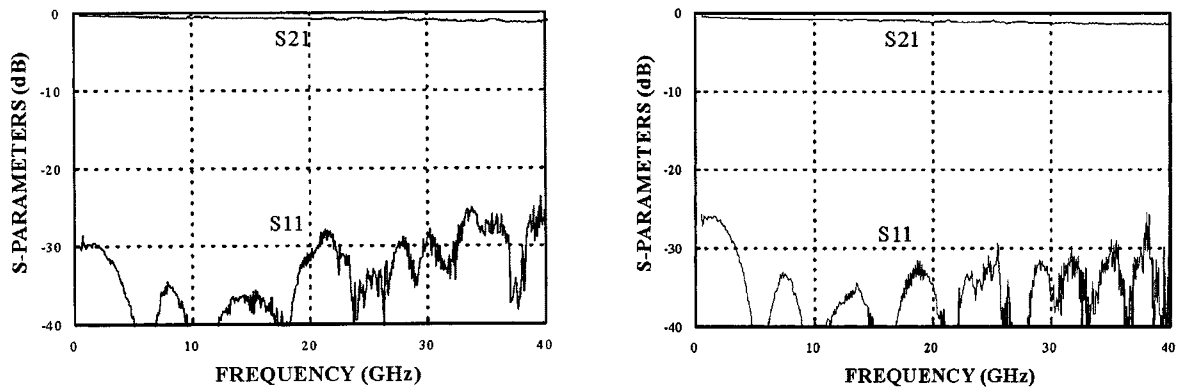
## V. Measured Results and Discussions

In Fig. 8, the $S$-parameters of the conventional CBCPWs are measured and compared with the FDTD results. The wider-slot CBCPW ($w = 100\ \mu$m, $s = 70\ \mu$m) shows more significant fluctuations of the $S_{21}$ by strong coupling to the PP mode [see Fig. 8(a)] while the narrower ($w = 70\ \mu$m, $s = 40\ \mu$m) has less resonant fluctuations [see Fig. 8(b)]. The wider-slot CBCPW also shows the smaller insertion loss, due to the smaller conductor loss of the wider center conductor than that of the narrower-slot CBCPW. The $S_{11}$ peaks can be explained by half-wavelength resonances of the PP mode in the finite GaAs substrate (10 mm × 10 mm × 0.635 mm). The resonant frequencies ($f_{mn}$) can be approximated by the following [17]:

$$f_{mn} = \frac{c}{\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m}{2a}\right)^2 + \left(\frac{n}{2b}\right)^2}$$

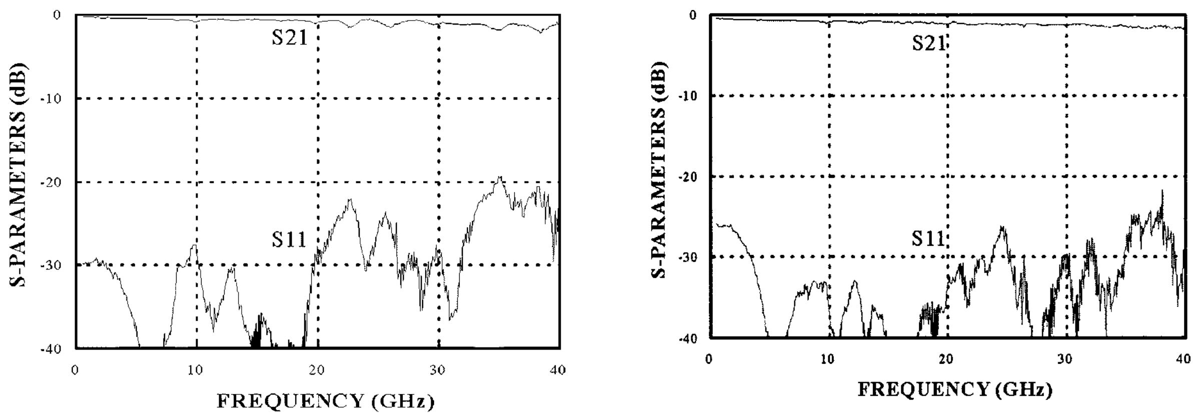
where $m$ and $n$ represent the resonant modal numbers, and $a$ and $b$ are the length and width of the device, respectively.

In Fig. 9, we calculated the total power loss from the measured $S$-parameters using the equation $1 - [S_{11}]^2$–$[S_{21}]^2$. The sharp loss peaks result from the substrate radiation enhanced by the resonant PP modes. The dashed line represents the material loss, mostly by the skin-effect loss. The wider-slot CBCPW shows the slightly lower skin effect loss due to the wider center conductor in Fig. 9(a) than that of the narrower-slot CBCPW in Fig. 9(b). However, the wider-slot CBCPW has more significant resonant peaks by stronger leakage coupling and radiation. These experimental observations show that the leakage resonance could significantly limit the performance of the coplanar microwave and millimeter-wave circuits.



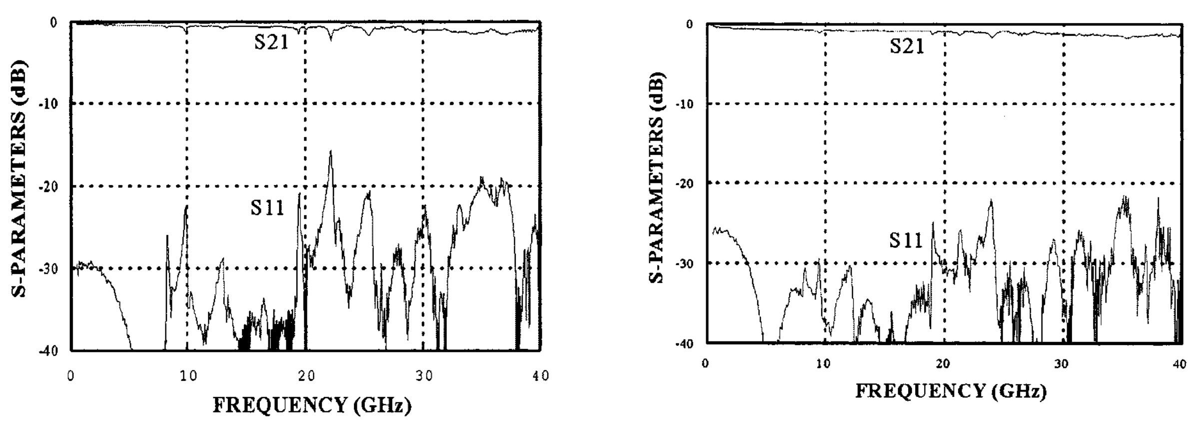

(a) (b)

Fig. 10. Measured $S$-parameters of the CBCPWs having a 15-$\Omega \cdot$ cm Si sub-mount layer. (a) $w = 100$ $\mu$m, $s = 70$ $\mu$m. (b) $w = 70$ $\mu$m, $s = 40$ $\mu$m.




(a) (b)

Fig. 11. Measured $S$-parameters of the CBCPWs having a 1 m$\Omega \cdot$ cm Si sub-mount layer. (a) $w = 100$ $\mu$m, $s = 70$ $\mu$m. (b) $w = 70$ $\mu$m, $s = 40$ $\mu$m.




(a) (b)

Fig. 12. Measured $S$-parameters of the CBCPWs having a 4 k$\Omega \cdot$ cm Si sub-mount layer. (a) $w = 100$ $\mu$m, $s = 70$ $\mu$m. (b) $w = 70$ $\mu$m, $s = 40$ $\mu$m.

The proposed resonance suppression scheme is verified by measuring the GaAs CBCPWs having a 15-$\Omega \cdot$ cm Si sub-mount layer, as shown in Fig. 10. The fluctuations of the $S$-parameters are greatly improved for both CBCPWs as the Si layer absorbs the resonant leakages. The CPW mode is mostly confined around the CPW slots due to their small ratio of the slot width to the substrate height. Therefore, the insertion loss mostly consists of the conductor loss increasing to the square root of frequency. The wider center-conductor CBCPW shows smaller insertion loss in Fig. 10(a) than that of the narrower center conductor in Fig. 10(b). For the wide slot width ($s > 150$ $\mu$m), the CPW mode can be tightly coupled into the Si layer and, hence, the insertion loss increases. The proper ratio of slot width to substrate height can be found from the field analysis of the CPW mode [18]. For the practical applications, the thickness of GaAs and Si layers also requires an optimization by considering the leakage coupling, insertion loss, and thermal management.

Fig. 11 shows the measured $S$-parameters of the CBCPWs having a 1-m$\Omega \cdot$ cm Si sub-mount layer. Smooth fluctuation of the $S_{21}$ is shown near the resonant frequencies of the conventional CBCPWs in Fig. 11(a). This explains that the 1 m$\Omega \cdot$cm Si is too conductive to attenuate the leakage resonance. In Fig. 11(b), the $S_{21}$ of the narrower-slot CBCPW is negligible. Even the very conductive heavily doped Si can be effective to attenuate the very small resonant leakages due to loose coupling to the resonant PP modes.

The measured $S$-parameters of the CBCPWs having a 4 k$\Omega \cdot$cm Si sub-mount layer are shown in Fig. 12. Leakage resonance is not suppressed due to the very small substrate loss of the HRS [19]. Comparing with the conventional CBCPWs, the fluctuations of $S$-parameters are slightly reduced due to smaller coupling to the PP modes in the thick substrate. However, the resonant peaks are still observed in the whole frequencies.

## VI. Conclusions

In this paper, the leakage resonant effects in the finite CBCPWs have been examined by FDTD calculation and experimental characterization of the fabricated GaAs CBCPWs. The results show that the CPW mode couples into the PP modes and the resultant PP modes become significantly resonant in finite substrates and also in package enclosures. In order to suppress the parasitic resonance, we proposed and experimentally characterized the CBCPWs using a doped-Si sub-mount layer for microwave and millimeter-wave frequency applications. The proper resistivity of Si was selected by the surface resistance calculation. Using a 500-$\mu$m-thick lightly doped Si (15 $\Omega \cdot$cm), the fluctuations of $S$-parameters are completely reduced by absorbing the resonant leakages. We expect that the Si absorbing layer can be effectively used for resonant-free coplanar circuits and face-up packages.

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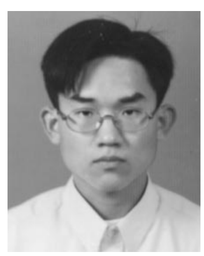

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