Application of Digital PGA Technology to K-Band Microcircuit and Microwave Subsystem Packages

Hongwei Liang, *Student Member, IEEE*, Heidi Langeberg Barnes, Joy Laskar, *Member, IEEE*, and Don Estreich, *Member, IEEE*

***Abstract*—We present for the first time a low-cost high-performance pin grid array (PGA) packaging technology for K-band microcircuit and microwave subsystem packaging. The first-generation package demonstrates a 20-dB return loss to 8 GHz, and the second-generation package improves the return loss to 25 dB from dc to 26.5 GHz. We apply a comprehensive analysis method, which facilitates the optimization of the radio-frequency transition into the package. It combines the time-domain reflectometry analysis and frequency-domain full-wave analysis and reduces the optimization time significantly. The theoretical analysis is verified with measurement in both frequency and time domains. The results demonstrate that the low-cost PGA can be a much more cost-effective microwave packaging solution than the traditional deep cavity metal packages.**

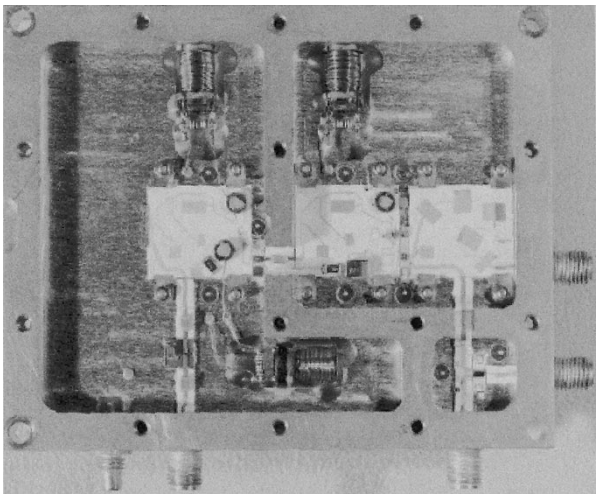
***Index Terms*—Hybrid integrated circuit interconnections, hybrid integrated circuit packaging, multichip modules, optimization methods.**

I. Introduction

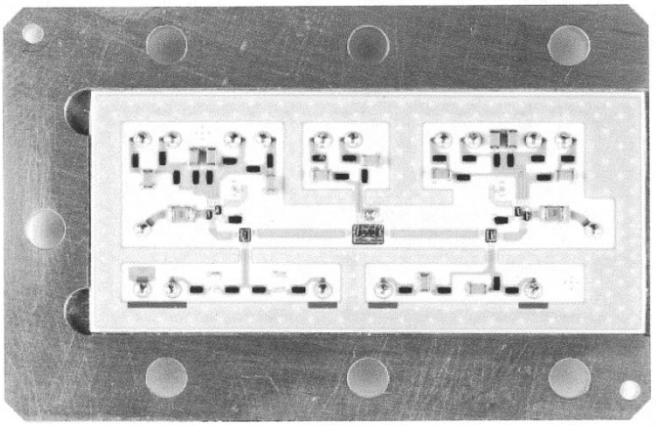
THE COST and performance of microcircuits and microwave subsystems packaging are crucial to a successful microwave product in the highly competitive electronics market. In the fast developing satellite, wireless, and fiber-optic communication area, the trend is that the operating frequency is increasing quickly, the function of monolithic microwave integrated circuits (MMIC) is becoming more complex, and the modules have more dc, radio-frequency (RF), and digital control signal I/O numbers [1]. The higher density of mixed-signal I/Os at higher operating frequency has put a very strict performance requirement on the packages. These demanding requirements include a good RF transition into and out of the package, low loss and low reflection between transmission lines and MMIC, and high isolation between circuit functions in the package.

Traditionally, to meet the requirements, deep cavity metal packages, as shown in Fig. 1(a), are used. The traditional packages are usually expensive and bulky. Their manufacturing process typically starts with a machined metal package with dc feedthroughs and RF glass-to-metal seals. Narrow channels are machined into the package to prevent waveguide modes by operating well below cutoff frequencies to provide good isolation from one circuit to another. Numerous thin-film circuits are attached to the floor of the package using conductive epoxy.

Various ICs are then attached in gaps between the thin-film circuits. Expensive RF connectors are attached to the sides of the package, which form edge launch transitions. Both the placement of the thin-film circuits and the bonding for their connection have to be done manually in the traditional packages, adding cost and reducing the repeatability of the product [2].



(a)



(b)

Fig. 1. (a) A traditional deep cavity metal package (from [2]). The lid is not shown. Note that edge-launch RF connectors are required to provide I/O to the package. These packages can provide high performances at high frequencies, but they are expensive and support low I/O numbers. (b) A microcircuit packaged in MIPPS.

Manuscript received March 6, 2000; revised August 25, 2000. This work was supported by the National Science Foundation (NSF) Packaging Research Center under Contract ECE-9402723 and by the NSF under Career Award ECS-9623964.

H. Liang and J. Laskar are with School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA.

H. Langeberg Barnes and D. Estreich are with the Microwave Technology Center, Agilent Technologies, Santa Rosa, CA 95403-1799 USA.

Publisher Item Identifier S 0018-9480(00)10741-0.

Although this kind of package can provide excellent performance, it has the problem of high manufacturing cost and low I/O counts.

Area array packaging provides a solution to address the need for high-density I/Os of the microcircuits and microwave modules. The pin grid array (PGA) package is one kind of area array packaging technology typically used in very large scale integration (VLSI) systems with a lead count greater than 100 [3]. The PGA package can be insertion-mounted to the sockets of the printed wiring board (PWB) using low-cost process control. This mature packaging technology is a potentially cost-effective solution for RF modules to be mounted on multilayer substrates such as FR-4 and Getek. There are a few literature reports on PGA characterization at low microwave frequencies. Williams *et al.* developed first-order models for a digital PGA package up to 1 GHz by using on-wafer probing techniques [4]. Goodman *et al.* performed characterization of a high-speed PGA package using time- and frequency-domain techniques and reported a maximum 3-dB bandwidth of 2.2 GHz for a signal line in the multilayered PGA substrate [5]. However, there are very few reports on extending PGA technology for higher frequency applications. Dove *et al.*have performed pioneering research on the development and modeling of a PGA package for microwave microcircuits for test and measurement instrumentation [2]. They reported that the pin interconnect has a better than 40 dB return loss at 3 GHz and 15 dB return loss at 10 GHz. For frequencies above 10 GHz, the complex electromagnetic (EM) issues are severe and degrade the performance dramatically.

We demonstrate in this paper that PGA technology can be transplanted to be a low-cost solution for even higher RF frequencies in K-band. In this paper, the emphasis is to develop a second-generation PGA interconnection that has excellent electrical performance to 26.5 GHz. In the next section, the package architecture is introduced. In Section III, we perform EM analysis on the first-generation PGA interconnect presented in [2] and optimize its return loss to 22 dB at 10 GHz. In Section IV, we present a new interconnection configuration, which is measured to have a better than 20 dB return loss to 20 GHz. This interconnection is successfully optimized to have a return loss better than 25 dB at 26.5 GHz using a comprehensive analysis method.

II. Microwave PGA Package Architecture

The PGA package developed by Agilent Technologies is called the multichip integral-substrate PGA package solution (MIPPS). A sample microcircuit packaged with MIPPS is shown in Fig. 1(b). The MIPPS mainly consists of a metal baseplate, a single piece of ceramic substrate, and a metal lid. An exploded view of the package assembly is shown in Fig. 2. The 0.095-in metal baseplate is designed for simplified machining processes with a slight recess on top to serve as the housing for the substrate. The baseplate is made from 416 stainless steel to minimize the thermal coefficient of expansion (TCE) mismatch with the ceramic substrate. A 0.006-in conductive silver-filled epoxy preform is required between the baseplate and the substrate to insure mechanical stability from

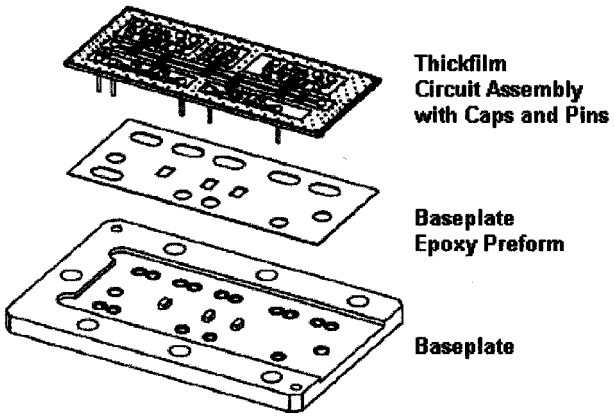


Fig. 2. The exploded view of MIPPS.

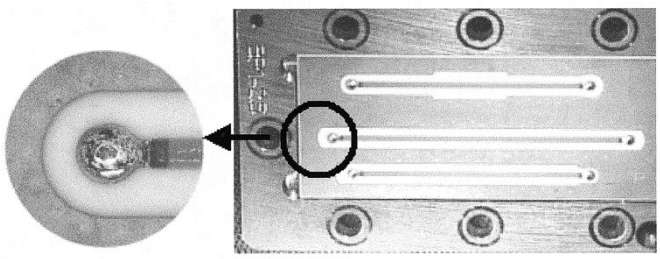


Fig. 3. Prototype MIPPS with first-generation soldered pin interconnection.

−55 to 150 °C. Gold-plated kovar pins of 0.020-in diameter are vertically connected to the microstrip to form the RF transitions for the microcircuits. To test the performance, some prototypes with 50-Ω microstrip substrates in MIPPS package are built, as shown in Fig. 3. On the backside of the substrate, a circular area of the grounding metal around the pin is pulled back to serve as a ground relief clearance between the pin and the ground. The vertical pins then go through the machined holes in the metal baseplate where a short airline coax section is formed, as shown in Fig. 4. In the first-generation MIPPS interconnection, both the dc and the RF pins are connected to the microstrip using a hemisphere of solder. The pins are all located on a 0.100-in grid, which makes for convenient assembly on PWB or testing in widely available PGA testers. A 0.025-in-thick alumina substrate is used in the MIPPS prototype structures. ICs can be attached directly to the thick film or mounted on pedestals that come up from the machined baseplate through laser-drilled cavities in the thick film. All bonded interconnections are easily automated on this flat single substrate surface. The RF pin can be plugged directly into the PWB if a low-RF-loss PWB is being used, or to a subminiature A (SMA) connector (either barrel or flange mount) if the RF signal is to be sent or received through a coaxial cable.

To obtain good isolation between the circuits on the ceramic substrate, hundreds of conductive filled vias that connect the bottom ground plane of the circuit with the ground metallization on the top are placed surrounding the RF signal lines, as shown in Fig. 6(a). A lid with cavities below cutoff frequency for isolation is then epoxied directly to the substrate using the conductive epoxy preform. When plugging an MIPPS into

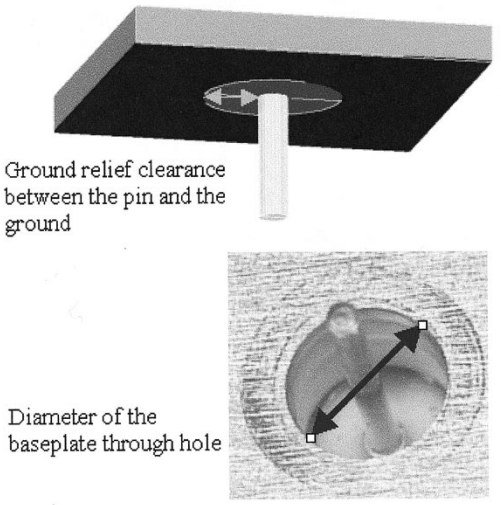


Fig. 4. RF pin goes through the microstrip substrate and the baseplate. Two parameters affecting the electrical performance are also pointed out.

sockets on a PWB, a metal waffle gasket is inserted between the MIPPS and the PWB to improve the isolation between the dc feedthroughs and the RF transitions. In addition, the dc pins can be kept uncoupled from the stray RF energy using low-cost surface-mount components in the module and can be plugged into single-contact sockets on the PWB [2]. This high degree of isolation is critical for the performance of some products, such as the 130-dB solid-state step attenuator module manufactured with the MIPPS packaging technology and used for a 4-GHz signal generator. Another example of MIPPS products is an electronic calibration module that operates from 30 KHz to 9 GHz [2].

The MIPPS packaging architecture is more cost effective and more reliable than a traditional deep cavity metal package. First, MIPPS uses much fewer expensive RF connectors than traditional packages. Secondly, MIPPS applies low-cost thick-film processes and low-cost pin interconnections to microcircuit design. MIPPS modules have all the microcircuits fabricated on a single piece of substrate, which provides significant cost advantages when compared with the numerous thin-film circuits used in traditional microcircuit modules. A thick-film circuit that has both conductors and resistors printed on it generally costs only 10–25% as much as a similar thin-film circuit [2]. Lastly, the MIPPS package takes advantage of automated assembly techniques for improved reliability over the manual placement and lineup of thin-film circuits in traditional packages.

III. First-Generation Interconnection for 10-GHz Application

In the first generation of the pin interconnect, the top of the pin is soldered to the 50-Ω microstrip lines using a 0.052-in circular solder pad, which can provide sufficient mechanical robustness, as shown in Fig. 3. For measurement purpose, the bottom of the pin is inserted into a high-performance SMA connector.

The HP8510C network analyzer is used to obtain the S-parameters of the prototype. A finite-element method (FEM) tool

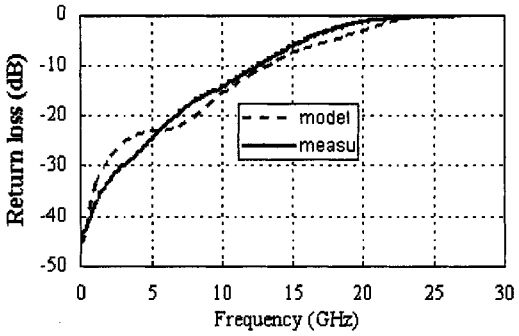


Fig. 5. Measured and modeled performance of the first-generation MIPPS package with soldered pin interconnection.

suitable for simulating arbitrary three-dimensional (3-D) geometry objects is used to perform EM modeling and analysis [6]. Fig. 5 shows the measured and modeled performance of the interconnection. This soldered pin transition exhibits a return loss better than 20 dB below 8 GHz. The return loss at 10 GHz is 15 dB, which is acceptable for many commercial applications. However, the return loss degrades quickly above 12 GHz.

A careful EM analysis has been performed on the interconnection by virtue of the field-displaying capability of the EM tool. It reveals some electromagnetic phenomena, which explains why the interconnection is not efficient for signal propagation at high frequency. Since the vertical pin makes the field transition from the microstrip to the coax line, two EM field view planes across the pin are chosen: one is inside the alumina substrate and is located 10 mil below the microstrip signal line; the other is across the middle of the baseplate through hole, as shown in Fig. 6(a). The E-field at these two planes is snapshot at 10 and 26 GHz, respectively, and is displayed in Fig. 6(b) and (c). From Fig. 6(b), the E-field at 10 GHz is much stronger at the pin side opposing the microstrip, and this phenomenon is more significant at 26 GHz; furthermore, the E-field energy tends to dissipate into the whole substrate at higher frequencies. From the field distribution at view plane 2, the E-field does not have a radially symmetrical transverse electromagnetic mode (TEM) wave pattern, and the dissymmetry becomes more severe at 26 GHz compared with at 10 GHz, as shown in Fig. 6(c). Time-domain reflectometry (TDR) measurement has shown a capacitive region near the solder ball, which indicates that the solder ball is a major factor in limiting the performance of the interconnect at higher frequencies.

From several experiments, we find that the performance of the interconnection is sensitive to the geometrical parameters, including the baseplate through hole diameter and the circular relief in the ground plane of the alumina. The 3-D EM tool [6] helps to determine the optimal values for these two parameters. The capacitance of the solder ball can be offset with some inductance by changing the two parameters. The optimized diameter of the ground clearance is between 140 and 200 mil, and the diameter for the hole in the metal baseplate is 90 mil. Fig. 7 shows the dependence between the return loss and those two parameters at 10 GHz. It shows that the return loss of the transition can be improved to 22 dB at 10 GHz. A prototype transition with a 143 mil-diameter ground clearance is fabricated according to

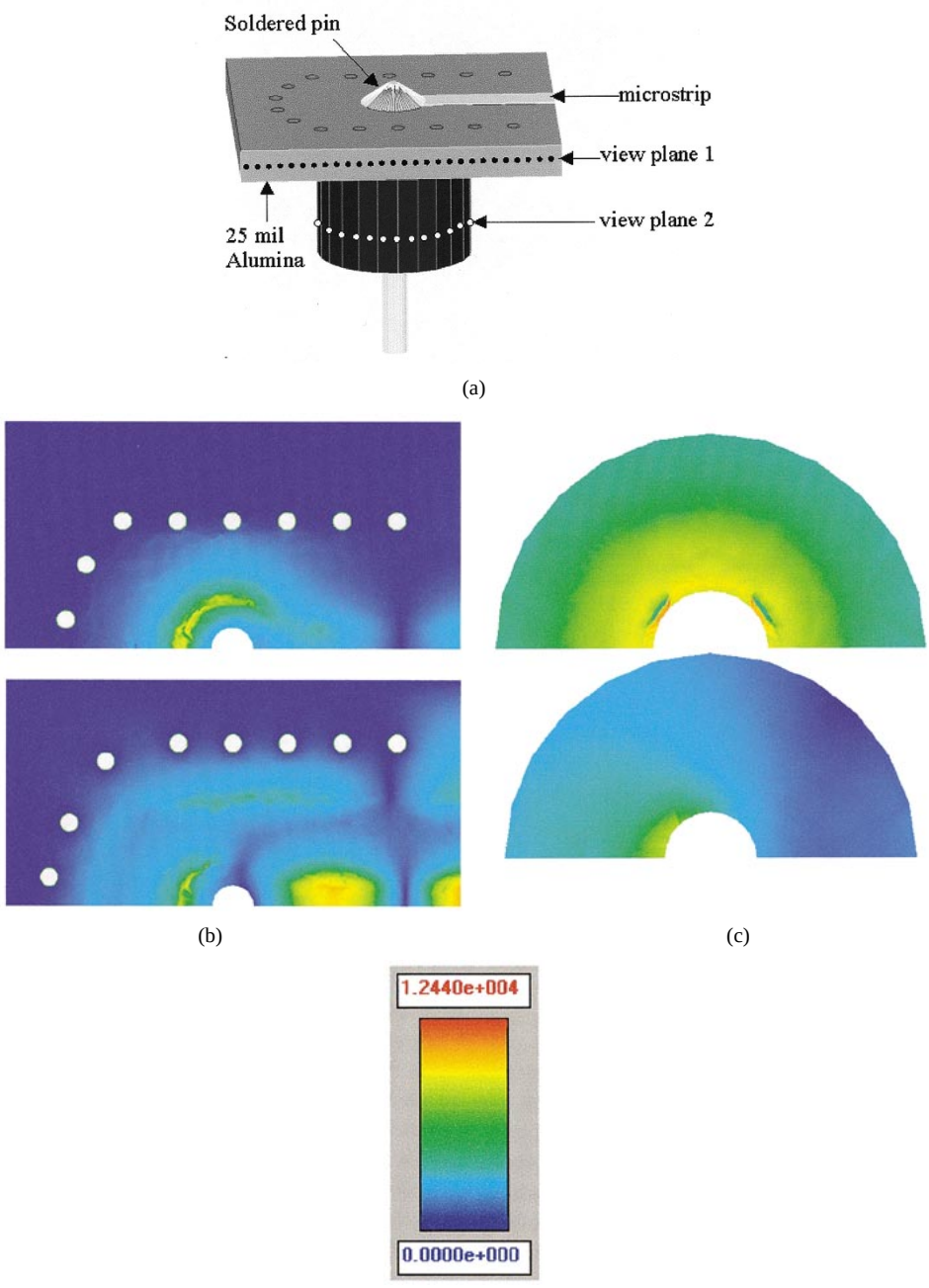


Fig. 6. Full-wave analysis of the first-generation interconnection. (a) Three-dimensional HFSS model for the first-generation MIPPS interconnection. Two planes are chosen to perform full-wave EM analysis. (b) E-field energy tends to propagate into space at high frequency, as seen at plane 1. (top) $f = 10$ GHz and (bottom) $f = 26$ GHz. (c) E-field shows a noncylindrically uniform pattern in the baseplate through hole at plane 2. (top) $f = 10$ GHz and (bottom) $f = 26$ GHz. (d) Scale of the electrical field.

these optimized data, and its measurement data confirms the optimization result. TDR from the measurement and simulation data also shows good agreement, as shown in Fig. 8.

IV. Second-Generation Interconnection for 26.5-GHz Application

A. Design

We have developed a second-generation interconnection that successfully improves the operating frequency to 26.5 GHz. In the new interconnection, the solder ball is replaced with a short ribbon bond as the electrical path from the microstrip to the pin, thereby removing the parasitic capacitance of the solder. The hole in the thick-film alumina substrate is made significantly larger than the pin to reduce capacitance, and the pin is placed eccentrically in the hole to minimize the length of the ribbon bonds, as shown in Fig. 9. The cross-section view at the symmetrical plane of the interconnection is shown in Fig. 10. The metal baseplate is machined with a hole that is different from that in the first-generation interconnection. The top 19 mil of the hole is drilled with a 46-mil radius. This hole, together with the pin, forms a coax line with a characteristic impedance of 50 Ω. The

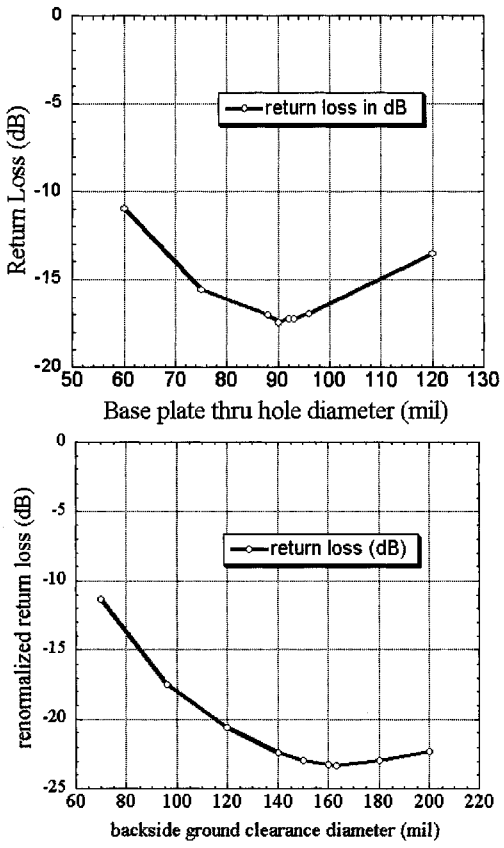


Fig. 7. The performance of the first-generation MIPPS interconnection is sensitive to the baseplate through hole diameter and the backside ground relief diameter. Optimization result shows that the return loss can be improved to 22 dB at 10 GHz.

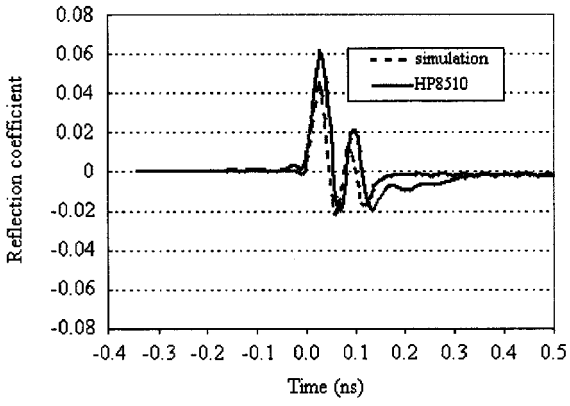


Fig. 8. Measured and modeled TDR response of the optimized MIPPS soldered pin interconnection matches very well.

hole is then made larger to accommodate a 50-Ω hermetic seal, which provides mechanical support for the pin as well as higher electrical performance. In the prototype, the edge-to-edge distance from the pin to the ceramic is 10 mil.

The HP 8510C network analyzer is used to obtain the performance of a prototype interconnection. The 3-D EM model

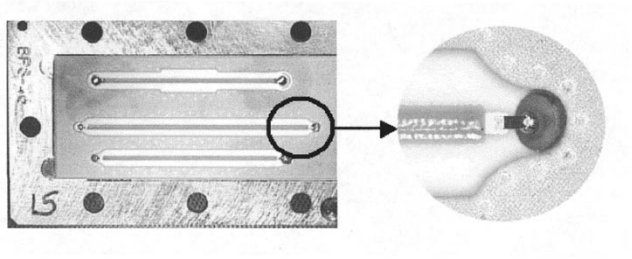
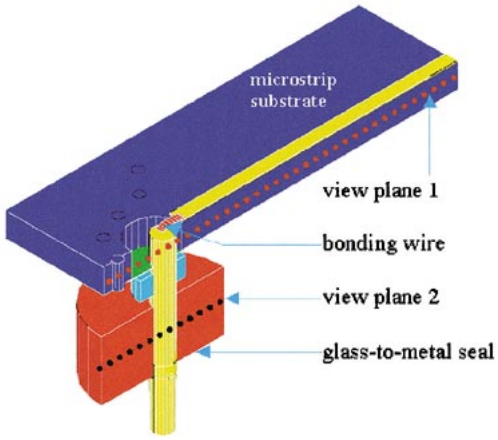
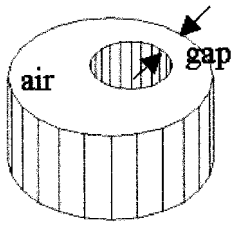


Fig. 9. Test structure of the second-generation MIPPS interconnection with ribbon bond.



(a)

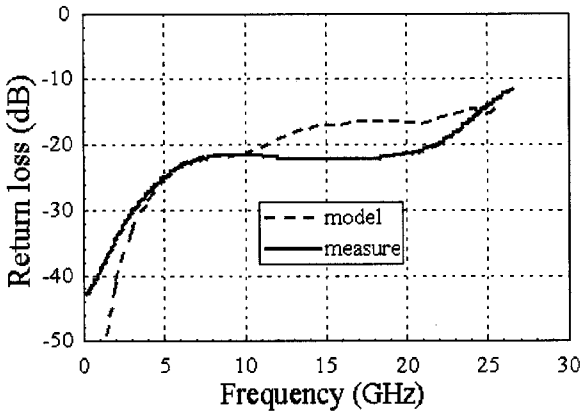


(b)

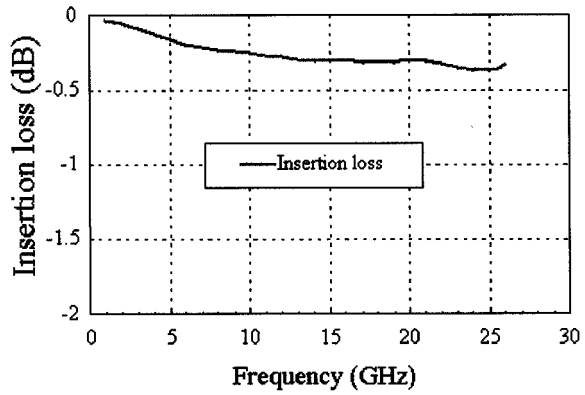
Fig. 10. (a) 3-D HFSS model for the second-generation MIPPS interconnection. (b) The pin is placed eccentrically in the substrate hole.

predicts the performance quite accurately. Fig. 11 shows the return loss and the insertion loss. The measured return loss is better than 20 dB from dc to 20 GHz, and the insertion loss is well below 1 dB to 26.5 GHz. EM analysis is also performed on this second-generation interconnection. Similar to that in Section III, two view planes are chosen: one is 10 mil below the microstrip line in the substrate and the other is across the 50-Ω hermetic seal, as in Fig. 10. The E-field distribution is observed both at 10 and at 26 GHz. Fig. 12(a) shows the E-field across the substrate.

Compared with that in the first-generation interconnection (Fig. 6), we see that the interconnection guides most of the field energy to propagate from the pin to the microstrip. In the baseplate hole, the TEM wave pattern is dominating and higher order modes are not obvious, both at 10 and at 26 GHz.



(a)

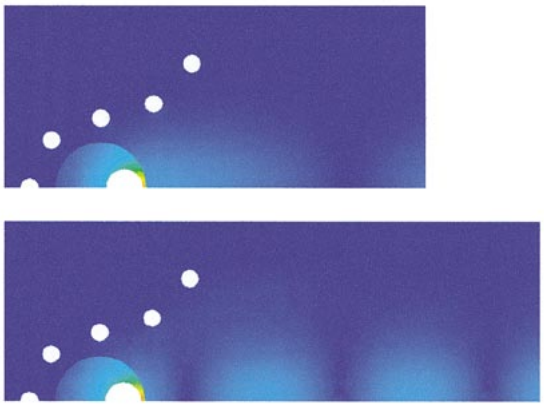


(b)

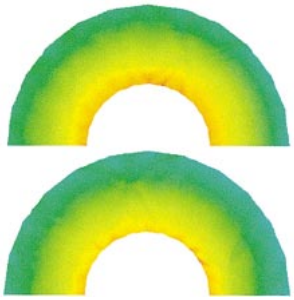
Fig. 11. Measured and modeled performance of the second-generation MIPPS interconnection. (a) Return loss and (b) insertion loss.

B. Optimization of the Performance to 26.5 GHz Using a Comprehensive Analysis Method

The 3-D EM tool provides S-parameters for the package. It is also used to serve as a platform to optimize the microwave passive structures using the traditional computer-aided optimization (CAO) methods [6]. The tool provides vivid presentation of electrical and magnetic field distribution as well as current flow at any particular frequency point, which gives insight to the physical mechanism of the package. However, it does not give a straightforward hint as to which area should be optimized. The traditional CAO procedure thus requires many iterations of "trial-and-error" cycles to identify where to optimize. Usually it can take a long time and occupies a lot of computer resources. In this paper, we propose a comprehensive analysis method that combines the traditional CAO method and time-domain analysis. We use it to optimize the second-generation interconnection successfully. TDR data provide a direct link between the electrical behavior and the physical position in the signal transmission path. It discloses the impedance and parasitic inductance or capacitance at any point along the signal transmission path. Thus it is easy to identify the area such as those with big impedance mismatch and parasitic inductance or capacitance, which usually have the most significant affect on performance. In the comprehensive optimization method, the package is first



(a)



(b)

Fig. 12. Full-wave analysis of the second-generation MIPPS interconnection shows that the E-field energy is propagating along the signal path properly and there is no obvious disturbance to the field. (a) E-field distribution across the view plane 1. (top) $f = 10$ GHz and (bottom) $f = 26$ GHz. (b) E-field distribution across the view plane 2. (top) $f = 10$ GHz and (bottom) $f = 26$ GHz.

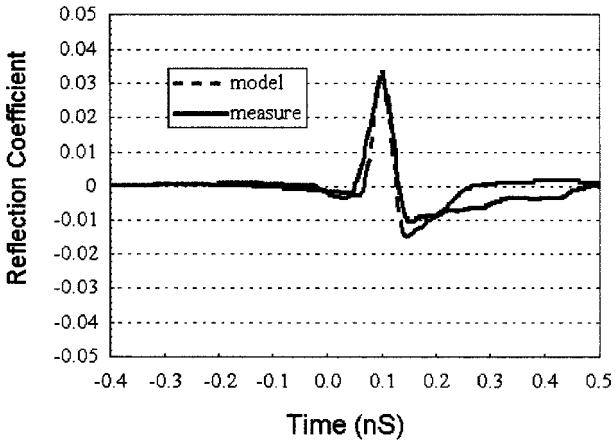
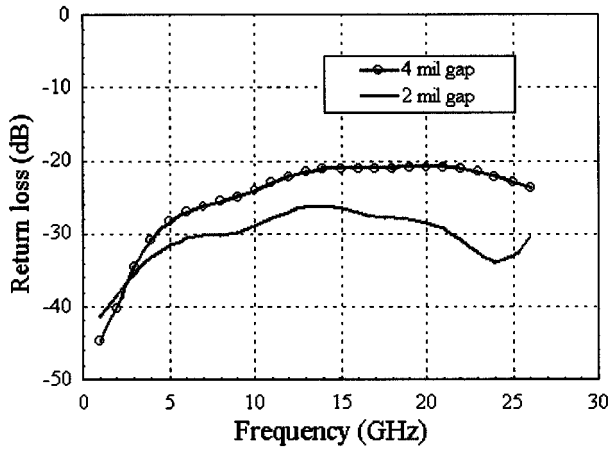
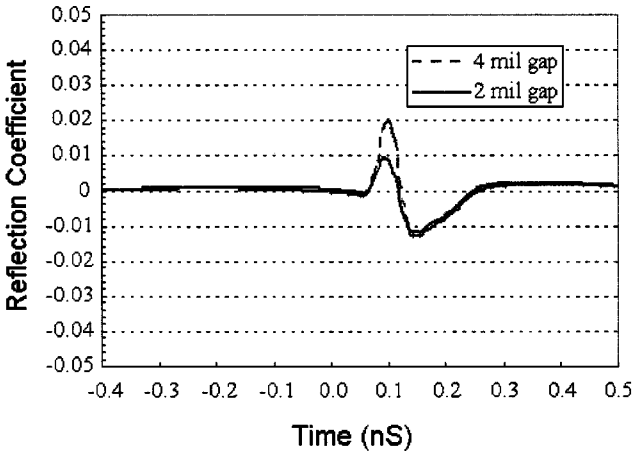


Fig. 13. TDR responses from measurement and model of the second-generation interconnection match very well. The TDR response provides a clear image that the dominant parasitic in the interconnection is inductive.

simulated using the 3-D EM tool, and the S-parameters are converted to TDR data using Agilent's Advanced Design System. After the most sensitive region is determined from the time-domain data, the full-wave EM behaviors are observed to understand the physical basis behind the electrical performance, and modification to or redesign of that region can be made according to the observations. The EM tool is then applied to simulate new



(a)



(b)

Fig. 14. Optimization result shows that the interconnection can achieve a better than 25-dB return loss over dc to 26.5 GHz, and it is possible to extend a good performance to 30 GHz. (a) Performance dependence on the distance between the pin and the edge of the hole in the alumina substrate. (b) TDR response shows that the inductance of the ribbon bond is suppressed more when the pin is moved closer to the edge of the hole. This is because the parasitic capacitance is bigger when they are closer, which compensates the parasitic inductance.

package designs. The iteration of EM simulation, time-domain analysis, and refinement of the structure may need to go on several times before the electrical performance specification is met. The optimized geometry is recorded and used to build test structures. The comprehensive optimization method avoids the long "guess" period spent for recognizing the most important parts and geometrical parameters in the structure, which is necessary when optimizing a complex 3-D structure using the traditional CAO method.

C. Results and Discussion

The TDR measurement of the second-generation interconnection unveils an inductive region in the signal transmission path, as shown in Fig. 13, which is due to the ribbon bond interconnection. Optimization of the interconnection can be done in either of two ways: reducing the parasitic inductance of the ribbon bond or providing a compensating capacitance.To reduce the parasitic inductance, the ribbon bond can be made shorter, down to the bonding process limitation of 20 mil. A 3-D model with this bond length still exhibits great inductance. To compensate it by adding parasitic capacitance, the source of compensating capacitance can be found from full-wave analysis. From Fig. 12(b), the E-field energy is highly concentrated near the shortest gap between the pin and the hole edge, which demonstrates a possible capacitive region. By moving the pin closer to the hole edge, the capacitance is increased. EM simulation shows that when the shortest gap distance is as small as 4 mil, the inductive peak in TDR response is greatly suppressed and the return loss is better than 20 dB up to 26.5 GHz. As the gap distance decreases further to 2 mil, the parasitic capacitance will be large enough to completely compensate the inductance of the bond wire. The return loss is improved to be better than 25 dB from dc to 26.5 GHz, as shown in Fig. 14.

Fig. 14 shows that it is possible to achieve 20-dB return loss up to 30 GHz. After the test structure is built, more optimization will be performed.

V. Conclusion

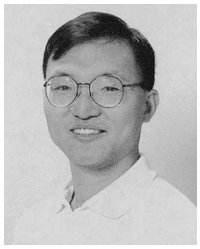
We have presented a novel 26.5-GHz PGA package design for microcircuits and microwave subsystems packaging. Compared with the traditional deep cavity metal packaging technologies, this packaging solution can reduce costs by more than 50% and yet maintain the high performance required at RF and microwave frequencies. Experimental and simulation results for the RF package interconnects have shown a return loss better than 20 dB to 20 GHz. Additional optimization of the transition has successfully extended the performance to 26.5 GHz. This is the first time that the PGA technology is successfully applied to K-band microwave packaging.

Acknowledgment

The authors would like to thank M. Guth for the assembly of the prototype MIPPS modules and D. Nicholson for his insights into the optimization and design of the MIPPS transition.

References

[1] T. A. Midford, J. J. Wooldridge, and R. L. Sturdivant, "The evolution of packages for monolithic microwave and millimeter-mave circuits," *IEEE Trans. Antennas Propagat.*, vol. 43, pp. 983–991, Sept. 1995.
[2] L. R. Dove, M. L. Guth, and D. B. Nicholson, "A low-cost RF multichip module packaging family," *Hewlett-Packard J.*, pp. 53–60, Aug. 1998.
[3] M. Pecht, *Handbook of Electronic Package Design*. New York: Marcel Dekker, 1991.
[4] J. Williams and E. Godshalk, "Characterization and modeling of pin grid array (PGA) packages," in *Proc. ISHM'92* , pp. 623–628.
[5] T. W. Goodman, H. Fujita, Y. Murakami, and A. T. Murphy, "High speed electrical characterization and simulation of a pin grid array package," *IEEE Trans. Comp., Packag., Manufact. Technol.*, vol. 18, pp. 163–167, Feb. 1995.
[6] "HP 85 180 high-frequency structure simulator,", version 5.4, 1999.

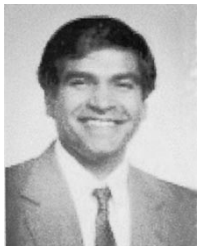


Hongwei Liang (S'97) was born in Jiangsu Province, China, in 1973. He received the B.S. degree in electrical and electronic engineering from Nanjing University, Nanjing, China, in 1993 and the M.S. degree in industrial automation from the Institute of Automation, Chinese Academy of Sciences, Beijing, China, in 1996. Since 1997, he has been pursuing the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

He was a Graduate Assistant with the Chinese Academy of Sciences. He is now a Graduate Research Assistant at Georgia Tech, where he has participated in several projects within the NSF Packaging Research Center. His research interests include development and characterization of microwave and millimeter-wave packaging and interconnects.

Heidi Langeberg Barnes received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1986.

From 1987 to 1997, she was with NASA's Stennis Space Center supporting instrumentation for rocket engine ground testing. Since 1997, she has been with Agilent Technologies' (formerly Hewlett-Packard) Microwave Technology Center, Santa Rosa, CA. Her areas of interest include modeling and design of high-frequency interconnect transitions for microwave packages and printed wiring board applications.



Joy Laskar (S'84–M'85) received the B.S. degree in computer engineering (highest honors) from Clemson University, Clemson, SC, in 1985.

Prior to joining Georgia Institute of Technology, Pasadena, in 1995, he held faculty positions at the University of Illinois and the University of Hawaii. At Georgia Tech, he is currently the Chair for the Electronic Design and Applications technical interest group, the Yamacraw Research Leader for Broadband Access Hardware, and the Packaging Research Center Thrust Leader for RF and wireless. His research has focused on high-frequency IC design and integration. At Georgia Tech, he heads a research group of 20 members with a focus on integration of high-frequency electronics with optoelectronics and integration of mixed technologies for next-generation wireless and optoelectronic systems. His research is supported by more than 15 companies and numerous federal agencies, including DARPA, NASA, and NSF. He is a Coorganizer and Chair for the Advanced Heterostructure Workshop. He is a Member of the North American Manufacturing Initiative Roadmapping Committee. He has published more than 100 papers, given numerous invited talks, and has eight patents pending. He is a Cofounder and Director of a RF Solutions, a broadband wireless company.

Dr. Laskar is a member of the IEEE Microwave Theory and Techniques Symposia Technical Program Committee. He received the 1995 Army Research Office Young Investigator Award, the 1996 National Science Foundation CAREER Award, the 1997 NSF Packaging Research Center Faculty of the Year Award, the 1998 NSF Packaging Research Center Educator of the Year Award, the 1999 IEEE Rappaport Award (best IEEE Electron Devices Society journal paper), and the 2000 IEEE MTT IMS Best Paper Award.

Don Estreich (M'79) received the B.S.E.E. degree at the University of California, Berkeley, in 1967 and the M.S.E.E. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1974 and 1980, respectively.

His doctoral dissertation was on the physics, modeling, and prevention of latchup in CMOS integrated circuits. He has been involved in the design, packaging, and application of GaAs integrated circuits and subsystems for nearly 20 years at Hewlett-Packard Company and now at Agilent Technologies, Santa Rosa, CA. He presently manages the Advanced Packaging and Interconnect R&D group within the Microwave Technology Center. He has been a Teaching Fellow at Stanford University, where in 1983 he developed a class on the design of analog GaAs integrated circuits. He has taught numerous short courses on GaAs IC technology, including most recently the yearly GaAs IC Primer Class at the GaAs IC Symposium. He is presently Chairman of the Industrial Advisory Committee at the NSF-sponsored Packaging Research Center located at the Georgia Institute of Technology, Atlanta.

Dr. Estreich has participated on a number of organizing committees of IEEE conferences.