Novel DC-Offset Cancellation Techniques for Even-Harmonic Direct Conversion Receivers

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***Abstract*—We present two novel dc-offset cancellation techniques for antiparallel diode pair even-harmonic mixers in a direct conversion receiver. Using fundamental equations, we describe the contribution of diode mismatch to dc offset and present an intrinsic mechanism of dc-offset cancellation. Similarly, we describe an extrinsic method of cancellation utilizing the second harmonic of the local oscillator. The cancellation techniques are successfully incorporated in fully monolithic C-band direct conversion receivers and mixers. Measurements confirm the equations and verify complete cancellation using the proposed methods. This works provides a solid foundation for the design and development of fully monolithic and high-performance direct conversion receivers.**

***Index Terms*—Demodulation, frequency conversion, homodyne detection, MESFET circuits, microwave circuits, microwave frequency conversion, microwave mixers, microwave receivers, mixers, MMIC mixers, MMIC receivers, monolithic microwave integrated circuits (MMICs), radio receivers, receivers.**

I. Introduction

DIRECT conversion receivers have attracted a great deal of attention over the past few years. By eliminating the intermediate-frequency stages and the image-reject requirement of the front-end filters, direct conversion can significantly improve on-chip integration of the receiver. However, use of this topology creates additional performance criteria such as second-order intermodulations (IM2), dc offsets, and in-band local oscillator (LO) radiation that are not present when using a heterodyne counterpart. As a result, physical implementations of direct conversion receivers have repeatedly proven to be a compromise between performance and the level of on-chip integration [1]–[6]. One of the most challenging of these performance criteria has been the effective cancellation of dc offsets without the use of off-chip components, such as compensation circuitry or large blocking capacitors [1], [2].

In direct conversion receivers, the mixer is immediately followed by a chain of high-gain direct coupled amplifiers that can amplify small levels of dc offset and saturate the proceeding stages. Consequently, sensitivity of the receiver can be directly limited by the dc-offset component of the mixer output.

The dc offset of a mixer can be separated into two components: a constant and a time-varying offset. The constant dc offset can be attributed to the mismatch between the mixer components while the time-varying dc offset is generated by the self-mixing of the LO. As demonstrated in Fig. 1, the in-band LO signal can penetrate the radio-frequency (RF) front end by leakage or radiation and result in generation of a dc-offset voltage by self-mixing in the down-convert mixer. The level of this dc offset, which is dependent on the time-varying load of the antenna, can also vary with time. By choosing an even-order subharmonic mixer topology, an out-of-band LO can be used in place of the in-band counterpart to alleviate LO radiation and, consequently, reduce the time-varying component of the dc offset. Even-harmonic (EH) mixing using an antiparallel diode pair (APDP) has been introduced in previous works as a good candidate for such mixer topology [2], [5]–[7].

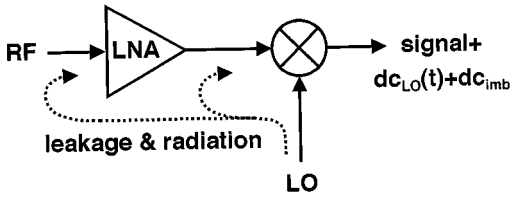

Fig. 1. Constant and time-varying dc offset in direct conversion receivers.

In this paper, we study the dc-offset generation mechanisms in the APDP structure as the fundamental building block of an EH mixer. Using an analytical approach, we describe the effects of mismatch on the dc offset and present an intrinsic mechanism that utilizes this mismatch for dc-offset cancellation. In addition, we present an extrinsic cancellation method using the second harmonic of the LO, which can provide better control and reproducibility than the intrinsic technique. Both techniques are successfully incorporated in a C-band direct conversion receiver and an EH mixer monolithic microwave integrated circuit (MMIC). Experimental results verify the fundamental formulas and the cancellation techniques.

II. Analysis

To fully understand the mechanisms of mixing and dc-offset generation in an APDP structure, we analyze the unbalance effect created by mismatch between the *I–V* characteristics of the diodes. Although monolithic processes can generally reduce mismatch between adjacent diodes so that it can be ignored for most performance criteria, effects of the mismatch on the dc offset remain significant.

In order to analyze the contribution of the APDP mismatch to dc offset, we derive the fundamental equations of a mismatched APDP shown in Fig. 2. We can describe the instantaneous current through the diodes by

$$i_1 = -i_s(e^{-\alpha V} - 1) \tag{1}$$

$$i_2 = i_s(e^{\alpha V} - 1) \tag{2}$$

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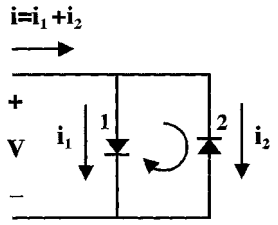

Fig. 2. Schematic of the antiparallel diode pair.

where α and i_s are the slope ($\alpha = q/kT$) and saturation current of the diodes, respectively. The instantaneous conductance of the diode pair can be described by differentiating each current term

$$g_{1,2} = \frac{di}{dV} = \alpha i_s e^{\pm \alpha V} \tag{3}$$

and adding the resulting conductance expressions

$$g = g_1 + g_2 = \alpha i_s (e^{\alpha V} + e^{-\alpha V}) = 2\alpha i_s \cosh(\alpha V). \tag{4}$$

In order to accurately account for diode imbalance, we need to consider the difference in both the slopes and saturation currents [8]. We define the modified slopes and saturation currents as

$$i_{s1} = i_s + \Delta i_s \quad \text{and} \quad i_{s2} = i_s - \Delta i_s \tag{5}$$

$$\alpha_1 = \alpha + \Delta\alpha \quad \text{and} \quad \alpha_2 = \alpha - \Delta\alpha. \tag{6}$$

Then we rewrite the instantaneous conductance expressions for each case

$$g_{\Delta i_s} = 2\alpha i_s \left[\cosh(\alpha V) + \frac{\Delta i_s}{i_s}\sinh(\alpha V)\right] \tag{7}$$

$$g_{\Delta\alpha} = 2\alpha i_s e^{(\Delta\alpha)V}\left[\cosh(\alpha V) + \frac{\Delta\alpha}{\alpha}\sinh(\alpha V)\right]. \tag{8}$$

Two modified expressions can be written to describe the change in conductance due to mismatch in each variable

$$\begin{aligned} g_{\Delta i_s} \approx\ & 2\alpha i_s[I_0(\alpha V_{\rm LO}) + 2I_2(\alpha V_{\rm LO})\cos(2w_{\rm LO}t) \\ & + 2I_4(\alpha V_{\rm LO})\cos(4w_{\rm LO}t) + \cdots] \\ & + 2\alpha(\Delta i_s)[2I_1(\alpha V_{\rm LO})\cos(w_{\rm LO}t) \\ & + 2I_3(\alpha V_{\rm LO})\cos(3w_{\rm LO}t) + \cdots] \end{aligned} \tag{9}$$

$$\begin{aligned} g_{\Delta\alpha} \approx\ & 2\alpha i_s[I_0(\Delta\alpha V_{\rm LO}) + I_1(\Delta\alpha V_{\rm LO})\cos(w_{\rm LO}t) \\ & + I_2(\Delta\alpha V_{\rm LO})\cos(2w_{\rm LO}t) + \cdots] \\ & \times \{[I_0(\alpha V_{\rm LO}) + 2I_2(\alpha V_{\rm LO})\cos(2w_{\rm LO}t) + \cdots] \\ & + (\Delta\alpha/\alpha)[2I_1(\alpha V_{\rm LO})\cos(w_{\rm LO}t) + \cdots]\} \end{aligned} \tag{10}$$

where $I_n(x)$ are nth-order modified Bessel functions. To simplify the analysis, we now collect all the significant conductance terms that result in a dc component and write

$$g_{\Delta i_s,\rm dc-offset} \approx 2\alpha(\Delta i_s) I_1(\alpha V_{\rm LO})\cos(w_{\rm LO}t) \tag{11}$$

$$\begin{aligned} g_{\Delta\alpha,\rm dc-offset} \approx\ & 2\alpha i_s \cos(w_{\rm LO}t) I_1(\Delta\alpha V_{\rm LO}) \\ & \times [I_0(\alpha V_{\rm LO}) + I_2(\alpha V_{\rm LO})]. \end{aligned} \tag{12}$$

Current characteristics of the APDP can then be found by multiplying the conductance expressions by the applied voltage $V = V_{\rm LO}\cos(w_{\rm LO}t) + V_{\rm RF}\cos(w_{\rm RF}t)$ and summing the two currents

$$\begin{aligned} i_{\rm dc-offset} \approx\ & \pm 2\alpha(\Delta i_s) V_{\rm LO} I_1(\alpha V_{\rm LO}) \\ & + 2\alpha i_s V_{\rm LO} I_1(\Delta\alpha V_{\rm LO}) \\ & \times [I_0(\alpha V_{\rm LO}) + I_2(\alpha V_{\rm LO})]. \end{aligned} \tag{13}$$

Current terms add constructively when one of the diodes has both a higher slope and a higher saturation current; they add destructively otherwise. A careful look at the initial diode equations of (1) and (2) shows that the existence of the former condition is unlikely. Higher saturation current and higher slope will result in considerable difference in the *I–V* characteristics of the diodes in the APDP, a condition that is not common in most monolithic processes. A more likely scenario is the latter when one of the diodes has a higher slope and a lower saturation current. In this case, both negative and positive dc offsets can be generated depending on the parameters in (13). More importantly, under special conditions, it is possible for the two terms to cancel each other and produce a net dc offset of zero. Consequently, this mechanism can not only eliminate dc offset generated by mismatch but also cancel any dc offset generated by other sources such as LO self-mixing. As shown in (13), the intrinsic dc-offset cancellation mechanism is directly related to the LO voltage applied across the APDP. Therefore, adjusting the LO power can vary the level of dc offset generated by the mismatch to produce a net dc offset of zero, a condition that we will refer to as a dc-offset null. While operating at this null point, all concerns regarding saturation of the direct coupled baseband amplifiers are eliminated, and any unexpected formation of dc offset can be compensated by minor tuning of the LO power. Problems can arise when the dc-offset nulls only occur for the LO powers that are either too low and result in poor conversion characteristics or too high and exceed the diode current limitations.

In order to eliminate the dc offsets with greater control and reproducibility, we propose an extrinsic cancellation method that uses a canceling dc component generated by down-converting an additional tone at the second harmonic of the LO, $V_{\rm 2LO}\cos(w_{\rm 2LO}t + \phi)$. The dc current generated from the addition of this tone can be described by multiplying the conductance expressions in (9) and (10) with the applied voltage and collecting the significant terms that arise from mixing the LO signal and the second harmonic

$$\begin{aligned} i_{\rm dc-cancel} \approx\ & V_{\rm LO} V_{\rm 2LO}\cos(\phi)\alpha i_s \\ & \times [I_2(\alpha V_{\rm LO}) + I_2(\Delta\alpha V_{\rm LO}) I_2(\alpha V_{\rm LO}) + \cdots]. \end{aligned} \tag{14}$$

Equation (14) shows that modifying the phase and amplitude of the second harmonic varies the amplitude and sign of this canceling dc component; therefore, it can be controlled to produce a net dc offset of zero by matching the amplitude and countering the sign of the preexisting dc offset.

Since the RF properties of on-chip active components can be controlled with relative ease and accuracy, this indirect RF tuning of the dc output can be performed with greater precision

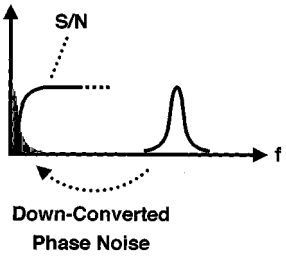

Fig. 3. Additive flicker noise effect in extrinsic dc-offset cancellation technique.

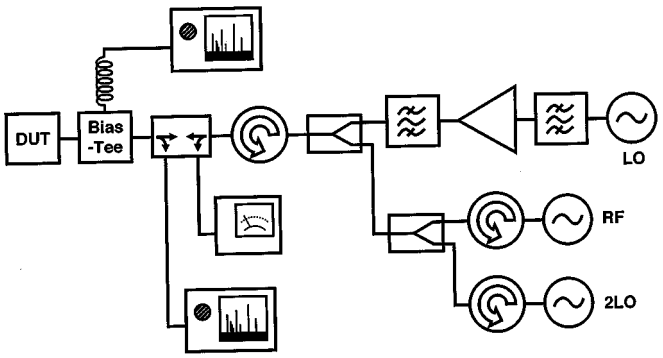

Fig. 4. Measurement setup used for the verification of APDP dc-offset generation and cancellation mechanisms.

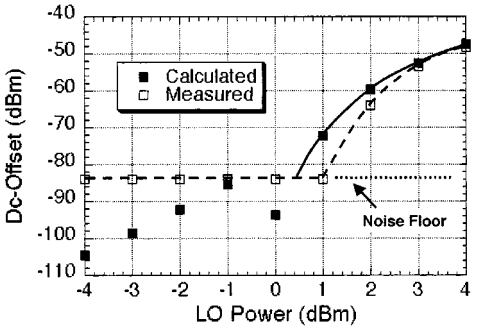

Fig. 5. Measured and calculated dc offset of a monolithic GaAs APDP at LO frequency of 2 GHz.

than low-frequency analog tuning. For example, a simple varactor can be used to vary the phase and amplitude of the second harmonic and consequently result in small changes in the corresponding dc component. In such a scenario, large shifts in the junction voltage of a varactor can translate into minute changes in the dc offset.

To fully explore the practicality of this cancellation technique, we also consider the noise contribution of the second harmonic tone to the mixer noise floor and flicker noise. As shown in Fig. 3, the phase noise associated with the second harmonic tone is down-converted to baseband in the mixing process. This addition of phase noise can be modeled by additive flicker noise at the output of the mixer, where the corner frequency and the shape of this flicker noise is determined by the skirt of the second harmonic tone. The signal-to-noise ratio (S/N) of signals below this corner frequency is degraded by the addition of the down-converted phase noise. Assuming a practical on-chip oscillator phase noise of -100 dBC/Hz at 100 kHz offset from the carrier, corner frequencies below 100 kHz can be achieved. This number can improve dramatically when using a phase-locked loop (PLL) synthesized source, which is common for most wireless applications.

III. Experimental Results

In order to verify the fundamental equations, we characterized a monolithic GaAs MESFET APDP fabricated in a commercial TriQuint process. The diodes were first measured and modeled so that the proper variables can be extracted for use in the formulas. Multiple values for the slope and saturation current of each diode were extracted for small ranges of the junction voltage and used to accurately model the current in each bias range. For voltages above the turn-on voltage, the diode behavior was found to be dominated by the series resistance and can no longer be described accurately by the ideal diode equation. Therefore, in this case, the validity of the formulas is limited to the "low" LO power levels of below 4 dBm. The diode parameters corresponding to "low" LO voltages were extracted and substituted in (13) to calculate the dc offset generated by the mismatch. The diodes were then measured using on-wafer probes in the measurement setup shown in Fig. 4. Extensive filtering was used in the setup to ensure sufficient rejection of the harmonics of the LO synthesizer, which can result in extraneous dc components. The LO signal is applied to the APDP test structure, while the baseband output is monitored through a bias-tee.

Fig. 5 shows the agreement between the calculated and measured values for dc offset at LO power levels varying from -4 to $+4$ dBm. The measurements verified the validity of the fundamental formulas in predicting the dc offset generated under "low" LO conditions. Small inconsistencies between the calculated and measured values are attributed to the effect of the variance in load impedance, which was not considered in the formulas.

This measurement is repeated for various APDP test structures of different peripheries to examine the feasibility of the intrinsic dc-offset cancellation described earlier. The LO power was varied over a wider range of powers reaching as high as 16 dBm. As shown in Fig. 6, measurements of fabricated APDP test structures demonstrated dc-offset cancellation by the intrinsic mechanism. The measurements confirmed cancellation within the LO power range that produces optimum conversion characteristics in terms of loss and intermodulations. Although these results verified the intrinsic mechanism of dc-offset cancellation, further study is needed to investigate the repeatability of this technique.

An experiment was also performed to verify the proposed extrinsic dc-offset cancellation technique. As shown in Fig. 4, two synthesized sources are used to generate the LO and second harmonic of the LO frequency. The signals are combined and applied across the APDP while the baseband output is monitored through a bias-tee. With the phase kept at a constant offset, the amplitude of the second harmonic is varied by the source until dc-offset cancellation is observed. Fig. 7 shows the dc output of the APDP as a function of second harmonic power. In a

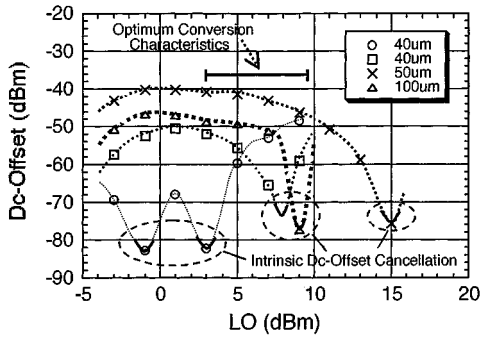

Fig. 6. DC offset of different periphery APDP test structures showing dc-offset nulls created by the intrinsic mechanism of dc-offset cancellation.

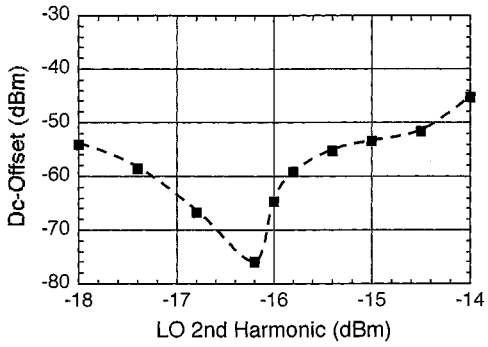

Fig. 7. DC offset of an APDP as a function of the power of the second harmonic showing dc-offset cancellation by the extrinsic method.

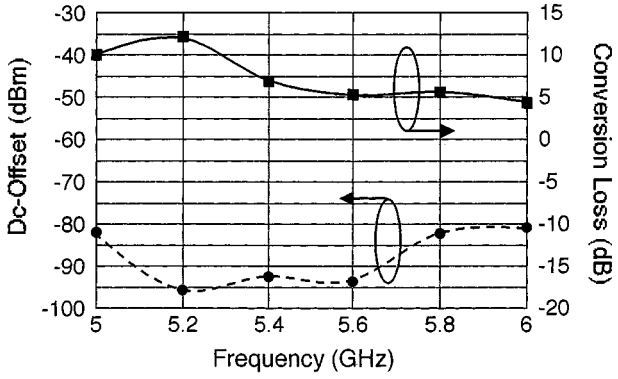

Fig. 8. DC offset and conversion loss of the EH mixer.

three-port test setup similar to that of Fig. 4, the experiment was repeated with a C-band EH direct conversion mixer that incorporated the same APDP structure. The balanced mixer consists of active baluns at the RF input and two sets of APDP mixers that utilize resonant tanks to reduce dc offsets generated by LO leakage [7]. Measurement results verify effective dc offset while maintaining a second-order input intercept point (IIP2) of $+16$ dBm and an average conversion loss of 10 dB for input RF frequencies of 5 to 6 GHz. Fig. 8 shows the conversion loss and dc-offset performance of this mixer. A die photograph of an APDP test structure and the EH mixer is shown in Fig. 9.

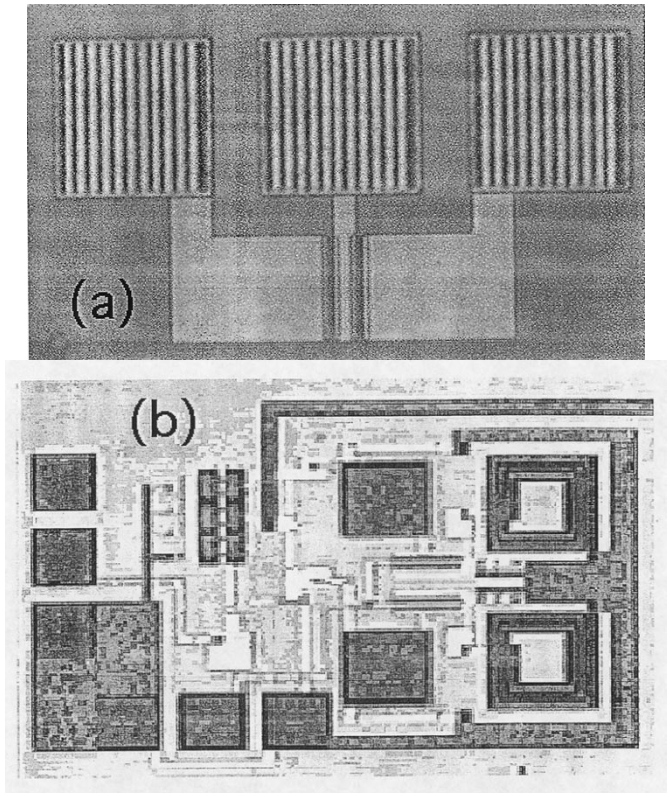

Fig. 9. Die photograph of (a) an APDP test structure and (b) the EH mixer MMIC.

IV. Direct Conversion Receiver

The receiver is designed for high-data-rate C-band wireless applications and fabricated in the TriQuint TQTRx GaAs MESFET process. It utilizes the EH mixer described earlier and the intrinsic cancellation mechanism to obtain high linearity and effective dc-offset cancellation.

A. Circuit Design

The receiver emulates a simple in-phase (I) and quadrature-phase (Q) demodulator topology with a subharmonic frequency conversion scheme. As illustrated in Fig. 10, the receiver consists of different circuit blocks such as dividers, phase shifters, and the EH mixers described earlier. Active implementations are utilized for the RF power divider and baluns to avoid the use of spiral inductors and reduce the die area. However, a passive Wilkinson approach is applied for the LO power divider to withstand high-power LO injection required to induce sufficient LO for intrinsic dc-offset cancellation. The RF power divider is power matched at the input and provides slight gain that helps to reduce the overall noise figure. Low-pass and high-pass filters (HPFs) are utilized as $\pm 45^{\circ}$ phase shifters on the RF path for quadrature phase differentiation, while a small resistor is used in series with the HPF to correct for amplitude imbalance. Active baluns are used to convert the single-ended RF signal into differential form before the balanced mixers [9].

Each mixer consists of two diode pairs that are pumped at the common node by an LO signal from the Wilkinson power divider. The diode pairs are terminated by two resonant tanks that are designed as short circuits at the LO and open circuits at

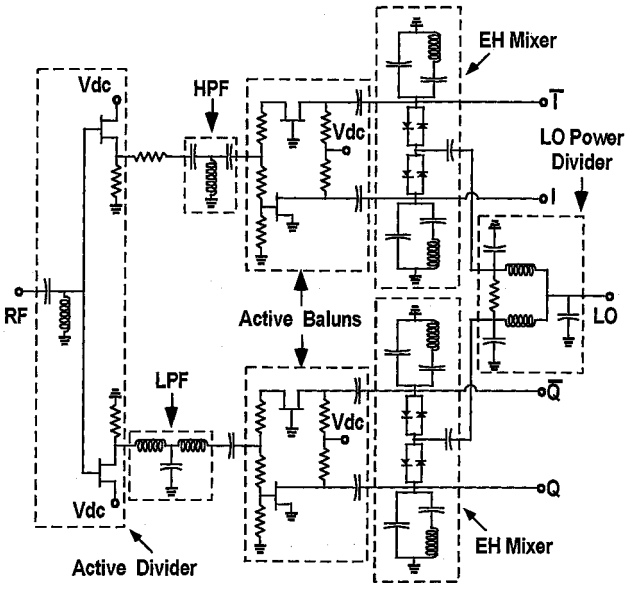

Fig. 10. Circuit schematic of the fully monolithic C-band direct conversion receiver.

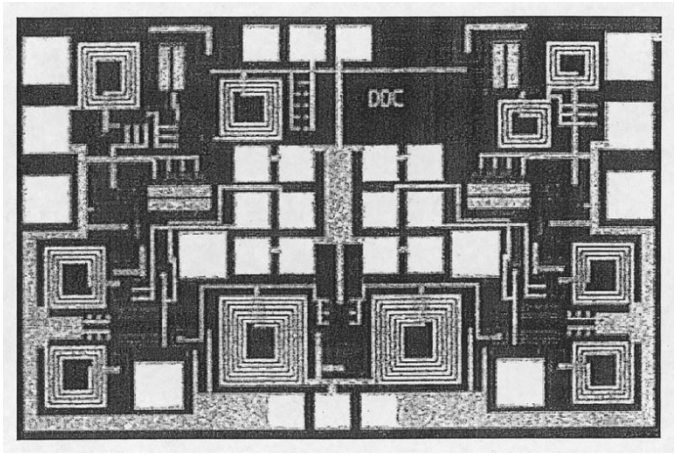

Fig. 11. Die photograph of the direct conversion receiver MMIC.

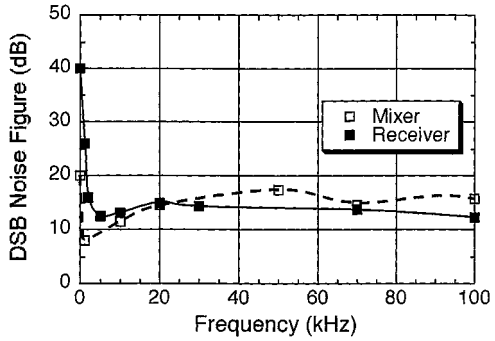

Fig. 12. Noise figure of the direct conversion EH mixer and receiver.

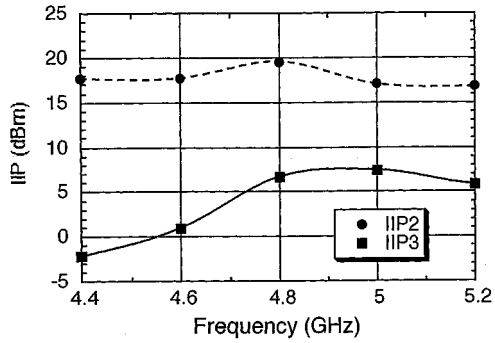

Fig. 13. Input intermodulation intercept points of the receiver.

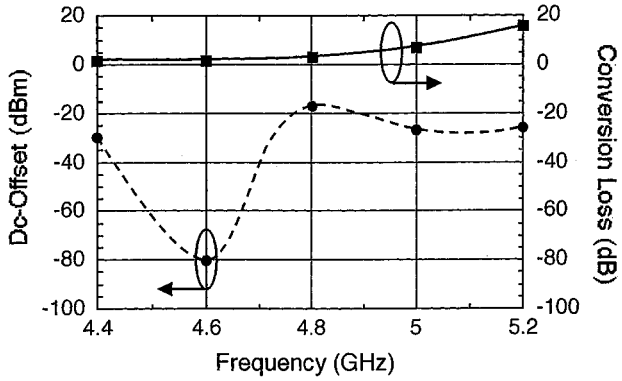

Fig. 14. DC offset and conversion loss of the receiver.

the RF frequencies. This configuration is utilized to improve the LO to RF isolation, to eliminate LO self-mixing, and to reduce the conversion loss by maximizing the LO voltage drop across the diode pairs. The mixers are designed for high output load impedance to maximize voltage conversion characteristics. A die photograph of the receiver MMIC is shown in Fig. 11.

B. Measurements

The receiver was powered by four 2.7-V sources supplying a total dc current of 21 mA. The receiver and the EH mixer were fully characterized for noise figure, conversion loss, linearity, and dc-offset performance from 4.4 to 5.2 GHz. A power sweep is first performed to find the dc-offset null point, LO power of 16 dBm, at which intrinsic dc-offset cancellation occurs. This LO power translates to approximately 8 dBm of LO power across the APDP pairs in each mixer. Noise figure measurements of the receiver and the EH mixer were performed using an HP3561A dynamic signal analyzer and plotted in Fig. 12. Two-tone and dc-offset measurements were also performed to examine linearity and verify intrinsic dc-offset cancellation as a function of frequency. Fig. 13 summarizes the two-tone measurement results in a plot of IIP2 and IIP3 as a function of the input RF frequency. Conversion loss and dc-offset performance of the receiver are plotted in Fig. 14 and show a narrow-band behavior induced by the frequency selectivity of the Wilkinson LO power divider. The loss and dc-offset performance of the receiver are optimized for the center frequency of the divider where sufficient LO power can be delivered to the mixers. A more robust divider interface between the mixers and the LO input port of the receiver will result in a broad-band conversion characteristics and dc-offset performance similar to that of the individual EH mixers.

V. Conclusion

We have presented two novel dc-offset cancellation techniques for even-harmonic direct conversion receivers. We derived the fundamental equations that describe the dc-offset generation due to mismatch in the antiparallel diode pair structure and presented an intrinsic mechanism of dc-offset cancellation. We also presented an extrinsic method of dc-offset cancellation using the second harmonic of the LO. An EH mixer and a fully monolithic direct conversion receiver, which incorporated the proposed cancellation techniques, were presented and characterized. Measurements showed good agreement with the predictions of the fundamental equations and verified complete dc-offset cancellation using the proposed techniques. This work provides a solid foundation for design and development of fully monolithic and high-performance direct conversion receivers.

Acknowledgment

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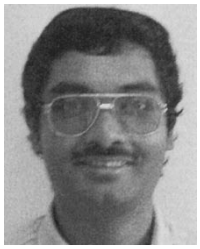

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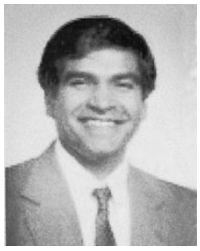

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