An L-Band High-Efficiency and Low-Distortion Power Amplifier Using HPF/LPF Combined Interstage Matching Circuit

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***Abstract*—An L-band high-efficiency and low-distortion power amplifier using a high-pass filter/low-pass filter (HPF/LPF) combined interstage matching circuit is presented in this paper. An HPF/LPF combined interstage matching circuit can realize both the optimum load impedance of the driver-stage FET and the optimum source impedance of the final-stage FET to achieve high efficiency with a specified distortion. The circuit has been utilized in a three-stage high-power-amplifier module, size of which is 0.08 cm^3 (7 mm $\times$ 7 mm $\times$ 1.7 mm). The amplifier achieves a power-added efficiency of 43.9% and an output power ($P_{\rm out}$) of 27.1 dBm with an adjacent channel leakage power of −38 dBc at 1.95 GHz for wide-band code-division multiple-access cellular phones.**

***Index Terms*—Distortion, high-pass filters, low-pass filters, microwave power amplifiers, MODFETs.**

I. Introduction

THE wide-band code-division multiple-access (CDMA) system is a leading candidate for the global third-generation mobile communication standard system. High efficiency, low distortion, and small size are required for power amplifiers used in wide-band CDMA cellular phones and several power amplifiers for wide-band CDMA cellular phones have been reported [1]–[3]. In providing high efficiency with a specified distortion, source impedance and load impedance of the final-stage FET must be optimized not only at the fundamental frequency [4], [5], but also at the harmonic frequency [6], [7]. It was indicated that the characteristics of the driver-stage FET have to be adjusted to compensate the distortion of the final-stage FET in achieving high efficiency with low distortion [8]–[10]. It was also suggested in [8]–[10] that the optimum interstage impedances at large-signal operation are different from those at small-signal operation. In such a case, we cannot realize both the optimum source impedance of the final-stage FET and the optimum load impedance of the driver-stage FET because the interstage matching circuit has to be comprised of lossless elements and the size of interstage matching circuit has to be small.

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In this paper, the high-pass filter/low-pass filter (HPF/LPF)-combined interstage matching circuit is presented. We calculate the load impedance of the driver-stage FET and the source impedance of the final-stage FET with six types of the interstage matching circuits comprised of single- or two-stage filters, such as the single-stage HPF, the single-stage LPF, the two-stage HPF, the two-stage LPF, the LPF/HPF combined, and the HPF/LPF combined interstage matching circuits. Next, a suitable interstage matching circuit providing both of the measured optimum interstage impedances for wide-band CDMA specifications is discussed. Finally, we propose the HPF/LPF combined interstage matching circuit, which leads to realizing both the optimum source impedance of the final-stage FET and the optimum load impedance of the driver-stage FET.

We apply the proposed HPF/LPF interstage matching circuit to a three-stage high-power amplifier (HPA) module for wide-band CDMA cellular phones in order to provide both optimum interstage impedances. The fundamental and second harmonic load impedances of the final-stage FET are also optimized by the output matching circuit. A multilayer ceramic substrate is used for reducing the size of the HPA module. The HPA module, size of which is 0.08 cm^3 (7 mm $\times$ 7 mm $\times$ 1.7 mm), provides a power-added efficiency (PAE) of 43.9% and an output power of 27.1 dBm with an adjacent channel leakage power (ACP) (5-MHz offset) of −38 dBc at 1.95 GHz.

II. Configuration of Interstage Matching Circuit

It is well known that the optimum load and source impedances of FETs at large-signal operation are different from those at small-signal operation. Besides, those optimum impedances depend on the target performance of amplifiers, e.g., high efficiency at a specified distortion, high efficiency at a specified power, and so on. In multistage power amplifiers, the final-stage FET operates in large signal condition. In addition, it is considered that the driver-stage FET operates near large-signal condition. Therefore, in addition to the optimum load impedances of the final-stage FET [8]–[10], we have to take into account the optimum interstage impedances, i.e. the optimum source impedance of the final-stage FET and the optimum load impedance of its driver-stage FET for achieving high efficiency with the specified distortion, Fig. 1 shows the configuration of power amplifiers. In this figure, $Z_{11\_\rm FET2}$, $Z_{\rm in2}$, $Z_{\rm in2\_opt}$ are referred to the input impedance, source

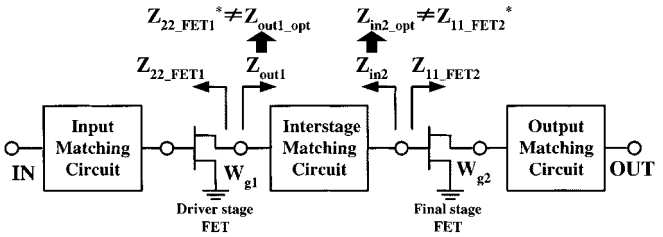

Fig. 1. Configuration of power amplifiers. Z_{22_FET1}: output impedance of the driver-stage FET. Z_{out1}: load impedance of the driver-stage FET. Z_{11_FET2}: input impedance of the final-stage FET. Z_{in2}: source impedance of the final-stage FET.

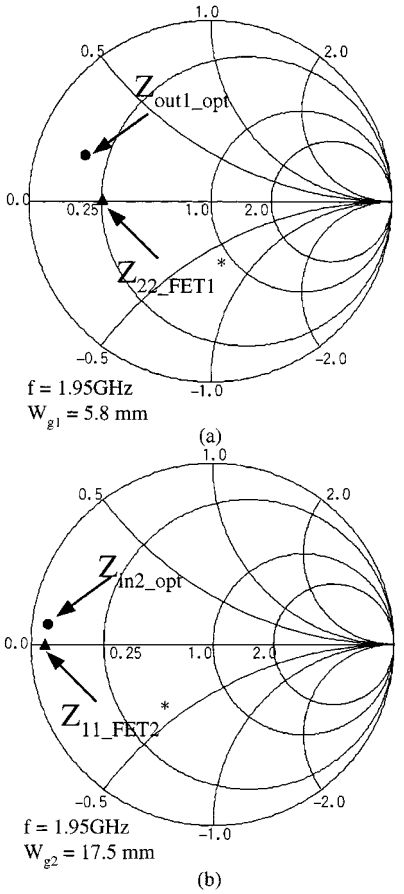

Fig. 2. Measured interstage impedances. (a) Conjugate of measured output impedance of the driver-stage FET ($Z^{*}_{22\_\mathrm{FET1}}$) and measured optimum load impedance of the driver-stage FET ($Z_{\mathrm{out1\_opt}}$). (b) Conjugate of measured input impedance of the final-stage FET ($Z^{*}_{11\_\mathrm{FET2}}$) and measured optimum source impedance of the final-stage FET ($Z_{\mathrm{in2\_opt}}$).

impedance, and optimum source impedance of the final-stage FET, respectively. Z_{22_FET1}, Z_{out1}, and $Z_{\mathrm{out1\_opt}}$ are defined as the output impedance, load impedance, and optimum load impedance of the driver-stage FET, respectively. Generally, the optimum impedances $Z_{\mathrm{in2\_opt}}$ and $Z_{\mathrm{out1\_opt}}$ are different from the conjugate impedances of Z_{11_FET2} and Z_{22_FET1} in large-signal operation. It is quite difficult to realize both optimum impedances at the two reference planes by using an lossless interstage matching circuit, particularly under the circuit scale limitation. Therefore, we have to investigate the optimum interstage inpedances and the suitable circuit

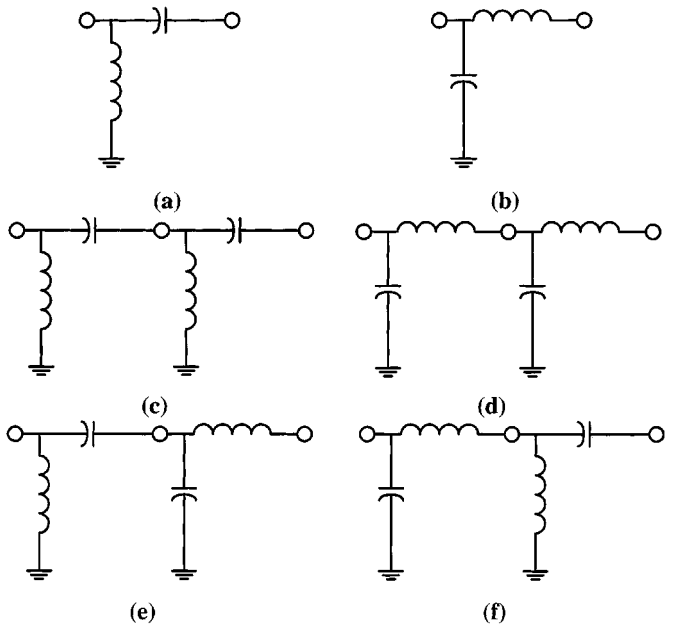

Fig. 3. Six circuit types of interstage matching circuits comprised of single- or two-stage filter circuits. (a) Single-stage HPF interstage matching circuit. (b) Single-stage LPF interstage matching circuit. (c) Two-stage HPF interstage matching circuit. (d) Two-stage LPF interstage matching circuit. (e) HPF/LPF combined interstage matching circuit. (f) LPF/HPF combined interstage matching circuit.

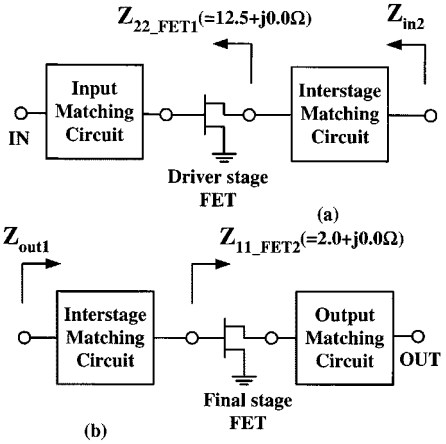

Fig. 4. Circuits used for calculation of the interstage impedances. (a) Circuits used for calculation of source impedance of the final-stage FET (Z_{in2}). (b) Circuits used for calculation of load impedance of the driver-stage FET (Z_{out1}).

configuration of the interstage matching circuit, which can realize almost optimum interstage impedances.

III. Optimum Interstage Impedances

In this section, we investigate the optimum interstage impedances in power amplifiers. First, we derive the optimum interstage impedances, i.e., the optimum source impedance of the final-stage FET ($Z_{\mathrm{in2\_opt}}$) and the optimum load impedance of the driver-stage FET ($Z_{\mathrm{out1\_opt}}$) for power amplifiers. Next, the derived impedances are optimized to achieve high efficiency at the specified ACP of -38 dBc for hybrid phase-shift keying (HPSK) modulated signal with the chip rate of 3.84 Mc/s for the wide-band CDMA cellular phones. Fig. 2

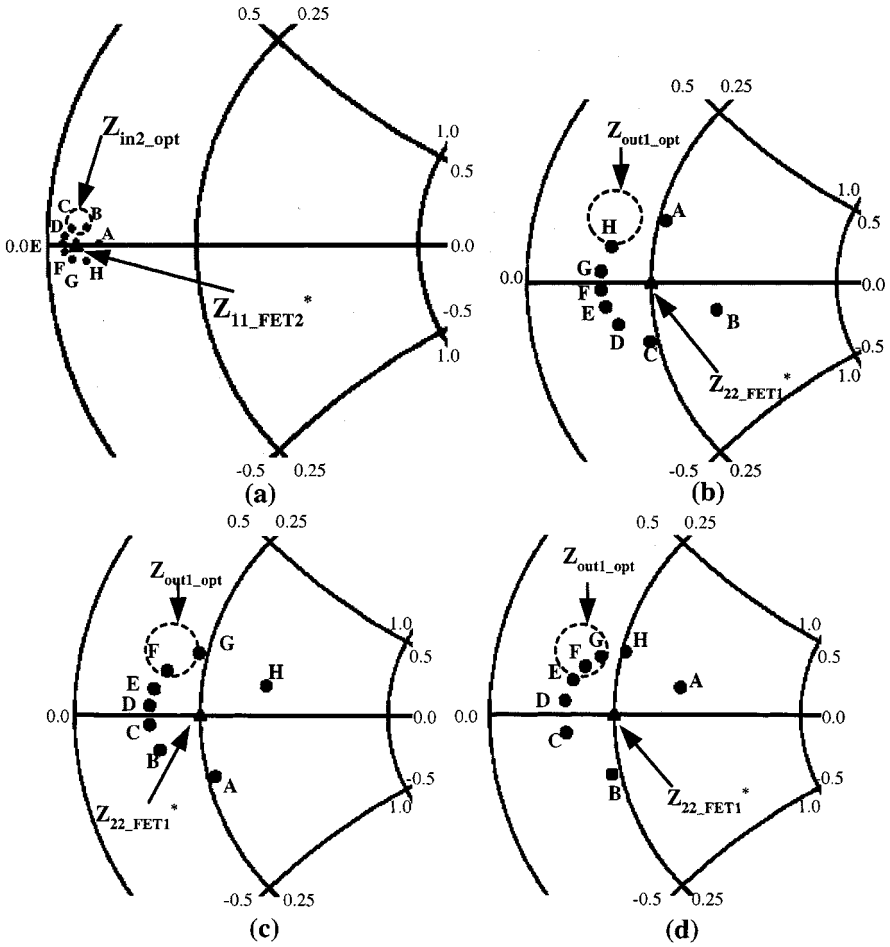

Fig. 5. Calculated interstage impedances for six types of interstage matching circuits comprised of single- or two-stage filter circuits (at $f = 1.95$ GHz, $Z^*_{22\_\mathrm{FET1}} = 12.5 + j\ 0.0\ \Omega$, and $Z^*_{11\_\mathrm{FET2}} = 2.0 + j\ 0.0\ \Omega$). (a) Calculated Z_{in2} for all types of interstage matching circuits. (b) Calculated Z_{out1} for the single-stage HPF interstage matching circuit. (c) Calculated Z_{out1} for the single-stage LPF interstage matching circuit. (d) Calculated Z_{out1} for the two-stage HPF interstage matching circuit.

shows the derived optimum interstage impedances $Z_{\mathrm{in2\_opt}}$ and $Z_{\mathrm{out1\_opt}}$. In Fig. 2, $Z^*_{11\_\mathrm{FET2}}$ and $Z^*_{22\_\mathrm{FET1}}$ are the conjugate of Z_{11_FET2} and Z_{22_FET1}, respectively. Gate peripheries of the driver- and final-stage GaAs pseudomorphic high electron-mobility transistors (pHEMTs) used are 5.8 and 17.5 mm, respectively. $Z_{\mathrm{in2\_opt}}$ and $Z_{\mathrm{out1\_opt}}$ were derived from the load–pull measurement results of the driver-stage FET and the source–pull measurement results of the final-stage FET taking into account the distortion compensation of the final-stage FET by the driver-stage FET. Z_{11_FET2} and Z_{22_FET1} were derived by the S-parameter measurement of the driver- and final-stage FET because it is quite difficult to measure the input and output impedances of the FETs at large-signal operation. It is demonstrated in Fig. 2 that both $Z_{\mathrm{in2\_opt}}$ and $Z_{\mathrm{out1\_opt}}$ are different from $Z^*_{11\_\mathrm{FET2}}$ and $Z^*_{22\_\mathrm{FET1}}$, respectively. The optimum interstage impedances move from $Z^*_{11\_\mathrm{FET2}}$ and $Z^*_{22\_\mathrm{FET1}}$ to $Z_{\mathrm{in2\_opt}}$ and $Z_{\mathrm{out1\_opt}}$ with the increase of input power of the FETs.

Therefore, we have to design the interstage matching circuit providing both of the optimum source impedance $Z_{\mathrm{in2\_opt}}$ at the input port of the final-stage FET and the optimum load impedance $Z_{\mathrm{out1\_opt}}$ at the output port of the driver-stage FET to achieve high efficiency with the specified ACP.

IV. Interstage Matching Circuit

As has been shown in the previous section, the optimum interstage impedances are different from conjugate of the output and input impedances of the FETs. In such a case, we cannot simultaneously realize the optimum source impedance of the final-stage FET and the optimum load impedance of the driver-stage FET because the interstage matching circuit has to be comprised of lossless elements and the size of the interstage matching circuit has to be small.

In this section, we discuss the suitable circuit type of the interstage matching circuit. We investigate six types of interstage matching circuits comprised of only single- or two-stage filter circuits because of the circuit scale restriction, such as the single-stage HPF, single-stage LPF, two-stage HPF, two-stage LPF, LPF/HPF combined, and HPF/LPF combined interstage matching circuits, as depicted in Fig. 3.

We calculate the source impedance of the final-stage FET and the load impedance of the driver-stage FET in the case of six types of the interstage matching circuits, respectively. The matching circuits are assumed to be lossless. The circuits used for calculation of interstage impedances are shown in Fig. 4. The source impedance Z_{in2} of the final-stage FET are calcu-

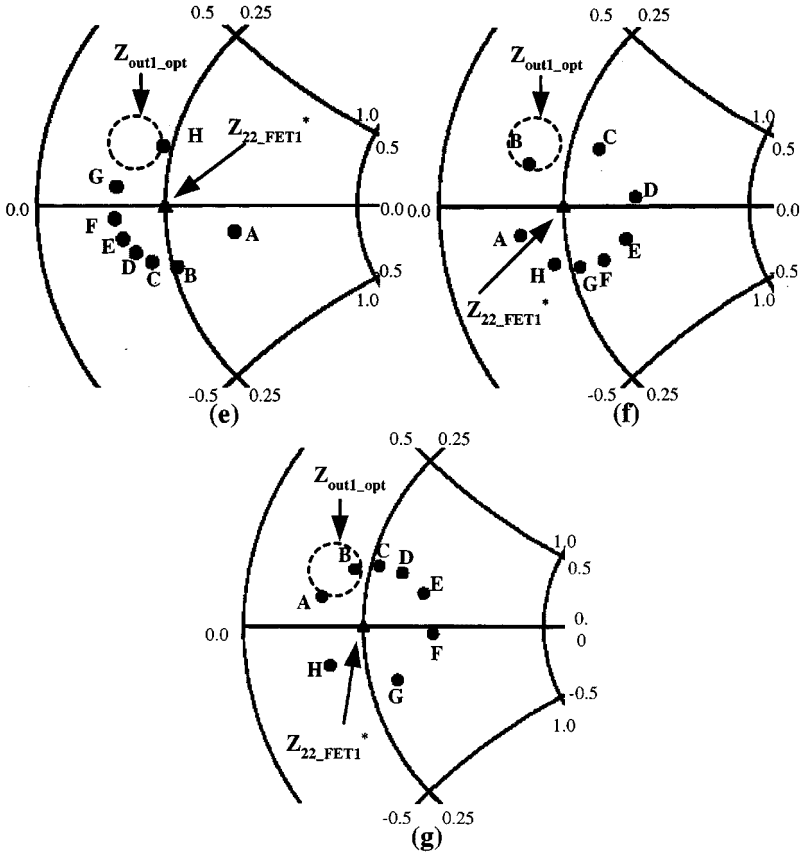

Fig. 5. *(Continued.)* Calculated interstage impedances for six types of interstage matching circuits comprised of single- or two-stage filter circuits (at $f = 1.95$ GHz, $Z^*_{22\_\mathrm{FET1}} = 12.5 + j\ 0.0\ \Omega$, and $Z^*_{11\_\mathrm{FET2}} = 2.0 + j\ 0.0\ \Omega$). (e) Calculated Z_{out1} for the two-stage LPF interstage matching circuit. (f) Calculated Z_{out1} for the HPF/LPF combined interstage matching circuit. (g) Calculated Z_{out1} for the LPF/HPF combined interstage matching circuit.

lated from Z_{22_FET1} and circuit parameters of the interstage matching circuit, as shown in Fig. 4(a). First, we derive the matching circuit parameters, which realize the impedances A to H for Z_{in2}, as shown in Fig. 5(a). The reflection coefficient between the impedances A to H and Z_{11_FET2} have a magnitude of 0.25 and phase of $m \times 45$ (deg) ($m = 0$ to 7: integer), respectively. Next, the load impedance Z_{out1} of the driver-stage FET is calculated from Z_{11_FET2} and the derived circuit parameters of the interstage matching circuit for each impedance A to H, as shown in Fig. 5(b). Calculation has been done in the case of $Z_{22\_\mathrm{FET1}} = 12.5 + j\ 0.0\ \Omega$ and $Z_{11\_\mathrm{FET2}} = 2.0 + j\ 0.0\ \Omega$ in accordance with the derived optimum interstage impedances in Fig. 2. When the interstage matching circuit is comprised of two-stage filter circuits, the impedance between the first- and second-stage filter circuits are assumed to be $5.0 + j\ 0.0\ \Omega$, which is equal to $\sqrt{Z_{22\_\mathrm{FET1}} \times Z_{11\_\mathrm{FET2}}}$. Z_{out1} and Z_{in2} are calculated for the interstage matching circuits comprised of the lumped elements.

Fig. 5(a)–(g) shows the calculated Z_{in2} and Z_{out1} on the Smith charts. Fig. 5(a) presents the calculated Z_{in2} for all types of the interstage matching circuits. Fig. 5(b)-(g) shows the calculated Z_{out1} for each type of the interstage matching circuit. The impedances A to H in Fig. 5(b)-(g) correspond to Z_{out1}, when Z_{in2} are matched to the impedances A to H in Fig. 5(a), respectively. It is clearly demonstrated in Fig. 5 that, if we use different type of interstage circuit, the load impedance Z_{out1} is matched to a different value while Z_{in2} is matched to the same impedance. The impedances A to H, phase of which are different from each other at the input port of the final-stage FET, are transformed to the impedances on the same impedance circles at the output port of the driver-stage FET by the six different types of interstage matching circuits, respectively. It means that we can optimize the phase of impedances at the same impedance circle by selecting the circuit configuration of the interstage matching circuit.

The optimum interstage impedances $Z_{\mathrm{out1\_opt}}$ and $Z_{\mathrm{in2\_opt}}$ for the wide-band CDMA specification are also depicted as the dotted circles in Fig. 5. In Fig. 5(a), the impedances B are located in $Z_{\mathrm{in2\_opt}}$. In Fig. 5(f) and (g), the impedances B are located in $Z_{\mathrm{out1\_opt}}$, while the impedances B are not located close to $Z_{\mathrm{out1\_opt}}$ in Fig. 5(b)-(e). Therefore, it is demonstrated that we can obtain almost optimum source impedance $Z_{\mathrm{in2\_opt}}$ of the final-stage FET and load impedance $Z_{\mathrm{out1\_opt}}$ of the driver-stage FET by employing the HPF/LPF or LPF/HPF combined interstage matching circuits. In the cases of the single-stage HPF, the single-stage LPF, two-stage HPF, and two-stage LPF interstage matching circuits, the impedance Z_{out1} is not close to $Z_{\mathrm{out1\_opt}}$ when the impedance Z_{in2} is matched to $Z_{\mathrm{in2\_opt}}$ so that we cannot realize both the optimum interstage impedances. Therefore, we propose the HPF/LPF or LPF/HPF combined interstage matching circuits in the power amplifiers for wide-band CDMA cellular phones.

In other words, it is important to point out that we have to select the suitable circuit type of the interstage matching circuit if

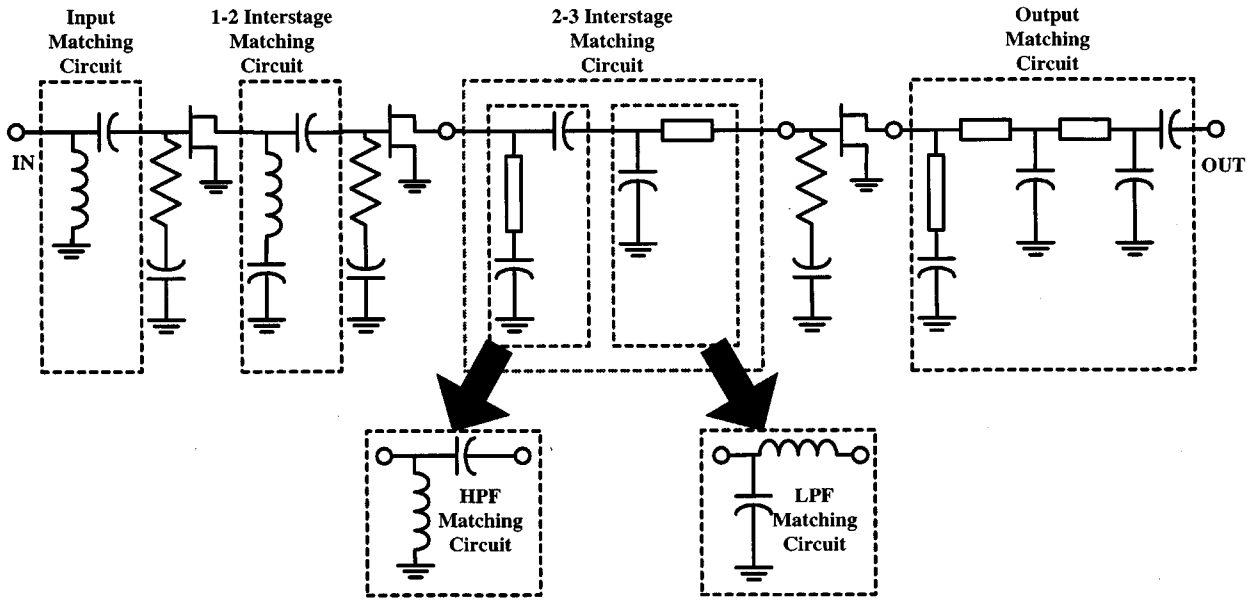

Fig. 6. Schematic diagram of the developed three-stage HPA module using HPF/LPF combined interstage matching circuit.

the optimum interstage impedances change in accordance with the specification of the power amplifiers or the characteristics of the employed devices.

V. Design of Three-Stage HPA Module

Fig. 6 shows a schematic diagram of the developed three-stage HPA module. GaAs pHEMT device has been used to realize high-efficiency and low-distortion characteristics. The gate peripheries of the first-, second-, and third-stage pHEMT are 1.5, 5, 8, and 17.5 mm, respectively. The proposed HPF/LPF combined interstage matching circuit is applied to the two to three interstage matching circuit to provide both optimum source impedance of the third-stage pHEMT and optimum load impedance of the second-stage pHEMT. In this HPA module, we do not use an LPF/HPF combined interstage matching circuit, but employ HPF/LPF combined interstage matching circuit. The circuit size can be reduced by using the bias short stab and dc block capacitor as the role of the parallel inductor and series capacitor, respectively, in the HPF/LPF combined interstage matching circuit. The output matching circuit is designed to achieve the optimum load impedance at both the fundamental and second harmonic frequencies. The optimum impedances are derived from load–pull and source–pull measurement for the third-stage pHEMT. The one to two interstage matching circuit is designed to provide small-signal matching impedances because the first-stage FET is considered to operate in small-signal condition.

VI. Experiment

Fig. 7 depicts the photograph of the developed three-stage HPA module. The multilayer ceramic substrate is employed to reduce the module size. The HPA module size is 0.08 cm^3 (7 mm $\times$ 7 mm $\times$ 1.7 mm).

Fig. 8 shows the measured output power $P_{\rm out}$, ACP (5-MHz offset), next adjacent channel leakage power (NACP) (10-MHz

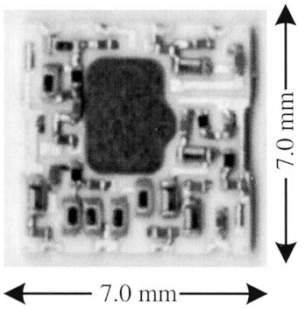

Fig. 7. Developed three-stage HPA module, size of which is 0.08 cm^3 (7 mm $\times$ 7 mm $\times$ 1.7 mm).

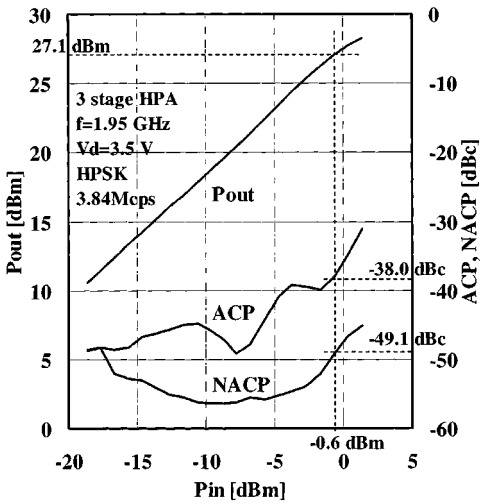

Fig. 8. Measured output power ($P_{\rm out}$), ACP, and NACP of the developed HPA module.

offset) of the developed HPA module at 1.95 GHz. Fig. 9 presents the PAE and the drain current I_d of the developed HPA module. An HPSK modulated signal with a chip rate of 3.84 Mc/s was used. The supplied drain voltage V_d is 3.5 V

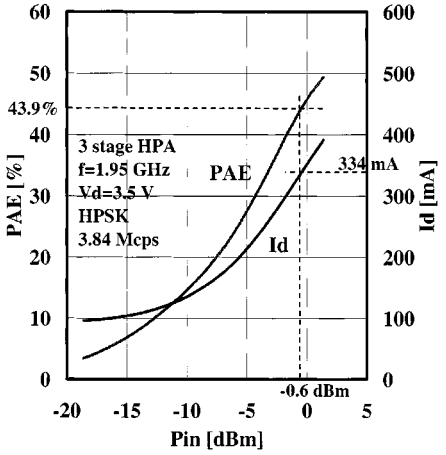

Fig. 9. Measured PAE and drain current (I_d) of the developed HPA module.

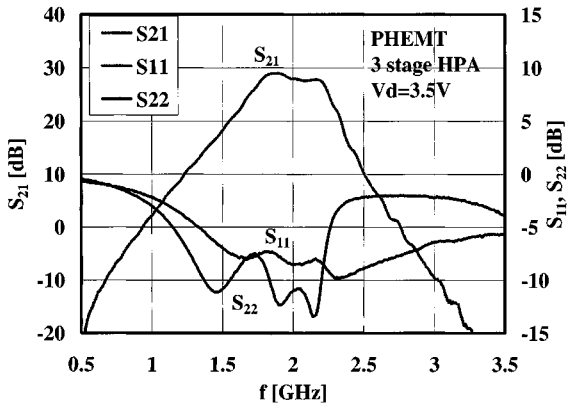

Fig. 10. Measured S-parameters of the developed HPA module.

and bias condition is Class AB. The HPA module achieved a PAE of 43.9% and an output power of 27.1 dBm with an ACP of −38 dBc and an NACP of −49.1 dBc. An associated gain of 27.7 dB and a drain current of 334 mA were obtained. High efficiency with the specified distortion characteristics are achieved by using the proposed HPF/LPF interstage matching circuit. Fig. 10 shows the measured S-parameters of the developed HPA module. A linear gain S_{21} of 28.5 dB, an input return loss S_{11} of −8.2 dB, and an output return loss S_{22} of −11.2 dB were obtained at 1.95 GHz.

VII. Conclusion

In this paper, we have proposed the HPF/LPF combined interstage matching circuit, which provides both optimum source impedance of the final-stage FET and optimum load impedance of the driver-stage FET. The proposed HPF/LPF interstage matching circuit has been applied to a three-stage HPA module for wide-band CDMA cellular phones. The fundamental and second harmonic load impedances of the final-stage FET were also optimized by the output matching circuit. The multilayer ceramic substrate has been used to reduce the size of the HPA module. Having the size of 0.08 cm^3 (7 mm × 7 mm × 1.7 mm), the HPA module achieved a PAE of 43.9% and an output power of 27.1 dBm with an ACP (5-MHz offset) of −38 dBc at 1.95 GHz. It was verified that the proposed HPF/LPF combined interstage circuit is useful to realize high efficiency with the specified distortion of HPAs used for personal cellular phones.

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