Temperature-Dependent Small-Signal and Noise Parameter Measurements and Modeling on InP HEMTs

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***Abstract*—In this paper, we present detailed on-wafer S-parameter and noise parameter measurements and modeling of InP/InAlAs/InGaAs high electron mobility transistors (0.1-μm gate length) at cryogenic temperatures. Various physical effects influencing small-signal parameters, especially the radio-frequency (RF) transconductance and RF output resistance and their temperature dependence, are discussed in detail. Accurate on-wafer noise parameter measurements are carried out from 300 to 18 K, and the variation of the equivalent noise temperatures of drain and source (T_d and T_g) are modeled against temperature. Based on these models, a cryogenic low-noise amplifier in the Ka-band is developed with a record-low noise temperature of 10 K.**

***Index Terms*—Cryogenic, high electron mobility transistor (HEMT), impact ionization, low-noise amplifier (LNA), noise, small-signal model.**

I. Introduction

ADVANCES in the technology of GaAs and InP-based high electron mobility transistors (HEMTs) combined with cryogenic cooling have resulted in low-noise amplifiers (LNAs) with excellent performance. The performance of InP-based LNAs operated at cryogenic temperatures especially compares well with that of solid-state masers. Various applications have emerged, over the years, for systems based on InP HEMTs in fields such as radio astronomy, ground-based receivers in deep space network (DSN), automotive radar, atmospheric science, very wide-band communications, etc. The first two applications use cryogenically cooled amplifiers.

The noise temperature $(T_{\min})$ as well as the frequency performance of field-effect transistor (FET)-based amplifiers is steadily improving: for example, at an ambient temperature $(T_{\rm amb})$ of 18 K and at a frequency of 4.75 GHz, the $T_{\min}$ was 20 K in year 1980 [1], about 15 K at 43 GHz in 1993 [2], and 30 K at 102 GHz ($T_{\rm amb} = 24$ K) in 1999 [3]. The last two results were obtained with InP HEMTs. The noise figures at cryogenic temperatures of the InP HEMTs reported so far are derived from measurements on multistage amplifiers, as opposed to on-wafer noise parameter measurements on a discrete transistor. Since the noise figure minimum $(F_{\min})$ of the devices becomes very small at cryogenic temperatures, on-wafer techniques have to be developed to measure it accurately. The only previous report of cryogenic on-wafer $F_{\min}$ measurements is on GaAs pseudomorphic HEMTs (pHEMTs) to a temperature of 80 K [4]. Although that paper demonstrates the feasibility of such measurements by standard hardware, the limited sensitivity of the measurements resulted in $F_{\min}$ values of nearly zero even at a temperature of about 100 K, while in reality an LNA still exhibits still substantial noise at these temperatures.

In this paper, we present on-wafer measurements of dc, S-parameter, and noise parameter measurements down to 18 K on InP/InAlAs/InGaAs HEMTs. We develop accurate small-signal and noise models at these temperatures, and to our knowledge these are the first on-wafer noise measurements and models at these temperatures. We also present the performance of a cryogenic LNA in the Ka-band with a record low noise temperature of 10 K. The important features of this paper are 1) first on-wafer noise parameter measurements down to 18 K on state-of-the-art InP HEMTs, 2) determination of the noise model as a function of temperature, and 3) development of an LNA with record low noise temperature in the Ka-band.

This paper is organized as follows. In Section II, we present the device structure and fabrication procedure of the InP pHEMTs. Details of the measurement techniques are presented in Section III. Results of dc, S-parameter measurements, and extraction of cryogenic small-signal models are presented in Section IV with emphasis on the extraction of parasitic elements. The results of on-wafer cryogenic noise parameters and the variation of the drain equivalent noise temperature are presented in Section V. In Section VI, the influence of such high field effects as impact ionization is discussed on the excess gate-leakage current, the small-signal output conductance (derived from S-parameters), and the noise figure minimum. The performance of a Ka-band LNA is reported in Section VII, followed by conclusions.

II. Device Structure and Fabrication

MBE grown InP high electron mobility transistors of gate dimensions 0.1 $\times$ 80 μm and an 80% InAs molefraction in the InGaAs channel are studied in this paper. The layers were grown on semi-insulating InP substrates with a lattice-matched InAlAs

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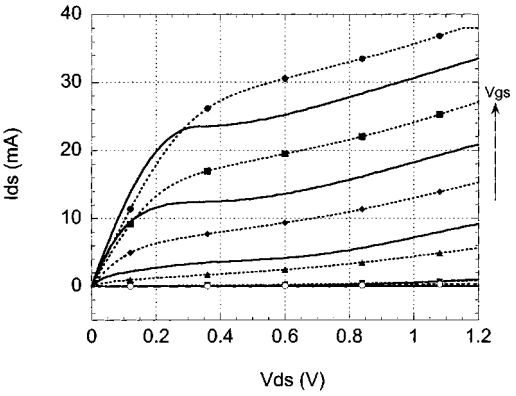


Fig. 1. Variation of the drain current with drain source voltage. $V_{gs} = 0.26, 0.14, 0.02, -0.1, -0.22, -0.26$ V ..... = 300 K, ___ = 18 K.

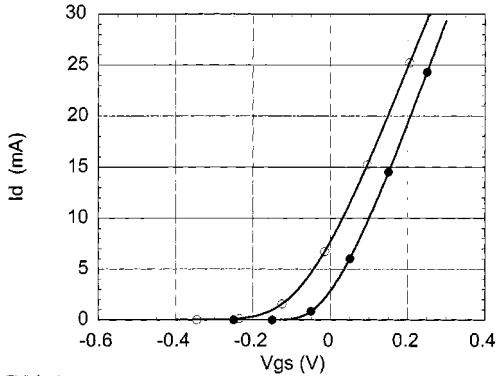


Fig. 2. Variation of the drain source current with gate-source voltage at 300 K (open circles) and 18 K (full circles).

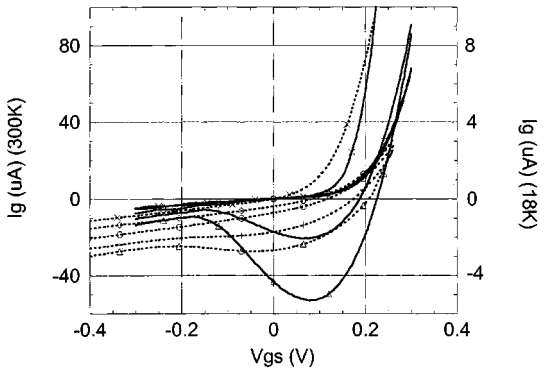


Fig. 3. Variation of the gate current as a function of gate-source voltage ..... = 300 K, ___ = 18 K. The left-hand Y-axis is for 300 K, and the right-hand Y-axis is for 18 K. [$V_{ds} = 0$ V (cross mark symbol), 0.4 V (diamond symbol), 0.8 V (open circles), 1.2 V (plus mark symbol), 1.4 V (open triangle symbol).]

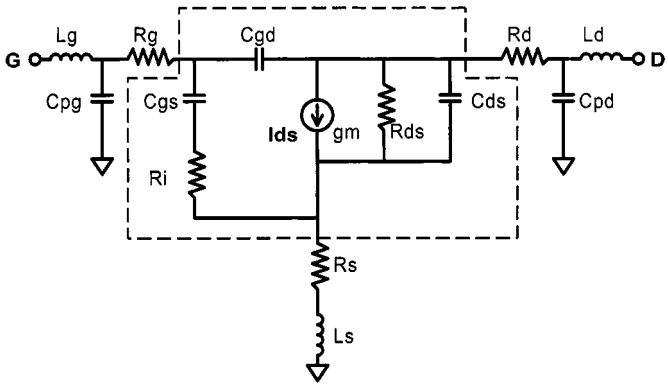


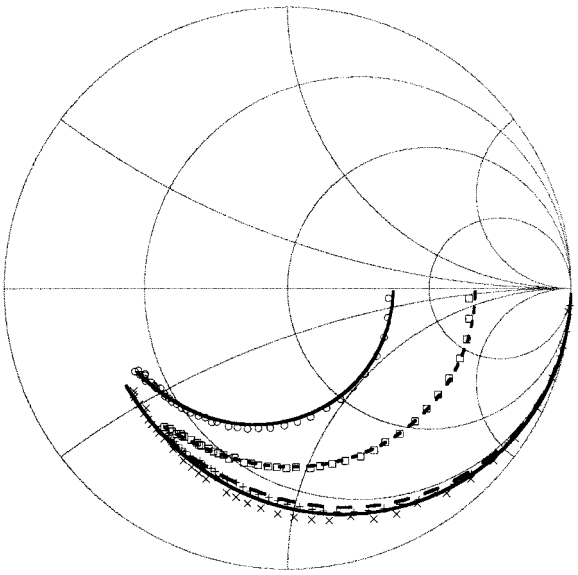
Fig. 4. The equivalent circuit diagram of an HEMT used for parameter extraction and modeling.

buffer layer. The layer structure is as follows: InP substrate/InAlAs buffer layer/InP buffer/undoped InGaAs channel/undoped InAlAs spacer layer/silicon delta doped layer/undoped InAlAs Schottky layer/n-type InGaAs cap. The sheet carrier density and the channel mobility at room temperature as determined by Hall measurements are 6×10^{12} cm^{-2} and 15 000 cm^{2}V^{-1}s^{-1}, respectively. Higher compositions of indium are chosen for the channel layer so as to improve the carrier confinement and electron mobility in the channel and consequently obtain higher cutoff frequency and lower noise. The devices were fabricated using TRW's InP HEMT process, which eliminated capacitor, thin-film resistor, and back-side via process steps. The devices were also not passivated in this study.

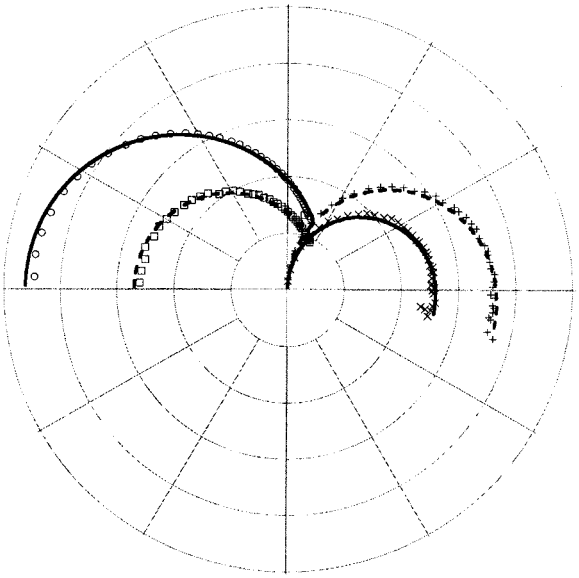
III. Measurements and Device Characterization

On-wafer dc, S-parameter, and noise parameter measurements are performed in this work for a detailed characterization of the device. The measurements are carried out on a Cascade Microtech probe station at room temperature and in a cryogenic on-wafer probe station [5] at low temperatures to 18 K. S-parameter measurements are performed using an HP 8510C network analyzer employing on-wafer load reflect match (LRM) calibrations at each temperature of measurement. Noise parameter measurements are performed utilizing an ATN microwave system with an HP346C diode as the noise source.

For low-temperature measurements, the samples are mounted in a cryogenic microwave probe station. It contains ports for RF cables, temperature sensors, vacuum pumps, and coplanar probes. The probes are attached to micromanipulators through bellows. The system is cooled by a closed-cycle Helium refrigerator. The probe body rests on a copper block attached to a fiberglass post, and the copper block itself is thermally anchored to the cold head using copper braids. Decoupling and damping of vibrations is achieved by mounting the whole system on a custom-made optical bench. The system allows small-signal microwave measurements from 0 to 50 GHz over a physical temperature range of 16–300 K. A vacuum of 10^{-6} Torr is maintained in the chamber during the measurements. For noise parameter measurements, the noise diode and noise modules (mismatched noise source and the receiver module) are at room temperature outside the cryogenic chamber. The noise modules are connected to the coplanar probes through short (4 in) semirigid cables. The temperature of the samples is monitored with an Omega CY7 diode. At low temperatures, since the $F_{\min}$ is very small, care is taken to see that the source impedance (Z_s) points are selected not too close to $Z_{\rm opt}$ so that the noise figure is measured with better accuracy. A special sample mount for cryogenic temperatures is designed to enable translation of the sample and the calibration substrate while the probes remain stationary. The key elements of distinction in this work that



(a)

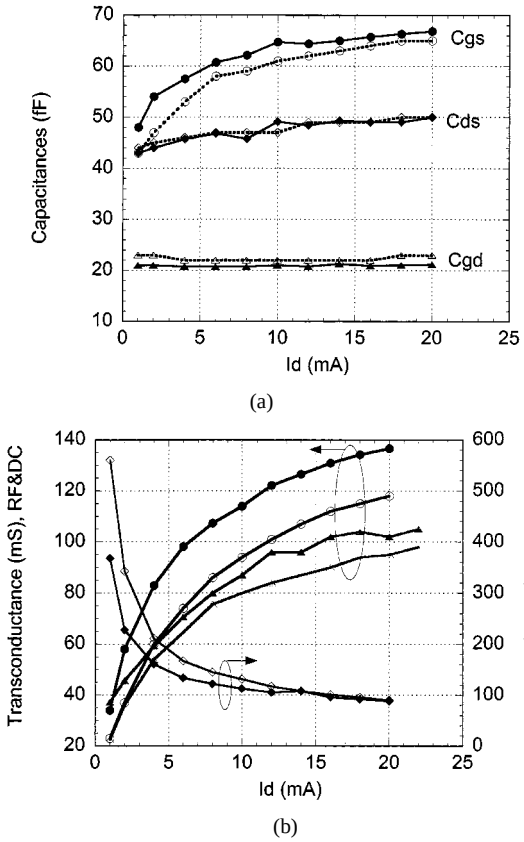


(b)

Fig. 5. Measured and modeled S-parameters at 18 K and at drain currents of 2 and 20 mA. The frequency range is 0.2–50 GHz. (a) Cross mark symbol = measured S_{11} at $I_{\rm ds} = 20$ mA. Open circle symbol = measured S_{22} at $I_{\rm ds} = 20$ mA. Plus mark symbol = measured S_{11} at $I_{\rm ds} = 2$ mA. Open square symbol = measured S_{22} at $I_{\rm ds} = 2$ mA. ____ = modeled at $I_{\rm ds} = 2$ mA. —— = modeled at $I_{\rm ds} = 20$ mA. (b) Open circle symbol = measured S_{21} at $I_{\rm ds} = 20$ mA (scale $S_{21}/8$). Cross mark symbol = measured S_{12} at $I_{\rm ds} = 20$ mA (scale $S_{12}*4$). Open square symbol = measured S_{21} at $I_{\rm ds} = 2$ mA (scale $S_{21}/8$). Plus mark symbol = measured S_{12} at $I_{\rm ds} = 2$ mA (scale $S_{12}*4$). ____ = modeled at $I_{\rm ds} = 20$ mA. —— = modeled at $I_{\rm ds} = 2$ mA).

are responsible for the stability of the calibrations and accuracy and repeatability of the measurements at cryogenic temperatures are:

1) the use of short feedthrough cables connecting the noise modules to the probes so that the impedance points are well spread and are not simply crowded at the 50 Ω point;
2) manual selection of the constellation of the impedance points on the Smith chart that are not too close to $Z_{\rm opt}$ so that the noise figure is measured with better accuracy at a given Z_s



(a)

(b)

Fig. 6. (a) The variation of the intrinsic capacitances $C_{\rm gs}$ (open/full circle symbol), $C_{\rm ds}$ (open/full diamond symbol), and $C_{\rm gd}$ (open/full triangle) as a function of the drain current at 300 K (—— and open symbols) and 18 K (____ and full symbols). (b) The variation of g_m (open/full circle symbol) and $R_{\rm ds}$ (open/full diamond symbol) obtained from small-signal analysis as a function of the drain current. Also dc-g_m (open/full triangle) is shown for comparison. Open symbols: 300 K and full symbols: 18 K.

3) keeping the probes stationary during calibrations and measurements so that the calibrations remain stable;
4) the decoupling of any small vibrations of the system reaching the sample so that the sample temperature and the calibrations are not disturbed during experiments.

The four noise parameters are derived from the raw noise figure data (measured at 32 source impedance points) by a modified Lane's method [6].

IV. DC Data, S-Parameters, and Small-Signal Modeling

A. DC Characteristics

Fig. 1 shows the I_d–$V_{\rm ds}$ characteristics of the device at 300 and 18 K. It can be seen that the drain current for a given $V_{\rm gs}$ is smaller at lower temperatures. We noticed the same trend for intermediate temperatures between 300 and 18 K also. It can be seen that from Fig. 1, the device pinches off at higher values of $V_{\rm gs}$ for lower temperatures. The I–V characteristics are light-independent and show no hysterisis behavior, confirming that the material is of good quality. Fig. 2 shows the $I_{\rm ds}$-$V_{\rm gs}$ characteristics at 300 and 18 K. The $I_{\rm ds}$ varies as $\sim(V_{\rm gs}$-$V_t)$ as expected for short-channel devices. Here V_t is the threshold voltage [7]. The dc g_m was observed to be about 1300 mS/mm at 18 K.

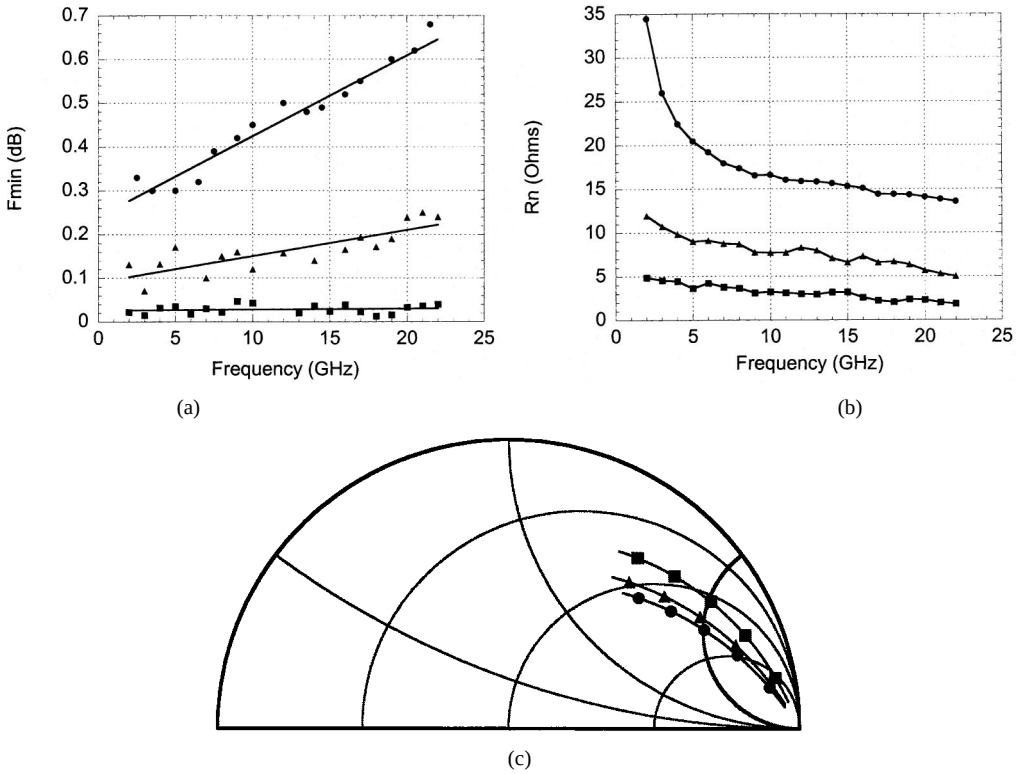


Fig. 7. Variation of (a) $F_{\min}$, (b) R_n, and (c) $\Gamma_{\rm opt}$ at 300 K (circle symbol), 200 K (triangle symbol), and 18 K (square symbol) in the frequency range 2–22 GHz.

Fig. 3 shows the gate current characteristics with $V_{\rm ds}$ as a parameter. At higher values of $V_{\rm ds}$, that is, as the electric field along the channel increases, the gate current shows a drastic increase as apparent from the bell shape of the I_g–$V_{\rm gs}$ curve. This is due to the impact ionization resulting in the generation of excess electron-hole pairs in the channel [8]. The additional electrons travel toward the drain and cause an increase in the drain current while the holes remain confined and drift parallel to the channel toward the source and recombine. However, when the field is sufficiently high, some holes surmount the heterojunction barrier and reach the gate and cause severe increase in the gate current. It can be seen that the gate current, which is a sum of the Schottky gate-leakage current and hole current due to impact ionization, decreases drastically at low temperatures. As can be seen from this plot, both of these components decrease substantially with temperature.

B. S-Parameters and Small-Signal Modeling

1) Determination of the Extrinsic Elements: The small-signal equivalent circuit is shown in Fig. 4 for the InP HEMT. We have used this topology up to 50 GHz on InP HEMTs over a complete range of bias conditions and temperatures. The part inside the dotted box represents the intrinsic part of the device. Accurate determination of the extrinsic elements is essential for proper deembedding. For consistent and correct extraction of the extrinsic parameters, we used a combination of methods:

1) coldfet method due to Dambrine *et al.* [9];
2) S-parameters of the unbiased FET [10];
3) fitting the evolution of forward-biased $(V_{\rm gs} > 0)$ coldfet Z-parameters with frequency [11];
4) geometrical considerations of the pads.

The extrinsic capacitances $C_{\rm pg}$ and $C_{\rm pd}$ are obtained by biasing the device at $V_{\rm ds} = 0$ and applying extremely high reverse bias to the gate diode until both S_{11} and S_{22} become capacitive. This situation can be easily described in terms of the Y-parameters, and the capacitances can be obtained accurately. The inductances are obtained by keeping $V_{\rm ds} = 0$ and applying a forward bias to the gate high enough for S_{11} and S_{22} to become inductive. The inductances are obtained from the imaginary parts of the Z-parameters and the resistances from the real parts. These values are compared with those obtained by the method of Miras *et al.* [11], which does not require overly high forward biases on the gate (thus preventing irreversible damage to the device) but only involves fitting the frequency evolution of the Z-parameters of the device. Through a few iterations, we could arrive at unique values for the inductances. The forward coldfet S-parameters are measured at several closely spaced $V_{\rm gs}$ values to enable a complete determination of the parasitic resistances [9]. An initial value for channel resistance is obtained from the geometrical and doping parameters of the channel and then fine-tuned during optimization.

2) Determination of the Intrinsic Elements: The extrinsic elements are deembedded from the measured S-parameters of the device through a series of matrix transformations, which finally express the Y-parameters of the intrinsic part of the device as

$$Y_{\rm int} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} -\frac{j\omega C_{\rm gs}}{1+j\omega C_{\rm gs}\cdot R_i} + j\omega C_{\rm gd} & -j\omega C_{\rm gd} \\ \frac{g_m\cdot\exp(-j\omega\tau)}{1+j\omega C_{\rm gs}\cdot R_i} - j\omega C_{\rm gd} & g_{\rm ds} + j\omega(C_{\rm gd}+C_{\rm ds}) \end{bmatrix}.$$

Here R_i is the intrinsic channel resistance, τ is the transconductance delay time, $g_{\rm ds}$ is the output conductance, g_m is the

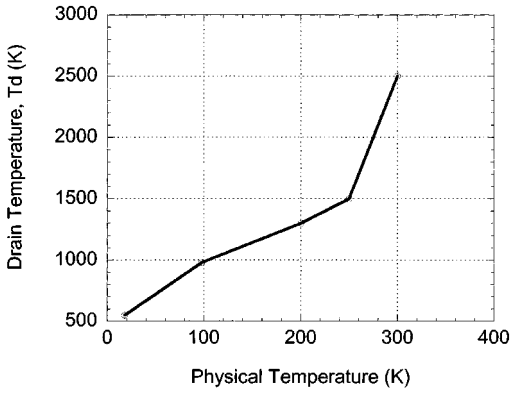


Fig. 8. Variation of the equivalent drain noise temperature as a function of the device physical temperature obtained from Pospieszalski model.

transconductance, and $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are the gate-source, gate-drain, and drain-source capacitances, respectively.

Fig. 5 shows the measured and modeled S-parameters for two different bias conditions at 18 K. The excellent agreement over such bias extremes, represented in the figure, is a result of the accurate determination of the parasitics. Fig. 6(a) and 6(b) shows the variation of the intrinsic capacitances, RF transconductance, and output resistance values as a function of the drain current for 300 and 18 K. It can be seen that g_m increases by about 20% at cryogenic temperatures while all other elements remain almost the same. The value of τ, the transconductance delay time—which represents the time taken for the redistribution of channel charge after a gate voltage excitation—was found to be somewhat difficult to extract uniquely. Good fits were obtained for values of τ between 0.3–0.8 ps. Since this parameter becomes important only beyond the f_t of the device (which is about 230 and 280 GHz at 300 and 18 K, respectively, for optimum bias conditions), its effect on the determination of any other parameter is negligible. The value of R_i was obtained to be between 1.5 and 2.5 Ω at 18 K. We have also verified that all the parameters show correct trends with bias (Fig. 6). For example, g_m was found to increase with increasing drain current as expected. In Fig. 6, it can be seen that the dc-g_m obtained from the $I_{\rm ds}$–$V_{\rm gs}$ data ($g_m = (dI_d/dV_{\rm gs})$) is somewhat smaller than the RF-g_m obtained from small-signal modeling. Extrinsic g_m ($g_{\rm me}$) is given as

$$g_{\rm me} = \frac{g_{\rm mi}}{1 + R_s \cdot g_{\rm mi}}.$$

Since the effect of R_s is removed through deembedding, the RF-g_m actually represents the intrinsic g_m (g_{mi}) of the device. The variation of the output resistance $R_{\rm ds}$ ($=1/g_{\rm ds}$) is dependent on the biasing regime, i.e., whether the device is biased near pinchoff or away from it. This will be discussed further in Section VI-A, along with the underlying physical mechanisms.

V. Noise Parameter Measurements and Modeling

Fig. 7(a) shows the variation of noise figure minimum with temperature. It can be seen that $F_{\rm min}$ reduces by almost an order of magnitude as the temperature is lowered to 18 K. Fig.7(b) shows the noise resistance for various temperatures. It can be seen that R_n decreases from about 17 Ω at 300 K to 3 Ω at 18 K, indicating that $F_{\rm min}$ is less sensitive to the source impedance at low temperatures. The variation of $\Gamma_{\rm opt}$ is shown in Fig. 7(c). It can be seen that at lower temperatures, $\Gamma_{\rm opt}$ moves closer to the periphery of the Smith chart.

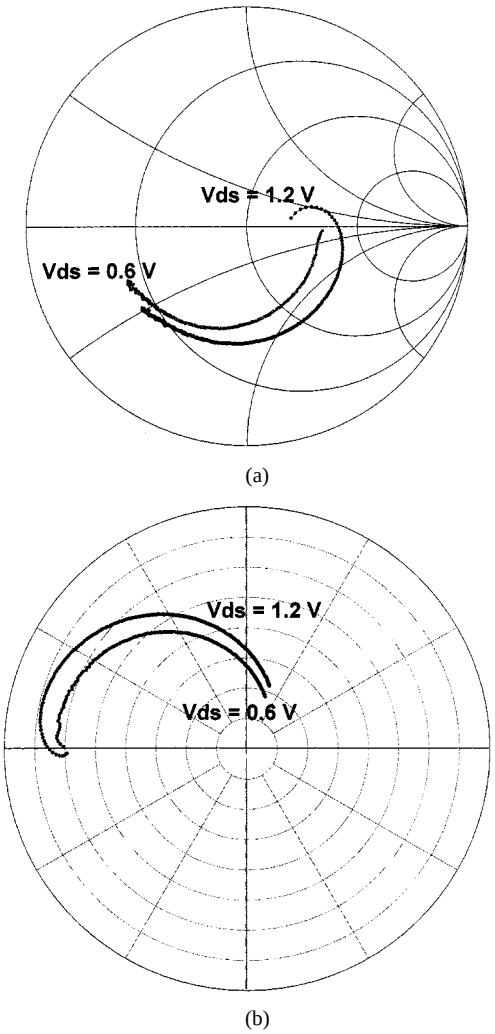


Fig. 9. (a) S_{22} of the device at $V_{\rm ds} = 0.6$ V and at $V_{\rm ds} = 1.2$ V. The inductive regime at 1.2 V represents the effect of impact ionization. (b) Corresponding S_{21}. The temperature is 300 K and frequency range is 0.2–50 GHz.

The measured noise parameters and the small-signal equivalent circuit parameters are sufficient in calculating the two-source Pospieszalski noise model [12]. The two sources of noise are described by a noise voltage source ($\overline{e_{\rm gs}^2}$) on the gate port in series with R_i and a noise current source ($\overline{i_{\rm ds}^2}$) on the drain side parallel to $g_{\rm ds}$. These noise sources are given as

$$\overline{e_{\rm gs}^2} = 4kT_g \cdot R_i \cdot \Delta f$$
$$\overline{i_{\rm ds}^2} = 4kT_d \cdot g_{\rm ds} \cdot \Delta f$$

where T_g and T_d are the noise equivalent temperatures at the gate and drain, respectively, with R_i and $g_{\rm ds}$ assumed to be at

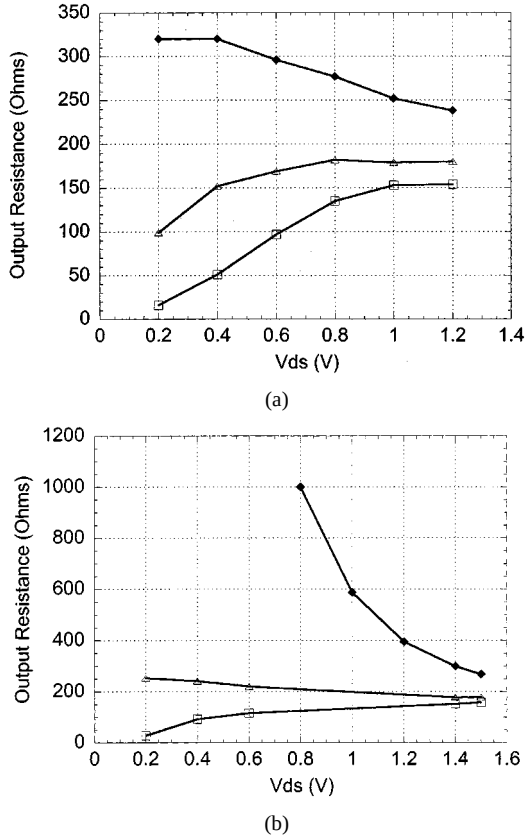


Fig. 10. Variation of the small-signal $R_{\rm ds}$ (Ω) against the drain source voltage. $V_{\rm gs} = -0.1$ V (full-diamond symbol), 0 V (open triangle), 0.2 V (open square) at (a) 300 K and (b) 18 K.

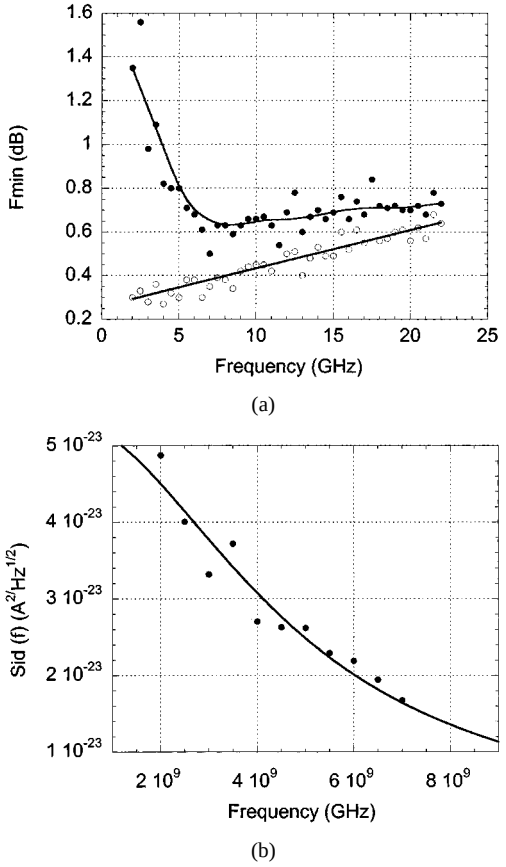


Fig. 11. (a) Variation of $F_{\rm min}$ with frequency for $V_{\rm ds} = 0.4$ V (open circle) and $V_{\rm ds} = 0.8$ V (full circle) at 300 K. The smooth line for the 0.8-V curve is to guide the eye. The low-frequency behavior at 0.8 V is indicative of the effect of impact ionization. (b) Fit of the low-frequency behavior of $F_{\rm min}$ to a Lorentzian function. $F_{\rm min}$ is converted to the spectral density.

0 K. All four noise parameters can be expressed in terms of T_g, T_d, and the small-signal elements as [12]

$$X_{\rm opt} = \frac{1}{\omega C_{\rm gs}}$$

$$R_{\rm opt} = \frac{ft}{f}\sqrt{\frac{r_i T_g}{g_{\rm ds} T_d}}$$

$$T_{\rm min} = 2\frac{f}{f_T}\sqrt{g_{\rm ds} T_d r_i T_g}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{\rm ds} T_d}{T_0}$$

where $X_{\rm opt}$ and $R_{\rm opt}$ are, respectively, the imaginary and real parts of the optimal source impedance for minimum noise. Utilizing the noise parameters measured at each temperature and the corresponding small-signal model, the drain temperature has been extracted and is depicted in Fig. 8 as a function of the physical temperature of the device. It can be seen that T_d is about 500 K at 18 K and is about 2500 K at RT. The gate temperature (T_g) is obtained to be close to the ambient temperature.

VI. Impact-Ionization Effects on S-Parameters and Noise

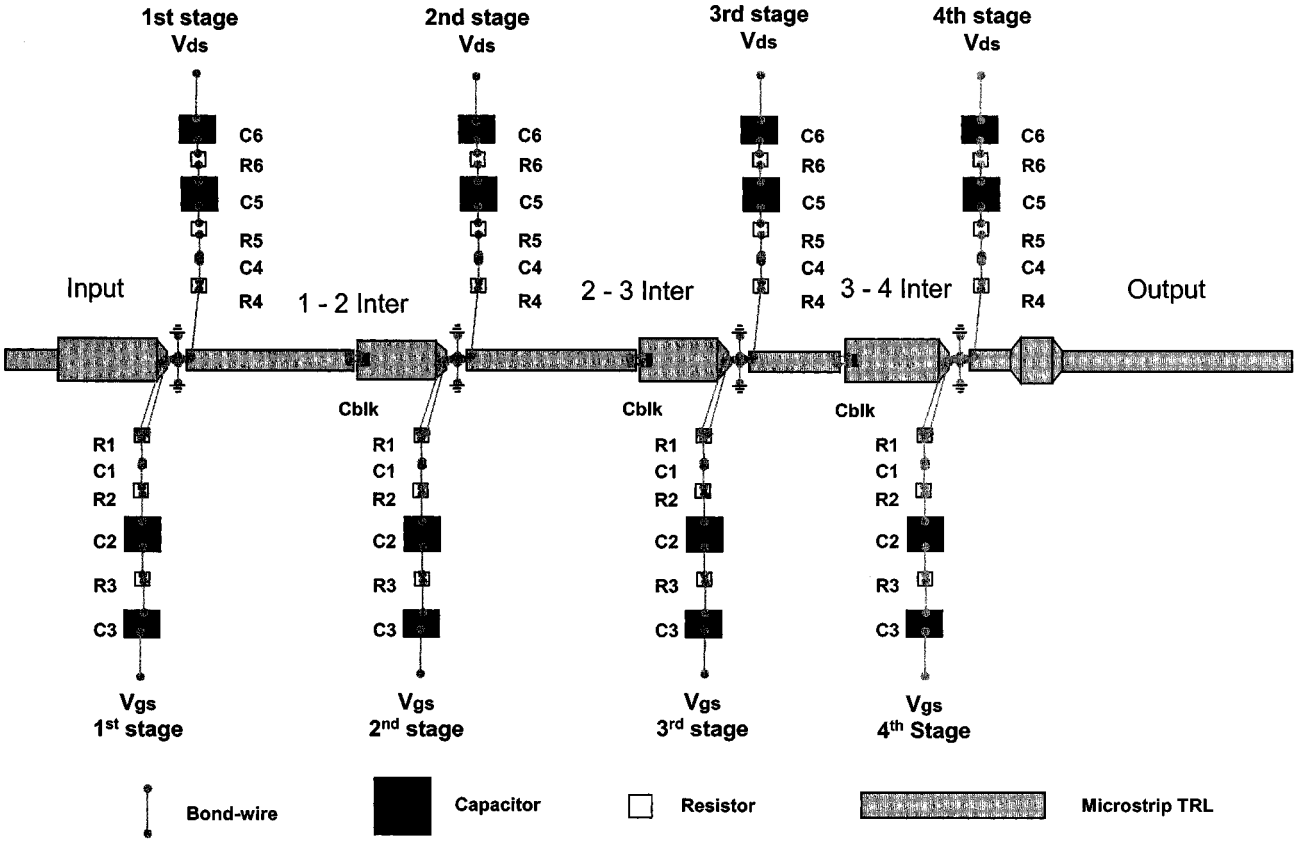
A. Effect of Impact Ionization on the Small-Signal Output Resistance

When the $V_{\rm ds}$ is high, the high electric field along the channel results in the generation of additional electron-hole pairs due to impact ionization. These additional carriers cause an increase in the conductance of the channel, and so its effect is most seen on S_{22}. Fig.9(a) shows S_{22} for two different values of $V_{\rm ds}$ at 300 K. The inductive component of S_{22}, which becomes predominant as $V_{\rm ds}$ increases, arises because of a phase lag between the drain voltage waveform and the impact ionization current [13]. Due to the dispersion of the output conductance, the forward transmission S_{21} is also reduced at lower frequencies, as can be seen from Fig. 9(b). The effect of impact ionization can be incorporated into the small-signal model by introducing a voltage-controlled current source at the output port, as discussed by Reuter *et al.* [14] in one such approach.

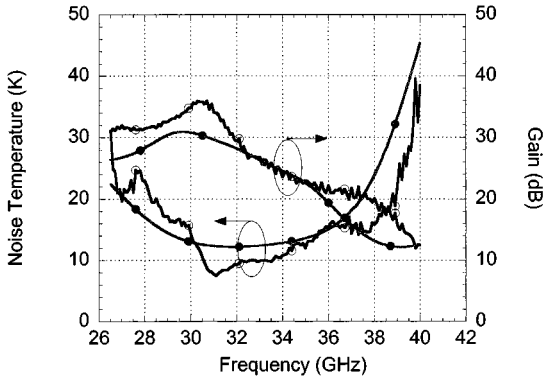
Fig. 10(a) and (b) shows $R_{\rm ds}$ (obtained from small-signal modeling) as a function of $V_{\rm ds}$ at 300 and 18 K. At higher values of $V_{\rm gs}$, the contribution of impact ionization current to the total drain current is much smaller and the output resistance shows the expected behavior of increasing with $V_{\rm ds}$ and reaching saturation as typical of short-channel devices. At gate voltages close to pinchoff and high enough drain voltages, the total current is dominated by the impact-ionization current, which increases with increasing $V_{\rm ds}$. As a result, the output resistance decreases with increasing $V_{\rm ds}$, as can be seen in Fig. 10(a) and (b).

B. Effect of Impact Ionization on Noise

With regard to the measurement of $F_{\rm min}$ as a function of $V_{\rm ds}$, we observed certain interesting trends. At low values of $V_{\rm ds}$,



(a)



(b)

Fig. 12. (a) Layout of the Ka-band cryogenic hybrid four-stage LNA module. The HEMTs are $0.1 \times 80\ \mu$, four-finger devices. The resistors R1–R6, capacitors C1-C6, and bond wires constitute the biasing network. The transmission lines and the bond wires constitute the interstage maching. $C_{\rm blk}$ is the dc-blocking capacitor (R1, R4 $= 50\,\Omega$, R2, R5, R6 $= 10\,\Omega$, R3 $= 1000\,\Omega$, C1 $= 0.2$ pF, C2, C5 $= 15$ pF, C3, C6 $= 680$ pF, C4 $= 0.8$ pF, and $C_{\rm blk} = 0.2$ pF). (b) Noise temperature and gain of a four-stage LNA operating at 16 K. Full-circle symbol = model and open-circle symbol = measurement.

below 0.5 V in the present case of 80% indium devices, $F_{\rm min}$ increases monotonically with frequency as expected. However, as $V_{\rm ds}$ increases, we found that $F_{\rm min}$ actually decreases with increasing frequency up to about 8 GHz. Beyond this frequency, $F_{\rm min}$ continues to increase. This behavior is shown in Fig. 11(a) for 300 K. Similar low-frequency behavior was pointed out by others as well [15]. The low-frequency noise figure in such a case can be described by fitting the noise spectral density $S_N(f)$ (in $\rm A^2$-$\rm Hz^{-1/2}$) to a Lorentzian function of the form [14], [16]

$$S_N(f) \propto \frac{\tau_i}{1+\omega^2\tau_i^2}$$

where $\omega = 2\pi f$ and τ_i is the impact ionization time constant (which is representative of the time between two impact ionization events). $S_N(f)$ is given as $4kT_n g_{\rm ds}$, where T_n is the noise temperature written from $F_{\rm min}$ as $T_n = (F'_{\rm min} - 1)T_0$. Here $F_{\rm min}$ (dB) $= 10\log(F'_{\rm min})$ and $g_{\rm ds}$ is the drain-source conductance obtained from small-signal modeling and $T_0 = 290$ K is the standard temperature used in noise calculations. Fig. 11(b) shows $S_N(f)$ plotted against frequency in the low-frequency regime and fitted to the Lorentzian function. This yielded a value of τ_i between 25 and 30 ps for all the samples. At higher frequencies, standard mechanisms of noise come into play and $F_{\rm min}$ increases linearly with frequency.

VII. LNA Results

The device model was subsequently used to design a four-stage LNA module. The LNA module is based on an earlier module, developed by Pospieszalski, National Radio Astronomy Observatory (NRAO), that uses Fujitsu (Part #.Fhr10x) devices. The current design incorporates the WR28 to microstrip input and output transitions and a bias circuit comparable to the NRAO module. The circuit layout is shown in Fig. 12(a). The input, interstage, and output matching circuits are etched on Cuflon, and the dc blocking and bias circuitry use surface mount, thin-film resistors and capacitors. The LNA module was designed with the aid of the software tools MMICAD and Sonnet. Additionally, measurements of passive components on the wafer probe station were used to verify, enhance, and extend passive component models. The design approach was to minimize the noise temperature at 32 GHz while maintaining LNA stability from 0 to 100 GHz at the physical temperature of 12 K.

Since the device is unstable (mu-factor <1) from 0 to 100 GHz [17], the bondwires and bias circuit networks are used to first stabilize the devices. The gate, drain, and source bondwire lengths are used to control the stability near 32 GHz, while the gate bias and drain bias circuits control the lower band and upper band stability, respectively. Then each of the stages is iteratively matched to its optimum source impedance.

The LNA module was then measured at a physical temperature of 16 K in a closed-cycle refrigerator using a cooled 20-dB waveguide attenuator [18]. Fig. 12(b) shows the noise temperature and gain of the final amplifier module. Here $V_{\rm ds} = 0.6$ V and $I_d = 3.5$ mA. The results indicate that the LNA model and measurement are in relatively good agreement. The gain measurement error is ± 0.5 dB, while the noise measurement error is ± 2.0 K.

VIII. Conclusion

Detailed measurements of dc, S-parameter, and noise parameters are carried out at cryogenic temperatures on InP/InAlAs/InGaAs HEMTs. A small-signal model and noise model are developed, and the variation of the drain equivalent temperature against physical device temperature is discussed in detail. A cryogenic hybrid four-stage LNA with a record low noise temperature of 10 K is demonstrated. These results represent the first on-wafer noise parameter measurements and modeling at such low temperatures as 18 K.

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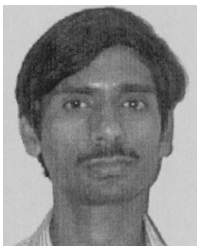

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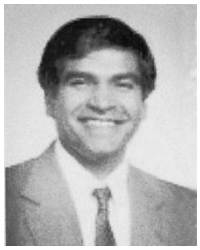

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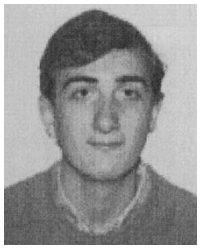

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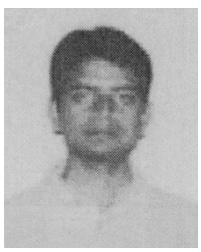

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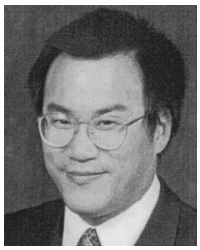

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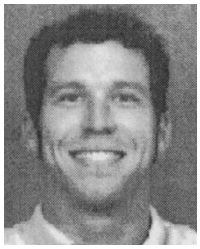

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P. Chin photograph and biography not available at time of publication.

P. H. Liu, photograph and biography not available at the time of publication.