Bias-Dependent Linear Scalable Millimeter-Wave FET Model

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***Abstract*—This paper describes a measurement-based bias-dependent linear equivalent circuit field-effect-transistor/high-electron-mobility-transistor model that is accurate to at least 100 GHz and scalable up to 12 parallel gate fingers and from 100 to 1000 μm total gate width. A new and accurate technique for extracting the Z-shell parameters has been developed, and the scaling rules for all the parasitic elements have been determined. The intrinsic equivalent circuit element values are determined at each bias point in $V_{\rm gs}$–$V_{\rm ds}$ space and interpolated by splines between points.**

***Index Terms*—Equivalent circuits, microwave field-effect transistors (FETs), millimeter-wave FETs, modeling.**

I. Introduction

LINEAR field-effect transistor (FET) models are widely used in the design of active linear monolithic microwave integrated circuits (MMICs). The linear FET model is an equivalent circuit representation of the small-signal electrical behavior, or S-parameters of the FET, over a very wide frequency range at any user-specified dc operating point. The equivalent circuit model is a compact representation of the S-parameter performance of the FET and provides an intuitive description of the FET electrical behavior. This has a number of advantages over using the S-parameters directly in a circuit design.

1) The scaling of the model with device dimensions can be readily determined from the expected scaling of the individual model elements. For example, a model capacitance element may be expected to scale straightforwardly with FET gate width, whereas the total FET input resistance, the real part of S_{11}, does *not* scale simply with gate width and number of gate fingers.
2) The model elements are frequency independent: this means that they can be extracted at a single frequency, for all bias points. This offers significant data reduction compared with storing all the S-parameters over all frequencies and bias points that can be measured, and reductions in measurement time and simulation time of the model.
3) The frequency dependence of the FET performance is determined by the arrangement of resistive and reactive components in the model. The model can then be used to predict the electrical performance of the FET, and hence the MMIC, at frequencies beyond the original measurement regime. This allows graceful degradation of the S-parameters beyond their measurement frequency, which is useful in circuits where other nonlinear components can create harmonics that may be beyond the measurement frequency range.
4) The linear equivalent circuit model is generally more accurate than a linearized large signal model for predicting the FET S-parameters.

The component elements of the equivalent circuit model can be obtained by direct extraction from the S-parameter measurements of the FET made at a single frequency (see, for example, Dambrine *et al.* [1], Berroth and Bosch [2], Hughes and Tasker [3]) or by optimization of the equivalent circuit elements (in whole or in part) from broadband S-parameter measurements (e.g., Lin and Kompa [4]). In both cases, the frequency independence of the model components is assumed. This criterion can be relaxed in the linear case but is essential for generalization of the model to the large-signal case. A major drawback with global parameter fitting by optimization is that the process can be inaccurate: local minima must be avoided, dependence on starting values may have an influence, and the resulting parameter values may also be unphysical, leading to difficulties with scaling. Direct extraction is generally simpler and quicker, and hence more appropriate for a production-oriented environment.

For the model to be a general-purpose design tool, it must be accurate over a range of bias points that may typically be used in MMIC circuit designs. This requires the FET to be measured over a wide range of bias space and the model extracted at each point. The variation of the equivalent circuit component values over gate and drain bias voltages can be determined. Their functional dependence is neither simple nor intuitive [1]. It is more straightforward to parameterize the elements by $(V_{\rm gs}, V_{\rm ds})$, and generate a lookup table of extracted component values. The equivalent circuit can then be determined quickly and easily at any bias, by direct lookup or spline interpolation between table points.

The purpose of this paper is to improve the accuracy and scalability of the bias-dependent linear equivalent circuit model so that it can be used with confidence for MMIC design at millimeter-wave frequencies up to at least 100 GHz. The work is directed primarily toward Agilent Microwave Technology Center's proprietary MESFET, pseudomorphic high electron-mobility transistor (pHEMT), and metamorphic high electron-mobility transistor (mHEMT) processes, and has been used successfully in the design of ICs, notably broadband amplifiers, operating in frequency ranges from 100 kHz to 110 GHz. The model has also been used successfully with several other commercial FET processes—for example, enhancement-mode pHEMTs—and the technique is sufficiently

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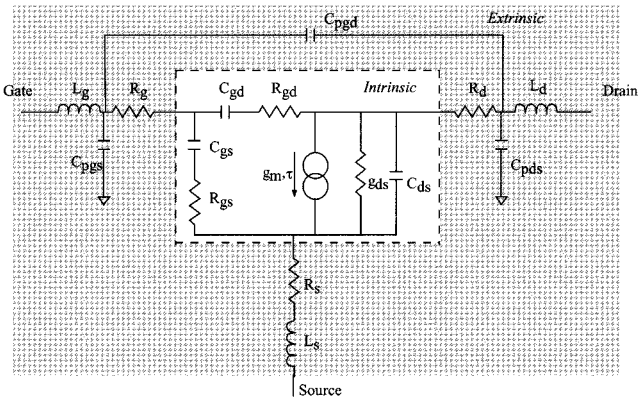

Fig. 1. "Typical" small-signal equivalent circuit [1]–[4], [6]–[18]. The intrinsic elements are in the clear box, and the extrinsic components are in the shaded area.

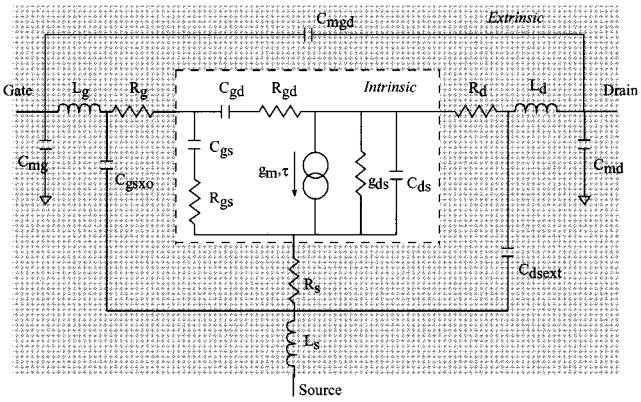

Fig. 2. The bias-dependent linear equivalent circuit model developed in this work. The intrinsic elements are in the clear box and are dependent on bias and frequency. The extrinsic components are in the shaded area and are independent of both bias and frequency.

general for three-terminal field-effect devices that can be described by this circuit topology. In summary, the goals of the model are that it must be the following.

1) *Accurate:* agreement between measured and modeled S-parameters at all frequencies and biases of interest.
2) *Scalable:* equivalent circuit component values scale with total gate width and number of parallel gate fingers, and the scaled-model predicts S-parameters accurately.
3) *Bias-dependent:* equivalent circuit component values are parameterized by bias at points over the entire usable $V_{\rm gs}$-$V_{\rm ds}$ space and interpolated by piecewise linear splines between points.

This paper will describe how the above goals have been met. The primary areas of investigation in the development of the model were the equivalent circuit topology: principally the extrinsic components, their extraction and scaling rules, and the calibration and measurement environment. Once the basic model topology and parameter extraction methodology had been verified, an automated measurement and table-model extraction process was developed. Each model that is constructed is verified against measured S-parameter data over a range of bias conditions, as part of the model production process [5]. Finally, the models are compared with S-parameter data measured to 110 GHz to illustrate the accuracy and scaling capabilities.

II. Equivalent Circuit Topology

Fig. 1 shows a "generic" small-signal model used by most workers [1]–[4], [6]–[18]. Elements inside the clear box labeled as *Intrinsic* attempt to describe the basic physics of operation of the FET itself. The remaining elements are *Extrinsic* or *Parasitic* components: these are part of the FET physical structure, which must be present to allow current flow to the intrinsic FET, and comprise the RF contact pad and metallization capacitances and inductances, for example. The more recent models place the pad capacitances outermost to simplify the extraction procedure by minimizing the number of impedance matrix inversions and improving the numerical accuracy [10]–[18].

The equivalent circuit topology developed in this study is shown in Fig. 2. The intrinsic components are in the clear box and are of the usual topology for depletion-mode FET devices. The intrinsic component values are determined at each bias point by direct extraction, after deembedding the extrinsic parameters [1]. The extrinsic parameters are shown in the shaded region and are a slightly more complex network than is usually found, in an attempt to model the multifinger gate and drain manifolds. In particular, two additional capacitance components are added to account for the interaction between the gate-source and gate-drain interdigitated metallizations. The extrinsic components are considered to be independent of applied bias. All the components in this equivalent circuit scale with gate width or number of fingers, or both. The accurate scaling of the extrinsic elements, in particular, is essential to obtain a model that will be scalable over a wide range of device dimensions.

III. Measurement Procedure

An array of 0.25-μm gate length InGaAs-channel pHEMTs, with total gate widths from 30 to 480 μm and number of gate fingers from 2 to 12, was prepared and measured to determine the equivalent circuit parameters and their scaling rules. The vias to the back side metallization are included in the measurement and the model parameters. We have also measured and modeled 0.35-μm gate length GaAs MESFETs and 0.12-μm gate length InGaAs-channel pHEMTs, in a variety of gate widths, up to 1 mm.

The S-parameter measurements for model extraction and verification to 50 GHz were made using an Agilent 8510C with a modified Agilent 8517B test set; measurements above 50 GHz were made using an Agilent 8510XF. DC bias was supplied by an Agilent 4142, with all instruments under computer control. All measurements were carried out on-wafer using air-coplanar probes.

Historically, the FET models were extracted from measurements made on test FETs in a coplanar environment, whereas the circuit applications are more typically in microstrip. While this approach is not uncommon, it was felt that better model accuracy could be obtained by extracting the model parameters from measurements made in the same circuit and electromagnetic environment as the application: microstrip. This

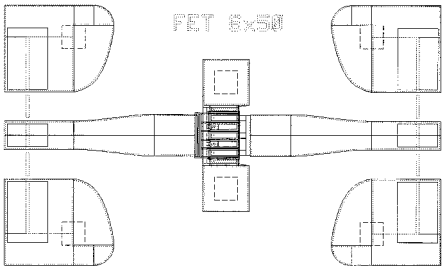

Fig. 3. A six-gate-finger 300-μm total gate width pHEMT with back-via contacts, located in 50-Ω CPW-to-microstrip transformers.

requires the use of coplanar waveguide (CPW)-to-microstrip transformers on the wafer as part of the FET test structure [19].

On-wafer microwave calibration standards for thru-reflect line (TRL) and line-reflect-match (LRM) methods have been designed in both microstrip and coplanar environments. For the standards, "guide marks" have been placed on the probe pads to improve the repeatability of probe placement from standard to standard, and hence improve the accuracy of both calibration and measurement [20]. The standards also place the measurement reference planes at the physical input and output of the test FET—the gate and drain "manifold" metallizations—thereby eliminating the probe pad parasitics from the measurement and subsequent extraction. A test FET with the CPW-to-microstrip transformers is shown in Fig. 3. The gate and drain manifold metallizations connecting the multiple gate and drain fingers to the input and output ports can be seen, and the multiple sources are connected to the back side vias by a further metallization "bus."

IV. Extrinsic Parameter Extraction

The extrinsic parameters are typically extracted using the "cold FET" method [1]: the drain-source voltage is set to zero, which effectively eliminates the controlled current source in the equivalent circuit, placing the FET in a passive condition. The equivalent circuit can then be simplified considerably, depending on the gate bias used. If the gate bias is set to below the pinch-off voltage, the equivalent circuit can be approximated by a network of capacitances that represent the gate capacitance and the capacitances of the metallizations of the device.

The pinched-off gate condition was used to determine the extrinsic capacitances of the array of test FETs. First, the two-gate-finger devices were measured to estimate the variation with gatewidth of the gate capacitance and the drain-source capacitance. These relations were then used in the multifinger devices to determine the influence of the manifold metallizations on the capacitances.

The condition of high forward gate bias that is commonly used for measurement of the Z-shell parameters is not typical of the operating condition of a FET, and the source and drain resistances may be overestimated. This basic method (with variations of gate bias) is used by several workers, but the accuracy of the extraction of the extrinsic resistances (in particular) is often limited by simple assumptions about the physical system and associated mathematical description. For example, in pHEMTs,

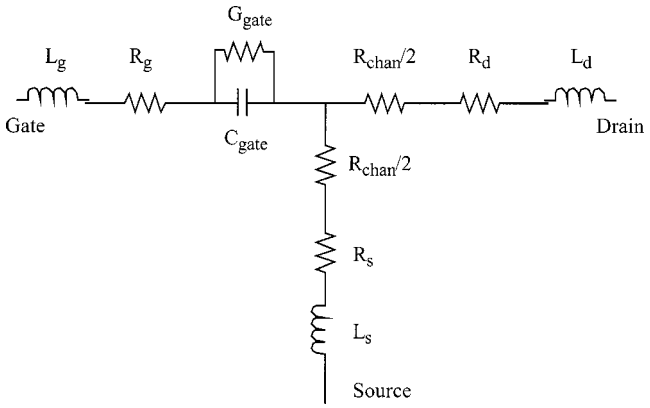

Fig. 4. Simplified FET equivalent circuit under the "cold FET" conditions of $V_{\rm gs}, V_{\rm ds} = (0, 0)$. The extrinsic $C_{\rm gs}$ and $C_{\rm ds}$ capacitances are neglected in the first approximation of the R-L component values.

the gate-to-channel contact is not a single Schottky barrier as in a MESFET but consists of a Schottky contact in series with an heterojunction. Thus, the extraction of gate resistance by assuming the constancy of the Schottky ideality factor with gate bias is inaccurate. An improved resistance extraction is necessary.

A new extraction method for the extrinsic Z-shell parameters was developed, based on optimizing the measured S-parameter data over frequency. The drain-source voltage is set to zero, again eliminating the influence of the controlled current source from the equivalent circuit, and the gate bias is set to 0 V. Under these conditions, the intrinsic circuit of the FET can be reduced to a simple T-network in which the gate branch contains a parallel resistance/capacitance combination representing the gate-to-channel contact, and the source and drain branches are half the channel resistance. This is shown in Fig. 4. The value of the channel resistance was estimated by using Agilent-EEsof's Advanced Physical Device Simulator to find the channel charge density at 0-V gate bias for the given device structures. This yields a much more accurate value of the channel resistance than has been previously estimated. Broadband S-parameter measurements were made. After deembedding the extrinsic capacitances, the branch impedance functions were fitted to the measured data using a rational function optimizer routine to determine the resistances and inductances. The complete extraction was accomplished in a two-pass process. In the first pass, *all* the extrinsic capacitance was subtracted from the measured data, and the optimizer produced initial values for R_x and $L_x(x = g, d, s)$. In the second pass, the deembedding process was carried out in accordance with the equivalent circuit in Fig. 2. First, the outer capacitance shell was subtracted from the measured data, followed by the initial values of inductance, and then the second capacitance shell. At this point the optimizer was run to yield new values of branch inductance and resistance. The new value of inductance was added to the initial value to provide the final extrinsic inductance value. Two passes were considered sufficient: the *delta* L and R values produced were generally small enough to be at the limit of our measurement accuracy, so further refinement was considered unnecessary. The gate resistance and inductance were fitted over a limited frequency range, from about 10 to 40 GHz, where the equivalent

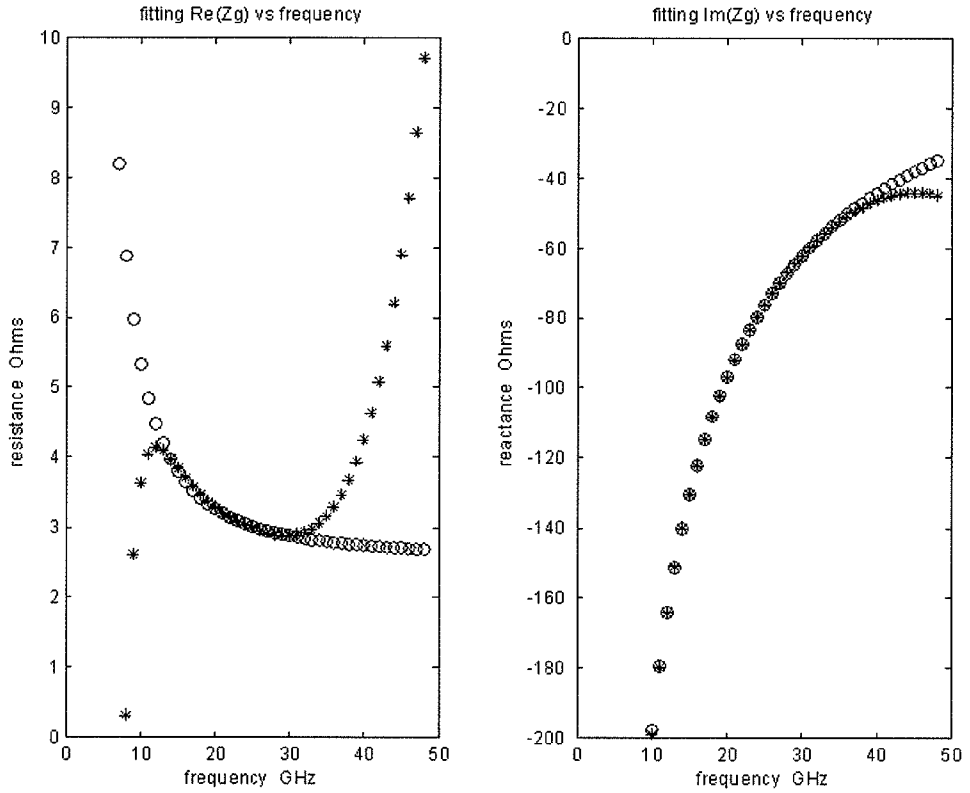

Fig. 5. Measured and optimized fit of the real and imaginary parts of the (R_g-L_g-$C_{\rm gate}//G_{\rm gate}$) gate branch impedance network in Fig. 4, with measured data (asterisks) and data fitted to the 10–40 GHz measurements (pen circles).

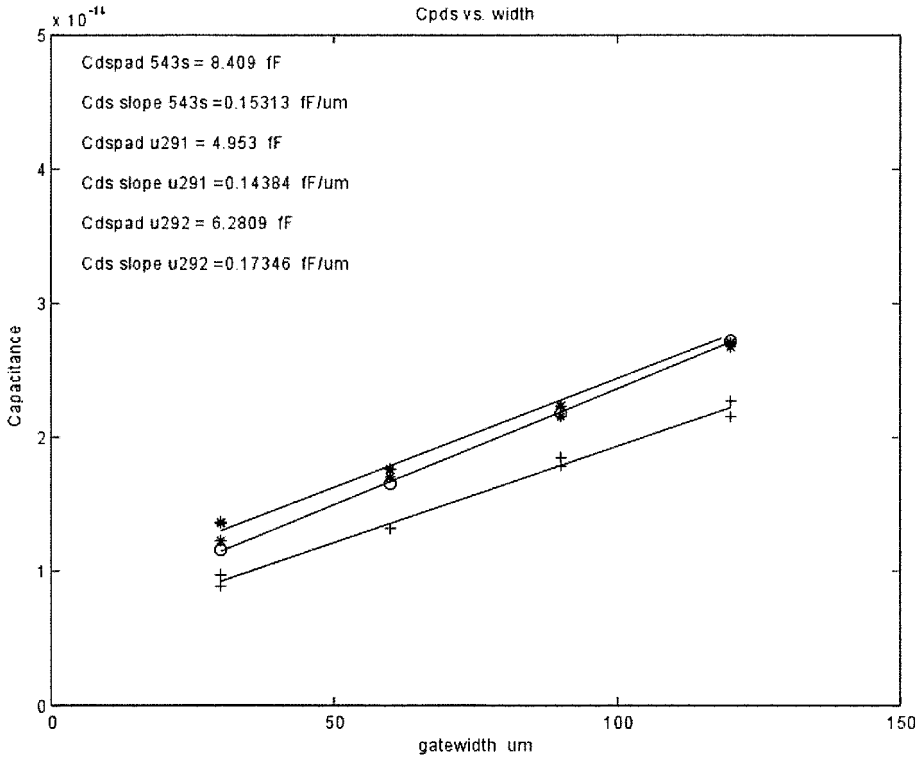

Fig. 6. Variation of extrinsic drain-source capacitance with total gate width, showing a linear relationship.

circuit of Fig. 4 is appropriate and the reactance can be accurately measured. An example of the fit of the real and imaginary parts of the gate branch impedance is shown in Fig. 5. The drain and source branches were modeled as simple series L-R networks, and the fitting process described here yielded excellent straight-line fits to the measured data. The contribution of

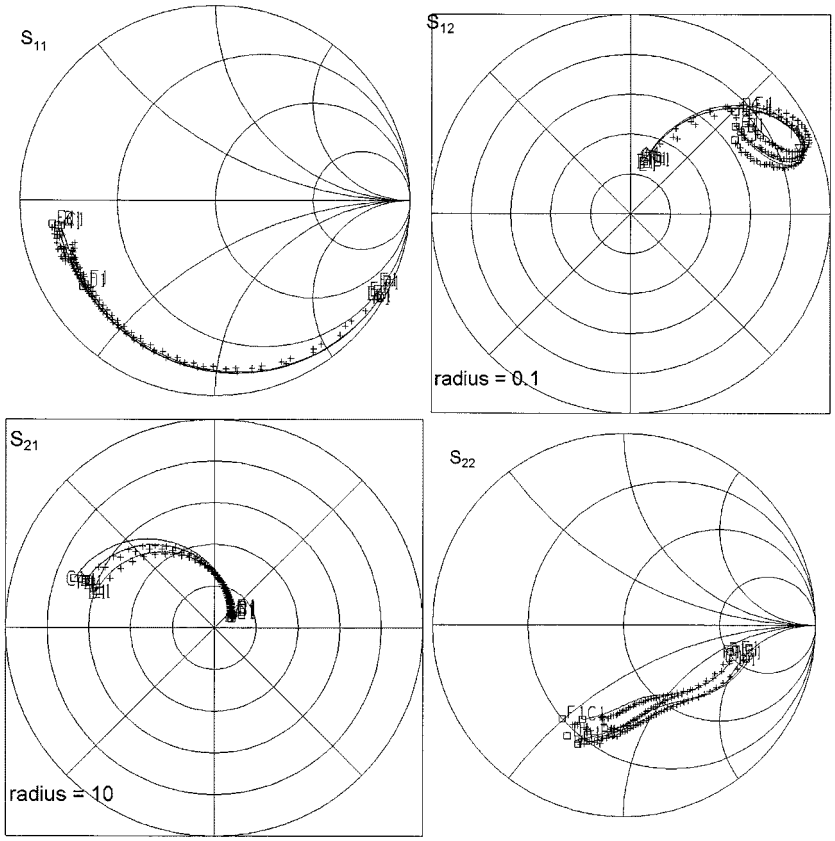

Fig. 7. Comparison of measured and modeled S-parameters for an 8 × 240 μm (number of gate fingers × unit gate width) 0.25-μm gate length pHEMT over the frequency range 2–48 GHz. Measured data from three different wafer lots ((+)) and model data (continuous line).

the vias to the extrinsic parameters is included in the source inductance and is readily identifiable.

V. Scaling Rules

The scaling rules for the extrinsic capacitances were determined by linear regression of the capacitance data obtained in cold FET pinched-off condition over the range of gate widths and number of fingers. In this bias condition, it is not possible to separate the gate-width dependence of the gate-source and gate-drain extrinsic capacitances, arising from the capacitance between the metal contacts, from the depletion capacitance of the gate itself: these extrinsics are contained within the $C_{\rm gs}$ and $C_{\rm gd}$ of the intrinsic model. The width dependence of the extrinsic drain-source capacitance is obtained from the slope of the extracted $C_{\rm ds}$ data: an example of these data is shown in Fig. 6. The manifold capacitances were found to consist of components that were fixed and dependent on the number of gate fingers.

The scaling rules for the resistive and inductive extrinsic components were similarly derived from the cold FET measurements at $(V_{\rm gs}, V_{\rm ds}) = (0, 0)$. For these extrinsic parameters, the scaling rules were not so straightforward as for the capacitances. The source and drain resistances vary inversely with gate width

$$R_{d,s} = \frac{\text{constant}}{\text{width}} \tag{1}$$

where the constant is given by the sheet resistivity of the channel material.

The gate resistance comprises two components: the first is of the usual form

$$R_g = \frac{R_{g0} \times \text{width}}{(\text{Number of gate fingers})^2} \tag{2}$$

and the second component is a contact resistance [21]

$$R_g = \frac{R_{g\rm Con}}{\text{width}} \tag{3}$$

where the constants are determined from fitting these functions to the measured data. The effect of the contact resistance component is noticeable for short unit gate widths of around 25 μm or less in our pHEMT processes.

The gate inductance scales in a similar manner to the first component of gate resistance: proportional to the unit gate width and inversely proportional to the number of parallel gate fingers

$$L_g = \frac{L_{g0} \times \text{width}}{(\text{Number of gate fingers})^2}. \tag{4}$$

The drain inductance scales linearly with unit gate width and inversely with number of parallel drain contacts. For our processes, this relationship with number of parallel drain fingers was found to be related to the inverse square root of the number of drain fingers

$$L_d \propto \frac{L_{g0} \times \left(\frac{\Delta\text{width}}{\Delta\text{fingers}}\right)}{\sqrt{(\text{Number of gate fingers})}} \tag{5}$$

where $L_{\rm d0}$ is the drain inductance scaling factor.

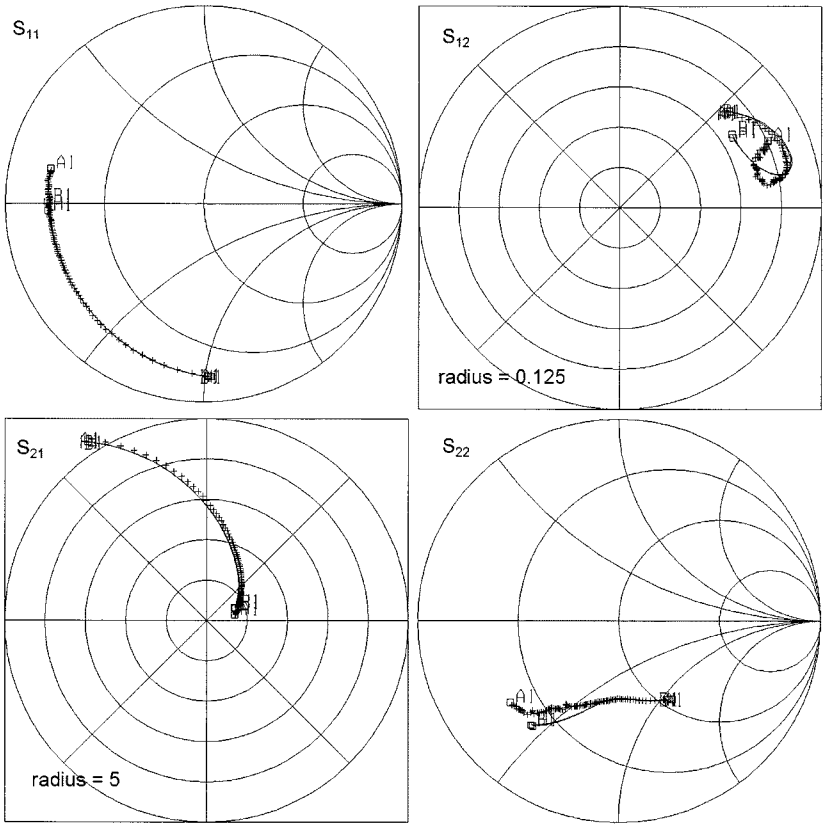

Fig. 8. Measured S-parameters for a 6 × 30 mm (number of gate fingers × unit gate width) 0.12-μm gate length pHEMT over the frequency range 10–100 GHz, compared with S-parameters derived from models taken from 6 × 30 μm and 4 × 50 μm devices, scaled to 6×30 μm.

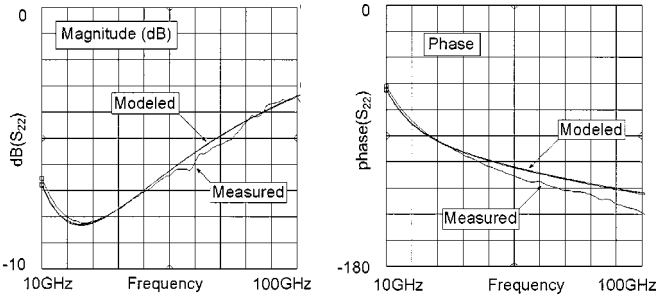

Fig. 9. Measured magnitude and phase of S_{22} for a 6×30 μm (number of gate fingers × unit gate width) 0.12 –μm gate length pHEMT, compared with S_{22} derived from models taken from 6 × 30 μm and 4 × 50 μm devices, scaled to 6 × 30 μm.

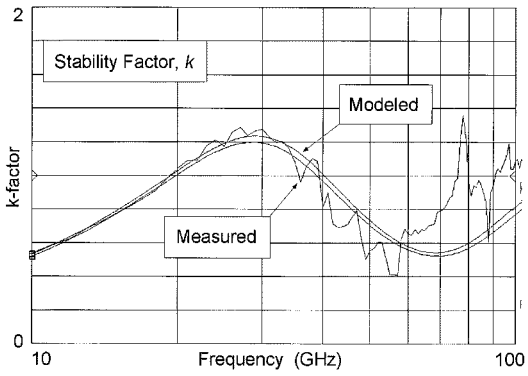

Fig. 10. Measured stability factor (k-factor) for a 10×60 μm (number of gate fingers × unit gate width) 0.25-μm gate length pHEMT, compared with k-factor derived from models taken from 6 × 75 μm and 8 × 30 μm devices, scaled to 10 × 60 μm.

The source inductance for our processes is due to the source bus bar connecting the individual source contacts, in series with the inductance of the back vias. The bus bar inductance is proportional to the length of the bus, essentially given by the number of gate fingers. For our processes, the contribution to L_s of the two vias is about 5.5 pH: this is obtained from extrapolation of the source inductance to zero gate fingers. This value was verified by a three-dimensional electromagnetic simulation of the FET metallization structure including the back side via contacts, using Agilent-EEsof HFSS. This simulation calculated the current flows in the metallization and along the via walls and determined the S-parameters of the structure from which a value of 6 pH for the two vias was calculated.

VI. Automated FET Model Generation and Verification

Once the extrinsic parameters are known, the linear model can be extracted from S-parameter data at a given frequency and bias condition. While this can be carried out manually for a small number of bias conditions, an automated process is required for generating the bias-dependent model. The existing in-house FET measurement control software [22] was adapted to include the new extrinsic parameter extraction measurement, and new deembedding and model extraction code was written to

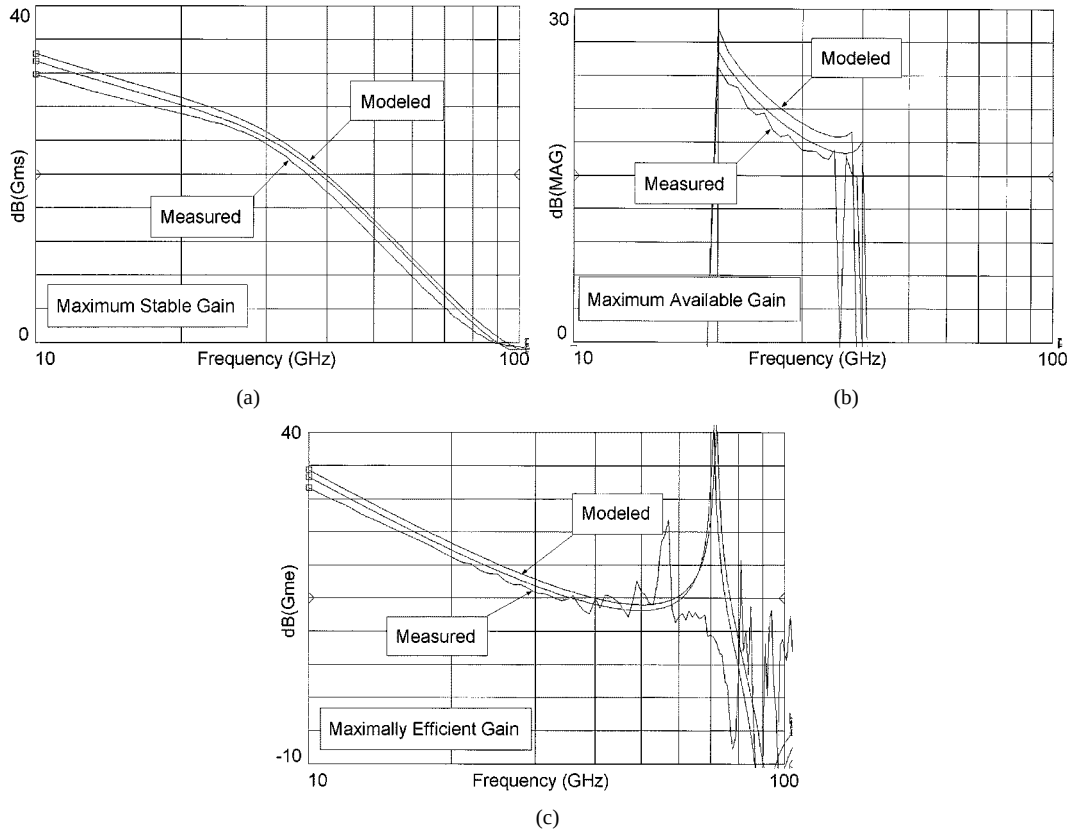

Fig. 11. Measured gains (MAG, MSG, maximally efficient gain) for a 10 × 60 μm (number of gate fingers × unit gate width) 0.25 –μm gate length pHEMT, compared with the gains derived from models taken from 6 × 75 μm and 8 × 30 μm devices, scaled to 10 × 60 μm.

generate the table-based data files. Because of the frequency-independence of the intrinsic model elements, only a single extraction frequency is necessary to obtain a broadband equivalent circuit model: the frequency used here is 16 GHz. This frequency is a good compromise for our devices, allowing the usual approximations to be made in the extraction equations [1] while retaining accurate measurement of the small capacitances found in millimeter-wave FETs. The equivalent circuit model has been realized as a parameterized subcircuit in MDS and Agilent-EEsof ADS circuit simulators.

Initial verification of the model is carried out by comparing model-generated broadband (∼1–50 GHz) S-parameter data with measured data on the same device, at several bias points. This verification is carried out for every data file generated. So far, we have produced 50 model data files for 0.35-μm MESFET and 0.25- and 0.12-μm pHEMT devices, in a range of device dimensions spanning 4 × 25 μm to 8 × 50 μm (number of gate fingers × unit gate width). Extremely close agreement between measured and modeled S-parameters has been demonstrated. This is illustrated in Fig. 7 for an 8 × 240 μm (number of gate fingers × unit gate width) 0.25-μm gate length pHEMT over the frequency range 2–48 GHz. These results are at bias conditions of $(V_{\rm gs}, V_{\rm ds}) = (-0.5\ {\rm V}, 5.0\ {\rm V})$, roughly in the center of the Class A operating regime. In particular, the S_{12} and S_{22} parameters are well modeled. In large devices, the manifold structure can produce a resonance in S_{12}: as can be seen, the locus of predicted S_{12} in the Smith chart follows the measured resonance characteristic very closely.

Further S-parameter measurements up to 110 GHz were made to determine the model accuracy in the higher millimeter-wave frequency regime. A resonance in the on-wafer calibration was observed at around 105 GHz, so for clarity, data above 100 GHz have been omitted from the following graphs. Measurements were made on a 6 × 30 μm, 0.12-μm gate length pHEMT biased at $V_{\rm gs} = 0.1$ V and $V_{\rm ds} = 3.0$ V. The measurements were compared with models taken from a 6 × 30 μm device and a 4 × 50 μm device scaled to 6 × 30 μm, from the same wafer as the measured device. The S-parameters are shown in Fig. 8, indicating close agreement between measured data and the models up to ∼100 GHz. The model data for the two models are virtually indistinguishable, indicating that the scaling rules are accurate. In many linear models, the output match is often poorly modeled at higher frequencies, a problem that is attributed to the location of the $C_{\rm ds}$ component in the equivalent circuit [14]. The magnitude and phase of the output match are presented in detail in Fig. 9 and show that for this equivalent circuit model, both the direct and scaled models are in excellent agreement with the measured data up to ∼100 GHz. The apparent phase error is about 14° at 100 GHz, which corresponds to a distance similar to the accuracy and repeatability of probe placement on our Agilent 8510XF probe station. In this model, S_{22} is shown to be modeled accurately by the combination of the carefully determined extrinsic and intrinsic contributions to $C_{\rm ds}$. This permits the accurate design of output matching networks for maximum power output in power amplifiers, for example.

In addition to the individual S-parameters, we have used derived parameters such as stability factor and power gains to highlight any interaction between the S-parameters. In Figs. 10 and 11, the k-factor and FET power gains are presented for a measured 10×60 μm 0.25-μm gate length pHEMT biased at $V_{\rm gs} = -0.5$ V, $V_{\rm ds} = 5.0$ V. These are compared with k-factors and gains derived from models taken from 8×30 μm and 6×75 μm devices, scaled to $10\times$ 60 μm, from the same wafer as the measured data. The measurements of these devices were made to 110 GHz, well above the f_τ for this FET process, which is nominally 55 GHz. The figures show extremely good agreement between the measured and the scaled, modeled data, at frequencies up to approximately f_τ, indicating that the S-parameters have been predicted very accurately in both magnitude and phase, and also that the derived scaling rules are valid. Above f_τ, the modeled behavior is very smooth, enabling accurate simulation at frequencies essentially beyond the fundamental frequency range of the device.

VII. Conclusions

We have developed a bias-dependent linear FET model with a new extrinsic topology and parameter extraction methodology. The model has been shown to predict S-parameters and their derived functions such as gain and stability factor accurately to frequencies up to 100 GHz. Scaling rules for the intrinsic and extrinsic equivalent circuit parameters have been determined, and the scaled S-parameters (etc.) are predicted accurately over a range of FET dimensions from four to 12 gate fingers and 100 to 1000 μm total gate width. Models have been extracted in a range of FET processes, including GaAs MESFET and pHEMT.

The same extrinsic shell and scaling rules can be applied to large-signal FET models. We have successfully extracted large-signal table-based (HPFET) models from the same S-parameter measurements used for the linear model, again showing good agreement between measured and modeled S-parameters, dc data, and large-signal figures of merit such as power-added efficiency, $P_{-1\rm dB}$, over the range of device geometries and frequencies.

The extrinsic element topology and element value extraction method are sufficiently general and can be applied successfully in the modeling of most three-terminal field-effect devices. Scaling rules need to be developed for any given FET device layout, using a sufficiently large array of device topologies as described here. The scaling rules are relatively simple to determine empirically. Accurate scaling rules for the extrinsic elements contribute significantly to the model accuracy at high frequencies.

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