

HP 8642A/B SYNTHESIZED SIGNAL GENERATOR (Including Options 001, 002 and 003)

Service Manual Volume 3 SERIAL NUMBERS

This manual applies directly to modules with serial numbers prefixed:

2427A to 2816A and all *MAJOR* changes that apply to your instrument/modules.

rev.01NOV88

For additional important information about serial numbers, refer to "INSTRUMENTS COVERED BY THIS MANUAL" in Section 1.

Second Edition

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Microfiche Operation and Calibration Manual HP Part 08642-90225

Operation and Calibration Manual HP Part 08642-90224

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A12 Module

Troubleshooting and Adjustments Contents

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Troubleshooting

A12 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A12 is the faulty module from Module Level Diagnostics (MLD) results.
- Open the HP 8642 manual to page 80-100. There are 3 diagrams of the A12 Module (Sum Loop). One diagram is titled Simplified Block Diagram. It is a block diagram intended to be used to understand the basic operation of A12. (There is a brief discussion of the modules circuit operation on page 80-3).
- Open the next foldout on page 80-101(BD12). There, you will see a more detailed Block Diagram of the Sum loop. **BD12 is meant to be used during Checks 1 through 4.** Notice there are three assemblies shown; A12A1, A12A2, and part of A12A3. The rest of A12A3 is a frequency divider circuit, and is shown on BD13 (page 80-103). **BD13 is meant to be used during Checks 5 and 6.** The A12 assemblies are represented on six Service Sheets, SS36-41.
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Tables in Component Level Repair Directory. Start with the tables that are labeled with a Service Sheet number (Example: **Table 12. SS36 DC Voltages**). Other tables are more general and are to be used at your discretion. It is suggested that you familiarize yourself with the contents of these tables so you can determine if they will be effective in solving your particular troubleshooting need.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustments and Auto Adjust Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No. 1	45 MHz, +0 dBm
Signal Generator No. 2	HP8642A/B
Oscilloscope	HP1980B
DVM	HP3456A
Power Meter	HP8902A
Spectrum Analyzer	HP8566A/B
HP 8642 Bench Service Kit	HP 11802A
Power Sensor	HP11722A
FET Probe	HP 1120A

Essentials of A12 Module Operation

Refer to the Simplified Block Diagram on page 80-100. The A12 Module contains a phase locked loop (SS38, SS36, SS37) which combines the IF Loop Output signal (from A9) with the Reference Loop Output signal (from A11) to produce the baseband frequencies of the HP 8642, from 528.75 MHz to 1057.5 MHz. The output of the phase locked loop is directed from A12A2 J3 to A12A3 J2. A12A3 contains Divide by 2^N (SS40, SS41) that divides the phase locked loop output (from BD 12) by a power's of 2, and outputs it on A12A3 J3. This is the output of the A12 Module, and is called Divider Output. The total output frequency range is 4.13 MHz to 1057.5 MHz.

CHECK 1: A12A3 ANALOG CIRCUITRY (SS38)

Essentials of SS38 Circuit Operation

Refer to BD12. Located on the A12A3 board is an input port for the IF Reference Loop Output (from the A9 module). It is A12A3 J6 (BD). There is also an input port for the Sum Loop IF, which is the main feedback signal in the Sum. It is A12A3 J5, (OS). These signals are amplified and sent to a mixer functioning as a **PHASE DETECTOR**. The **PHASE DETECTOR** outputs an error signal (at Z1 pins 3 and 4) which is filtered, then directed through **DIPLEXERS** and an **INTEGRATOR**. After being integrated, the error signal is buffered (in **LOOP EMITTER FOLLOWER**), shaped, and output to A12A1 as the Sum Loop Tune Voltage. If the loop is not phase locked, the integrator is forced to sweep in an attempt to achieve lock (sweep to lock). If switch A12A3 S1 is in its OPEN (open loop) position, the sweep to lock is discontinued and the integrator output is held at approximately half its maximum value.

NOTE

Use the Module Test Point/Adjustment Locations diagram on page 80-100 (the foldout opposite BD12) to locate test points on A12A1, A12A2, and A12A3. Test point designators (XX) will be used in text whenever applicable.

Description of Check 1

The largest board in the A12 module is the A12A3 Sum Loop Detector/Divider (see bottom board shown on Module Test Point/Adjustment Locations on page 80-100). This is a check of the A12A3 analog circuitry, and is intended to identify failures that would lead you to SS38 for component repair. In this check you first test the **POWER SUPPLY** for the A12 module. Then, you will substitute signals at the two RF inputs to the board, and verify the output waveform with the Oscilloscope to check for correct **PHASE DETECTOR** and **INTEGRATOR** operation. The **SHAPER** and four diagnostic sense points are also tested. If a test fails during Check 1, refer to Component Level Repair Directory.

Required Equipment:

Signal Generator No. 1*	45 MHz, +2.5 dBm
Signal Generator No. 2	HP8642A/B
Oscilloscope	HP1980B
DVM	HP3456A

* The IF Loop Output on W30 can be used if the A9 module is known to be good.

Test the A12 Power Supplies

1. Setup:

Switch the HP 8642 to standby (STBY).

Extend A12 module on extender posts (refer to paragraph 8-4 in Disassembly Procedure).

Remove the A12A3 cover (See the Assembly Locator on page 80-100).

Switch the HP 8642 on.

2. Measure Voltage Levels:

Use the DVM to measure the **POWER SUPPLY AND GND** lines at the filters given in Table 80-1. (FL locations can be found in the Component Locator diagram on page 80-108, and measurements can be made on either side of filter.)

Table 80-1. A12 Power Supply Lines

Filter	Nominal Voltage
A12A3 FL6	+50V
A12A3 FL7	+15V
A12A3 FL8	-5V
A12A3 FL9	+5V
A12A3 FL10	-5V
A12A3 FL11	+5V
A12A3 L112	-5V

Test the SS38 Diagnostic Circuitry**3. Setup:**

Switch the HP 8642 to standby.

Disconnect A12 W3 from A12A3 J5.

Ensure that A12A3 S1 is in the CLSD position.

Connect an Oscilloscope probe to A12A3 TP4 (Located at top of A12A3 board next to J1).

Turn on the HP 8642.

4. Verify Waveforms at Diagnostic Sense Points:

Key in **[SHIFT] [SPCL] [325] [Hz]** to enter Service Mode and internal voltage measurements. Then key in the Service Functions from Table 80-2 and compare the waveform on the oscilloscope to the figure listed for each service function. Disregard the HP 8642 front panel display during this check. Internal voltages are measured using service special functions for the purpose of switching the desired A12 sense line to A12A3 TP4.

NOTE

*The Diagnostic Sense Points are measured at A12A3 TP4 (the output of the **SUM LOOP DIAGNOSTICS** on SS39) for convenience. If the signal doesn't match the figure, observe the SS38 signal source. (refer to Table 80-2). This will determine whether the failure is on SS39 or SS38.*

Table 80-2. Diagnostic Sense Points

Service Function	Figure	Line Label	SS38 Signal Source
[2] [2] [Hz]	80-1	Integrator Output Sense [DW]	A12A3 U18 pin 8
[2] [4] [Hz]	80-2	Comparator Output Sense [DV]	A12A3 U18 pin 1
[1] [9] [Hz]	80-3	Out-of-Lock Sense [DY]	A12A3 S1 pin 5

Test the Phase Detector and Integrator

5. Setup:

Switch the HP 8642 to standby.

Set Signal Generator 1 to 45 MHz and 0 dBm. (The A9 IF LOOP OUTPUT on W30 can be used if A9 is known to be good. If so, set the HP 8642 frequency to 607.5 MHz, and disregard the next setup step.)

If Signal Generator 1 is an external HP 8642, disconnect W30 from A12A3 J6 (BD), and connect Signal Generator #1's output to A12A3 J6 (BD).

Set Signal Generator 2 to 45.1 MHz and +5 dBm.

Connect Signal Generator No. 2's output to A12A3 J5 (DS).

Lock the timebases of Signal Generator No. 1 and Signal Generator No. 2 together.

Disconnect A12W4 from A12A1 J1 (DO) and connect A12W4 to the Oscilloscope input.

6. Verify Waveforms:

Switch the HP 8642 ON.

Adjust the scope (DC coupled) so that the display appears similar to the Sweep-to-Lock Signal shown in Figure 80-4. The amplitude should be 3 to 9 V_{pp}.

Adjust the scope (DC coupled) so that the display appears similar to Figure 80-5. This is a 100 kHz beat note superimposed on the Sweep-to-Lock Signal. The amplitude should be 0.5 to 1.5 V_{pp}.

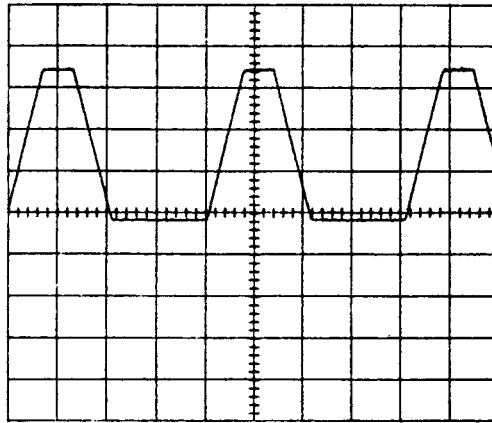


Figure 80-1. Integrator Output Sense Signal
(4.0V/DIV 1 mS/DIV)

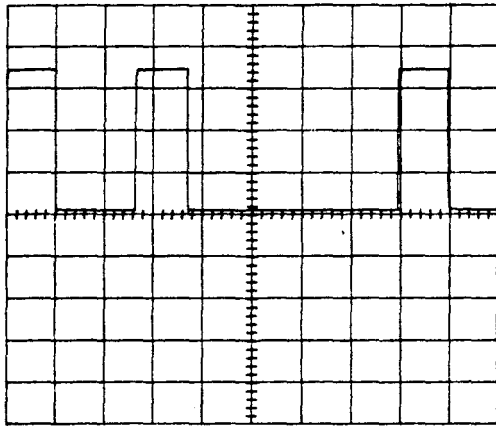


Figure 80-2. Comparator Output Sense Signal (1.5V/DIV 500 μ S/DIV)

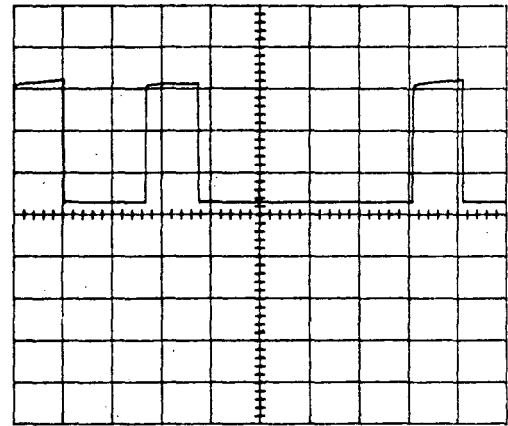


Figure 80-3. Out-of-Lock Sense Signal (1.5V/DIV 500 μ S/DIV)

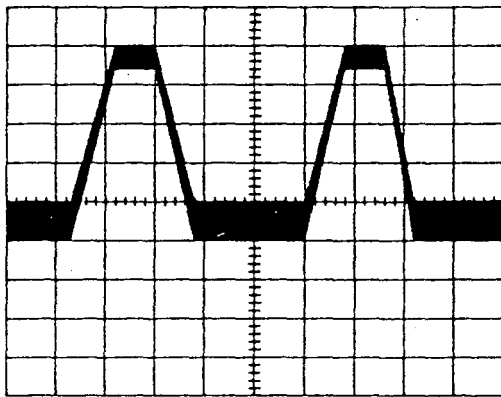


Figure 80-4. Integrator Sweep-to-Lock Signal (3-9 Vpp and \approx 4.0 mS period)

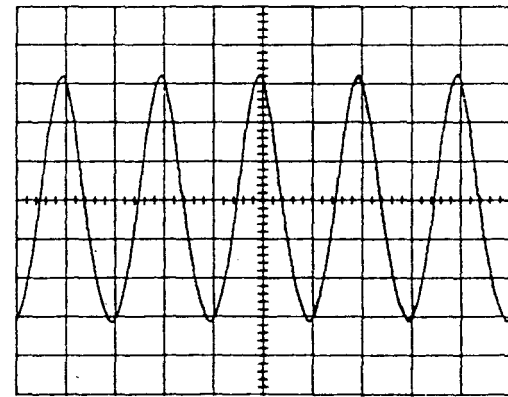


Figure 80-5. 100 kHz Beat Note Signal (0.5 to 1.5 Vpp and 10 μ S period)

Test the Shaper DAC**7. Setup:**

Remove Signal Generator No. 2 from A12A3J5 **DS** . Leave A12W3 disconnected.

Set A12A3 to open loop (OPEN) position. This halts sweep-to-lock action.

8. Measure Voltage at input lines:

Enter **SHIFT SPCL 3** to enter Service Mode. Then key in each Service Function in Table 8O-3. Verify correct TTL levels at the A12A3 U4 pins **DX** indicated in Table 8O-3.

Table 8O-3. Shaper DAC Input Lines

Service Function	DVM Measurement at A12A3 U4 Pin #					
	5(SB0)	1(SB1)	11(SB2)	13(SB3)	9(SB4)	3(SB5)
6 3 4 0 HZ (All Off)	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 4 1 HZ	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 4 2 HZ	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 4 4 HZ	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc
6 3 4 8 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc	≈0 Vdc
6 3 4 16 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc	≈0 Vdc
6 3 4 32 HZ	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈0 Vdc	≈5 Vdc
6 3 4 63 HZ (All On)	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc	≈5 Vdc

9. Measure Voltage Levels at Output Lines:

Disconnect A12W4 from Oscilloscope input. Connect A12W4 to DVM input.

Ensure A3S1 is in it's OPEN position.

Key in **SHIFT SPCL 3** to enter Service Mode. Key in the Service Functions from Table 8O-4. Record the DVM measurement for each Service Function in Table 8O-4 in the column labeled "DVM measurement at A12W4." Determine the actual results as indicated in the "Actual" column.

Table 80-4. Shaper DAC Output Lines

Service Function	DVM Measurement A12W4	LIMITS		
		Min.	Actual	Max
6 3 4 0 HZ	A = _____	0.8 Vdc	A = _____	1.0 Vdc
6 3 4 1 HZ	B = _____	10 mVdc	B - A = _____	15 mVdc
6 3 4 2 HZ	C = _____	10 mVdc	C - B = _____	15 mVdc
6 3 4 4 HZ	D = _____	17 mVdc	D - C = _____	37 mVdc
6 3 4 8 HZ	E = _____	43 mVdc	E - D = _____	72 mVdc
6 3 4 16 HZ	F = _____	110 mVdc	F - E = _____	150 mVdc
6 3 4 32 HZ	G = _____	275 mVdc	G - F = _____	425 mVdc
6 3 4 63 HZ	H = _____	5.2 Vdc	H = _____	5.7 Vdc

Restore Module

10. Reconnect A12 W4 to A12A1 J1
11. Reconnect W30 to A12A3 J6.
12. Reconnect A12 W3 to A12A3 J5.
13. Set A3S1 to it's close position.

CHECK 2: A12A3 CONTROL CIRCUITRY (SS39)

Essentials of SS39 Circuit Operation

Refer to BD12. Serial data comes from the microprocessor to the Sum Loop Module and is received at J1 pins 16 and 18. Data is converted to a parallel bus in **SERIAL DATA INTERFACE** and sent to other functional blocks. The functional blocks labeled **OSCILLATOR BAND SELECT**, **SUM LOOP DIAGNOSTICS**, and **PRETUNE** perform control functions.

Description of Check 2

This check tests the control circuitry for the A12 module (Service Sheet 39). The A12 control circuitry is located on A12A3.

You will use the DVM to verify the output level of the **PRETUNE** DAC as different bit numbers are input. Then, you will calculate the output level change from service function to service function. If a test fails during Check 2, refer to Component Level Repair Directory.

Required Equipment:

OscilloscopeHP1980B
DVMHP3456A

Test the Serial Data Interface

1. Setup:

Switch the HP 8642 to standby (STBY).

Extend A12 module on extender posts (refer to Disassembly Procedures if you are not familiar with module extension).

Remove the A12A3 cover (see the assembly locator on the foldout opposite BD12 for location of A12A3 cover).

Switch the HP 8642 ON.

2. Measure TTL levels:

Key in Service Function 1 (SF1), use the Oscilloscope to verify TTL levels listed in Table 8O-5 in the column labeled SF1. Then key in Service Function (SF2), verify TTL levels listed in Table 8O-5 in the column labeled SF2.

SF1 = SHIFT SPCL 360611184810 HZ

SF2 = SHIFT SPCL 36065592405 Hz

Table 80-5. REF Loop Control Lines

Line label	A12A3 REF.Des.	Bit No.	TTL Levels*	
			SF1	SF2
N/A	U15 pin 6	0	L	H
N/A	U15 pin 9	1	H	L
NC	U15 pin 12	2	L	H
NC	U15 pin 5	3	H	L
NC	U15 pin 16	4	L	H
SEL 2	U15 pin 2	5	H	L
SEL 1	U15 pin 19	6	L	H
SEL 0	U15 pin 15	7	H	L
VCO 4	U2 pin 12	8	L	H
VCO 3	U2 pin 6	9	H	L
VCO 2	U2 pin 9	10	L	H
VCO 1	U2 pin 5	11	H	L
PT 5	U2 pin 15	12	L	H
PT 4	U2 pin 2	13	H	L
PT 3	U2 pin 19	14	L	H
PT 2	U2 pin 16	15	H	L
PT 1	U5 pin 15	16	L	H
PT 0	U5 pin 6	17	H	L
SB 5	U5 pin 16	18	L	H
SB 4	U5 pin 9	19	H	L
SB 3	U5 pin 5	20	L	H
SB 2	U5 pin 2	21	H	L
SB 1	U5 pin 19	22	L	H
SB 0	U5 pin 12	23	H	L
* TTL High (H) = 2.0 to 5.0 VDC TTL Low (L) = 0.0 to 0.8 VDC				

Test the Pretune DAC**3. Setup:**

Connect the DVM to A12A3 TP4 (Located at the top of the A12A3 board next to ribbon connector J1).

4. Measure Voltage Levels at Pretune DAC output:

Key in: **SHIFT** **SPCL** **3** **2** **2** **1** **Hz** to enable measurement of the PRETUNE SENSE at A12A3 TP4.

Key in **SHIFT** **SPCL** **3** to enter Service Mode. Then key in the Service Functions from Table 80-6. Record the DVM reading for each Service function in the column labeled "DVM Measurements A12A3 TP4". Determine and record the actual results as indicated in the "Actual" column.

NOTE

The Pretune DAC output is prescaled before being multiplexed by U10 (at pin 6). To Calculate the actual output of the DAC (at A12A1 TP5), multiply the measurement at A12A3 TP4 by 3.874.

Table 80-6. Pretune DAC

Service Function	DVM Measurement A12A3 TP4	LIMITS		
		Min.	Actual	Max.
6 3 3 0 HZ	A = _____	2.0 Vdc	A = _____	2.5 Vdc
6 3 3 1 HZ	B = _____	75 mVdc	B - A = _____	100 mVdc
6 3 3 2 HZ	C = _____	75 mVdc	C - B = _____	100 mVdc
6 3 3 4 HZ	D = _____	150 mVdc	D - C = _____	200 mVdc
6 3 3 8 HZ	E = _____	325 mVdc	E - D = _____	425 mVdc
6 3 3 1 6 HZ	F = _____	700 mVdc	F - E = _____	950 mVdc
6 3 3 3 2 HZ	G = _____	1.8 Vdc	G - F = _____	2.35 Vdc
6 3 3 6 3 HZ	H = _____	12.5 Vdc	H = _____	13.5 Vdc

Test the Oscillator Band Select Lines

5. Setup:

Remove DVM from A12A3 TP4.

6. Measure Voltage Levels:

Set the HP 8642 to each frequency shown in Table 80-6, and verify with the DVM that the voltages are correct at each A12A3J7 pin listed for each front panel setting.

Table 80-7. Oscillator Band Select Lines Measurements

HP 8642 Frequency Setting	A12A3J7 Pin 5 (Band 1)	A12A3J7 Pin 7 (Band 2)	A12A3J7 Pin 6 (Band 3)	A12A3J7 Pin 8 (Band 4)
560 MHz	0	+15	+15	+15
690 MHz	+15	0	+15	+15
830 MHz	+15	+15	0	+15
960 MHz	+15	+15	+15	0

Restore Module

- Set A12A3 S1 to CLSD (closed loop) position (unless proceeding to Check 3).
- Replace A12A1/A12A2 cover (unless proceeding to Check 3).

CHECK 3: A12A1 VCO BOARD (SS36)

Essentials of SS36 Circuit Operation

Refer to BD12. Each of the four VCOs are electronically tunable. Their combined frequency range covers the baseband frequency range of the HP 8642, which is 528.75 MHz to 1057.5 MHz. (The separate VCO frequency ranges are shown in Table 80-8.

There is a functional block called **VCO SWITCH DRIVE** that enables the selected VCO. The **PRETUNE** block filters a voltage from the Pretune DAC (SS39 **DM**), that pretunes the selected VCO to the correct frequency). The **BUFFER**, buffers the tune voltage that phase locks the selected VCO. The Sum Loop VCO Output frequencies are locked to the mixing products (sum and difference) of the IF Loop Output and the Reference Loop Output (SS38).

Description of Check 3

The smallest board in the A12 module is A12A1 (see top board on Module Test Point/Adjustment Locations on page 80-100). This check is a verification that the four Voltage Controlled Oscillators on A12A1 are at the correct frequency and power levels for the front panel settings given in Table 80-8. The Power Splitter adapter allows you to observe the output of the VCOs while the instrument is being cycled through different frequencies. If a test fails during Check 3, refer to SS36 Component Level Repair Directory.

Required Equipment:

Spectrum Analyzer	HP8566A/B
HP 8642 Bench Service Kit	HP 11802A
Power Splitter Adapter	HP 08642-60079

Test the VCOs

1. Setup:

Switch the HP 8642 to standby.

Remove Power Splitter A12A2 Z2. (If the A12A1/A12A2 cover is not removed, use needle nose pliers to remove (by pulling) Z2 through the access hole labeled Z2).

Install Power Splitter Adapter (HP 08642-60079) in place of Z2. (The notch in the adapter should face the front of HP 8642).

Connect Pin 1 of the adapter to the input of the Spectrum Analyzer.

Set A12A1 S1 to its open (open loop) position.

Remove A12 W3 from A12A3 J5.

Turn on the HP 8642.

2. Measure Power Levels:

Set the HP 8642 to sweep between the front panel frequencies shown in Table 80-8, and compare the measured power levels with the Table 80-8 values listed.

To set the HP 8642 to sweep, key in: **START FREQ** **XX MHz**, **STOP FREQ** **XX MHz**, **SHIFT** **START FREQ** (TIME) **5** **MHz** (seconds). Pressing MHz should enter 5 seconds as the sweep time. This slower sweep time is necessary in order to see power levels at each VCO frequency with loop shaping occurring (every 2.5 MHz).

Table 80–8. VCO Frequency Select Table

HP 8642 Sweep Range	VCO Band	VCO Power
528.750001 to 652.5 MHz	1	≥5 dBm
652.50001 to 787.5 MHz	2	≥5 dBm
787.50001 to 922.5 MHz	3	≥5 dBm
922.50001 to 1057.5 MHz	4	≥5 dBm

Restore Module

3. Switch the HP 8642 to Standby.
4. Return S1 to its CLSD (closed loop) position.
5. Reconnect A12W3 to A12A3 J5.
6. Replace A12A2 Z2.

CHECK 4: A12A2 BOARD (SS37)

Essentials of SS37 Circuit Operation

Refer to BD12. The A12A1 Sum Loop VCO's output is connected to the A12A2 **SUM LOOP POWER SPLITTER ASSEMBLY** by semi-rigid coax cable, from A12A1 J3 (DQ) to A12A2 J4 (DQ). On the A12A2 Assembly the **Sum Loop VCO's** output is input to the Power Splitter. One output from the Power Splitter drives the **Output Limiter/Amplifier**, which supplies the A12 module's main octave output (528.75 to 1057.5 MHz) to the A12A3 Divider circuitry (BD13 (DR)).

The other output from the Power Splitter drives the **LO Limiter/Amplifier**. This amplifier supplies **LO** drive for the **SUM LOOP MIXER**.

The **SUM LOOP MIXER** mixes the **SUM LOOP OUTPUT (LO LIMITER/AMPLIFIER)** with the A11 Reference Loop Output (A12A2 J2 (DK)) through the 9 dB Attenuator. The output from the **SUM LOOP MIXER** is the **SUM LOOP IF**. This is low pass filtered in the **IF FILTER**, amplified and impedance transformed in the **IF AMPLIFIER**, and again low pass filtered in the **IF OUTPUT FILTER**. The **SUM LOOP IF** is phase locked to the IF Reference Loop output (45 to 90 MHz) on SS38.

Description of Check 4

The A12A2 assembly (see middle board on Module Test Point/Adjustment Locations, page 80-100) is the board next to A12A1. The output of A12A2 at A12A2 J3 (DR), is tested for correct **POWER SPLITTER** operation. Then, the output of the feedback path (Sum Loop IF) is tested to verify correct **POWER SPLITTER** and **SUM LOOP MIXER** operation. If a test fails during Check 4, refer to Component Level Repair Directory.

Required Equipment:

Spectrum Analyzer HP8566A/B

NOTE

The A11 Reference Module must be known good for this check. If it is not, a signal generator can be substituted at A12A2 J2 at A11 frequencies listed, amplitude + 4 dbm.

Test the A12A2 Sum Loop Output Level Accuracy

1. Setup:

Switch the HP 8642 to Standby.

Remove A12W2 from SUM LOOP/DIVIDER MODULE connector A12A3 J2 (see instrument top cover) and connect the Spectrum Analyzer to A12 W2.

Disconnect A12 W3 from A12A3 J5 (DS).

Switch A12A3 S1 to it's open loop position.

Turn on the HP 8642.

2. Measure Power Levels:

On the HP 8642 key in **START FREQ** **528.75 MHz**, **STOP FREQ** **1057.25 MHz** **SHIFT** **START FREQ** (TIME) **10** **MHz** (seconds). This sets the HP 8642 to sweep between 528.75 MHz and 1057.25 MHz with a 10 second sweep time.

The signal level on the Spectrum Analyzer should be between 3 and 9 dBm, from 528 MHz to 1057 MHz.

Reconnect A12 W2 to A12A3 J2 (DR).

Test the A12 Sum Loop IF

3. Setup:

Connect the Spectrum Analyzer to the loose end of A12 W3.

4. Measure Power Levels and Frequency:

Set the HP 8642 RF frequencies to the values given in Table 80-9 and compare the Spectrum Analyzer frequency and power measurements with the values in Table 80-9.

Table 80-9. Sum Loop IF Path Check (SS37)

HP 8642 Frequency	A11 Ref. Freq. At A12A2J2	Results	
		A12A2J1 Frequency*	A12A2J1 Level
528.76 MHz	607.5 MHz	78.74* MHz	3 dBm to 9 dBm
562.40 MHz	607.5 MHz	45.10* MHz	3 dBm to 9 dBm
562.60 MHz	652.5 MHz	89.90* MHz	3 dBm to 9 dBm
607.40 MHz	652.5 MHz	45.10* MHz	3 dBm to 9 dBm
607.60 MHz	697.5 MHz	89.90* MHz	3 dBm to 9 dBm
652.4 MHz	697.5 MHz	45.10* MHz	3 dBm to 9 dBm
787.6 MHz	877.5 MHz	89.90* MHz	3 dBm to 9 dBm
832.4 MHz	877.5 MHz	45.10* MHz	3 dBm to 9 dBm
862.6 MHz	922.5 MHz	89.90* MHz	3 dBm to 9 dBm
877.4 MHz	922.5 MHz	45.10* MHz	3 dBm to 9 dBm
877.6 MHz	967.5 MHz	89.90* MHz	3 dBm to 9 dBm
922.4 MHz	967.5 MHz	45.10* MHz	3 dBm to 9 dBm
1057.49 MHz	967.5 MHz	89.99* MHz	3 dBm to 9 dBm
* These are approximate frequencies, due to the loop being unlocked.			

Restore Module

5. Reconnect A12W2 to A1A3J2.
6. Reconnect A12W3 to A12A3J3.
7. Replace A12A2 cover if removed.
8. Set A12A3 S1 to it's CLOSED position.

CHECK 5: A12A3 DIVIDER CIRCUITRY(SS40)

Essentials of SS40 Circuit Operation

Refer to BD13. The SUM LOOP OUTPUT is routed from the A12A2 board to A12A3 J2 through A12 W2, (the short RF cable). This signal is split at the **INPUT LIMITER**. If the signal is to be divided, it is directed to the dividers on SS41. If not, it is directed to $2N = 0$ **DIVIDE**, then buffered and output. There are two blocks of circuitry called **N=1 TO 4 SELECT GATES** and **N=5 TO 7 SELECT GATES**. Each block has an input line from the dividers on SS41 (RF÷2 TO 16) or (RF÷32 TO 128). The number (N) represents the power of 2 that the Sum Loop Output is being divided by. Either one of these two blocks of circuitry is selected by the **CONTROL LOGIC** on SS41, depending on the divide number (N = 1 TO 4) or (N = 5 TO 7). The output of either block labeled **SELECT GATES** is output through the single pole double throw **OUTPUT PATH SWITCH**. The output signal path is also controlled by **CONTROL LOGIC**.

Description of Check 5

The Sum Loop Output (A12A3 J2) is tested first for the correct frequency and power level. Then, the Divider Output (A12A3 J3) is tested to verify the correct frequency and power level in all the divide bands.

NOTE

*If check 5 passes, then check 6 is good and you do not need to perform it.
If test 5 fails perform test 6 to determine if the failure is on SS40 or SS41.*

Test the Sum Loop Output

1. Setup:

Disconnect A12 W2 from A12A3 J2 **DR** .

Connect A12 W2 to the Spectrum Analyzer input.

Key in 640 MHz and 0 dBm on the HP 8642 front panel.

2. Measure Power Level and Frequency:

Verify that the power level is +3 to +9 dBm at 640 MHz.

Reconnect A12W2 to A12A3 J2.

Test the Divider Output

3. Setup:

Disconnect W32 from A13A2 J6.

Connect W32 to the Spectrum Analyzer input.

4. Measure Frequency and Power Levels:

Verify frequency power levels for each HP 8642 front panel frequency Table 80-10.

Table 80-10. Divider Outputs

HP 8642 Front Panel Frequency	Divide by 2N	Divide Band	Frequency at W32	Power Level at W32
640 MHz	0	1	640 MHz	0 to 6 dBm
320 MHz	1	2	320 MHz	0 to 6 dBm
160 MHz	2	4	160 MHz	0 to 6 dBm
80 MHz	3	8	80 MHz	0 to 6 dBm
40 MHz	4	16	40 MHz	0 to 6 dBm
20 MHz	5	32	20 MHz	0 to 6 dBm
10 MHz	6	64	10 MHz	0 to 6 dBm
2 MHz	7	128	5 MHz	0 to 6 dBm

Restore Module

5. Reconnect W32 to A13A2 J6.

CHECK 6: A12A3 DIVIDER CIRCUITRY(SS 41)**Essentials of SS41 Circuit Operation**

Refer to BD13. The block of circuitry labeled $2^N = 1$ to 7 **DIVIDERS** divides the RF signal from the SUM LOOP OUTPUT (BD12) by a power of 2. The divided RF signal is output from $2^N = 1$ to 7 **DIVIDERS** on one of two lines, depending on the divide number. The block of circuitry labeled **CONTROL LOGIC** determines which dividers are enabled. The input lines to **CONTROL LOGIC**, (DIV 0, 1, 2), come on to the A12A3 board at J1 pins 20, 22, and 24. (These three lines come from the instruments microprocessor). The output lines from **CONTROL LOGIC** include the "enable" lines that enable the dividers, and "select" lines that select RF signal path gates and a switch. (Gates and switches are shown on SS40 and discussed in Check 5).

Description of Check 6

This check tests the control circuitry on SS41 along with the $2^N = 1$ to 7 **DIVIDERS**. Tables provided in this test give you HP 8642 front panel settings that allow you to assume control over circuitry normally controlled by the instruments microprocessor and firmware routines. Correct voltage levels are verified throughout their operating ranges with the DVM. In Table 80-11, the Spectrum Analyzer is used to check for correct divider operation. If a test fails in Check 5, refer to Component Level Repair Information.

Required Equipment:

DVMHP3456A
 Spectrum Analyzer HP8566A/B
 HP 8642 Bench Service Kit HP 11802A
 FET Probe HP 1120

Test the Control Logic Inputs

1. Measure Voltage Levels:

Key in the HP 8642 front panel frequency setting from Table 80-11 and verify correct DVM measurements at A12A3 FL3, 4, and 5 , .

Table 80-11. Divider Control Logic Inputs

HP 8642 Frequency	FL5 (DIV 0) <input type="text" value="EK"/>	FL4 (DIV 1) <input type="text" value="EK"/>	FL3 (DIV 2) <input type="text" value="RR"/>
640 MHz	≈0 Vdc	≈0 Vdc	≈0 Vdc
320 MHz	≈5 Vdc	≈0 Vdc	≈0 Vdc
160 MHz	≈0 Vdc	≈5 Vdc	≈0 Vdc
40 MHz	≈0 Vdc	≈0 Vdc	≈5 Vdc

Test the Select Lines

2. Measure Voltage Levels:

Key in the HP 8642 front panel frequency settings from Table 8N-12 and verify correct DVM measurements at A12A3 U103, U108, and U110 pin number listed.

Table 80-12. Select line

HP 8642 Front Panel Frequency	N=0 U103 Pin10 (ED)	N=1 U103 Pin6 (EF)	N=2 U108 Pin2 (EF)	N=3 U108 Pin1 (EF)	N=4 U108 Pin15 (EF)	N=5 U110 Pin4 (EH)	N=6 U110 Pin12 (EH)
640 MHz ÷1	≈0V	≈5V	≈0V	≈0V	≈0V	≈0V	≈0V
320 MHz ÷2	≈5V	≈0V	≈0V	≈0V	≈0V	≈0V	≈0V
160 MHz ÷4	≈5V	≈5V	≈2V	≈0V	≈0V	≈0V	≈0V
80 MHz ÷8	≈5V	≈5V	≈0V	≈2V	≈0V	≈0V	≈0V
40 MHz ÷16	≈5V	≈5V	≈0V	≈0V	≈2V	≈0V	≈0V
20 MHz ÷32	≈5V	≈5V	≈0V	≈0V	≈0V	≈5V	≈0V
10 MHz ÷64	≈5V	≈5V	≈0V	≈0V	≈0V	≈0V	≈5V
5 MHz ÷128	≈5V	≈5V	≈0V	≈0V	≈0V	≈0V	≈0V

Test the RF Path Select Lines

Key in the HP 8642 front panel frequency settings from Table 80-13, and verify correct DVM measurements at the U103 test points given.

Table 80-13. RF Path Select

HP 8642 Front Panel Frequency	DVM	
	U103 Pin 12 (E1)	U103 Pin 8 (E1)
640 MHz	5V	≈0 Vdc
20 MHz	0V	≈1 Vdc

Test the Divider Input

3. Setup:

Set the HP 8642 frequency to 640 MHz, and set the amplitude to 0 dBm.

Using the RF Test Probe (HP 1250-1598) from the Bench Service Kit, connect the Spectrum Analyzer to U106 Pin 4 (EE).

4. Measure Power Level and Frequency:

The signal at U106 pin 4 should measure 0 dBm at 640 MHz.

Test the $2^N = 1$ to 7 Dividers Outputs

5. Setup:

Set the HP 8642 frequency to 640 MHz, and set the amplitude to 0 dBm.

6. Measure Divider Frequency and Power Levels:

Key in the HP 8642 Front Panel Frequency settings from Table 80-14 and use the Fet Probe to verify the divider outputs at the divider pin numbers listed. Output level from all dividers should be between -5 dBm to +10 dBm.

Table 80-14. Divider Check *

HP 8642 Front Panel Frequency	U106 Pin10 ED	U113 Pin2 EF	U114 Pin2 EF	U115 Pin1 EF	U117 Pin15 EF	U117 Pin9 EH	U118 Pin9 EH
320 MHz ÷2	320 MHz	—	—	—	—	—	—
160 MHz ÷4	320 MHz	—	—	—	—	—	—
80 MHz ÷8	300 MHz	160 MHz	80 MHz	—	—	—	—
40 MHz ÷16	320 MHz	160 MHz	80 MHz	40 MHz	—	—	—
20 MHz ÷32	320 MHz	160 MHz	80 MHz	40 MHz	20 MHz	—	—
10 MHz ÷64	320 MHz	160 MHz	80 MHz	40 MHz	20 MHz	10 MHz	—
5 MHz ÷128	320 MHz	160 MHz	80 MHz	40 MHz	20 MHz	10 MHz	5 MHz
* Check each dividers output using an active probe, output level should be -5 to +10 dbm							

Restore Module

7. Replace the A12A3 cover.
8. Reconnect all cables.

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

- * Special function codes relevant to the module.
- * Transistor emitter, base and collector voltages.
- * Frequency and power levels at different circuit points.
- * Module control line and power supply interconnections in the module and instrument.

NOTE

*Start with the tables that are labeled with a Service Sheet number (Example: **Table 80-15 SS36 DC Voltages**). Other tables are more general and are to be used at your discretion. It is suggested that you familiarize yourself with the contents of these tables so you can determine if they will be effective in solving your particular troubleshooting need.*

Table 80-15	SS36 DC Voltages	80-23
Table 80-16	SS36 RF Power Levels	80-23
Table 80-17	SS36 Sum Loop Frequency Select Table	80-23
Table 80-18	SS37 DC Voltages	80-23
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Table 80-20	SS37 Typical Filter Response	80-24
Table 80-21	SS37 Overall Performance of IF Filter/Amp Chains	80-24
Table 80-22	SS38 DC Voltages	80-25
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Table 80-26	SS39 Setting Register Outputs in Serial Data Interface	80-27
Table 80-27	SS40 Worst Case Divider Harmonics	80-28
Table 80-28	SS40 Divider Specifications	80-28
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Table 80-30	SS41 Divide Band Frequencies	80-29
Table 80-31	A12 Power Supply Distribution Table	80-29
Table 80-32	Control Line Interconnections (Between Modules)	80-29
Table 80-33	Setting Control Lines	80-30
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SERVICE SHEET 36**Table 80-15. SS36 DC Voltages**

Transistor	Collector	Base
Q1-Q5*	5.5 to 6.5 Vdc	0.6 to 0.9 Vdc
Transistor	Emitter	Base
Q6**	-0.2 to +5.2 Vdc	0.4 to 5.9 Vdc
* Q1 through Q4 measurements are taken when each transistor's VCO is selected.		
** Q6's voltage varies with the Shaper DAC setting.		

Table 80-16. SS36 RF Power Levels

Measurement Point	Level
TP8	-6 to +5 dBm
TP9	3 to 10 dBm

Table 80-17. SS36 Sum Loop Frequency Select Table

HP 8642 Output Frequency	VCO #	REF Frequency	IF Frequency
528.750001 to 562.5 MHz	1	607.5 MHz	REF-OUTPUT
562.500001 to 607.5 MHz	1	652.5 MHz	REF-OUTPUT
607.500001 to 652.5 MHz	1	697.7 MHz	REF-OUTPUT
652.500001 to 697.5 MHz	2	607.5 MHz	OUTPUT-REF
697.500001 to 742.5 MHz	2	652.5 MHz	OUTPUT-REF
742.500001 to 787.5 MHz	2	697.5 MHz	OUTPUT-REF
787.500001 to 832.5 MHz	3	877.5 MHz	REF-OUTPUT
832.500001 to 877.5 MHz	3	922.5 MHz	REF-OUTPUT
877.500001 to 922.5 MHz	3	967.5 MHz	REF-OUTPUT
922.500001 to 967.5 MHz	4	877.5 MHz	OUTPUT-REF
967.500001 to 1012.5 MHz	4	922.5 MHz	OUTPUT-REF
1012.500001 to 1057.5 MHz	4	967.5 MHz	OUTPUT-REF

Example: At 550 MHz: IF FREQUENCY = 607.5 (ref. freq) - 550 (output freq.) = 57.5 MHz.

SERVICE SHEET 37**Table 80-18. SS37 DC Voltages**

Transistor	Collector	Base
Q1	6.2 to 7.9 Vdc	0.6 to 1.2 Vdc
Q2-Q6	4.3 to 6.1 Vdc	0.6 to 0.9 Vdc
Q7	5.0 to 6.9 Vdc	0.7 to 1.0 Vdc
Q8	4.9 to 6.9 Vdc	0.6 to 0.9 Vdc
Q9, Q10	4.3 to 6.0 Vdc	0.6 to 0.9 Vdc

Table 80–19. SS37 RF Power Levels

Stage	Input Level	Output Level	Gain
Power Splitter	6 to 10 dBm	0 to 8 dBm	
Output Limiter/Amp Stage 1 Q6 Stage 2 Q4 Stage 3 Q2	0 to 8 dBm	3 to 9 dBm	≈ 20 dBm* ≈ 6 dBm* ≈ 7 dBm* ≈ 7 dBm*
LO Limiter/Amp Stage 1 Q10 Stage 2 Q9 Stage 3 Q5 Stage 4 Q3 Stage 5 Q1	0 to 8 dBm	16.5 to 20 dBm	≈ 40 dBm* ≈ 5 dBm* ≈ 5 dBm* ≈ 5 dBm* ≈ 7 dBm* ≈ 18 dBm*
9 dB pad	0 to 3 dBm	–9 to –6 dBm	
Mixer (LO Port)	16.5 to 20 dBm	–16 to –12 dBm	
Mixer (RF Port)	–9 to –6 dBm	–16 to –12 dBm	
IF Amp	–16 to –12 dBm	5 to 10 dBm	≈ 20 dBm
* These stages are normally driven into compression causing the stage to limit. The value given is with input levels at amplitudes so as not to drive the stage into compression (≈ -30 dBm). Under normal operation, actual stage gains are much lower. Normal operating gain can be derived from the Input Level and Output Level columns.			

Table 80–20. SS37 Typical Filter Response

Filter	Input Level	Cutoff Freq	Freq	Response
IF Filter	≈ -15 dBm	120 MHz	100 MHz	–1.5 dBc
			150 MHz	< –10 dBc
			200 MHz	< –30 dBc
			250 MHz	< –50 dBc
			300 MHz	< –70 dBc
			≥ 375 MHz	< –100 dBc

Table 80–21. SS37 Overall Performance of IF Filter/Amp Chain

Input	Output Freq.	Level
1 to 400 MHz at –15 dBm	1 to 50 MHz	5 dBm
	100 MHz	2 dBm
	150 MHz	–10 dBm
	200 MHz	–30 dBm
	300 MHz	–60 dBm
	375 MHz to 1.5 GHz	–90 dBm

SERVICE SHEET 38**Table 80-22. SS38 DC Voltages**

Transistor	Collector	Base
Q2,Q5	5.3 to 6.9 Vdc	0.9 to 1.3 Vdc
Q3	5.0 to 6.9 Vdc	0.7 to 1.0 Vdc
Transistor	Emitter	Base
Q1	-6.5 to -5.5 Vdc	-5.8 to -4.8 Vdc
Q6	6.0 to 6.4 Vdc	6.5 to 7.3 Vdc

Table 80-23. SS38 RF Power Levels

Stage	Input Level	Output Level	Gain
RF Port Driver	5 to 10 dBm	16.5 to 19.5 dBm	≈ 12 dBm
LO Port Driver Stage 1 (Q3) Stage 2 (Q5)	0 to 3 dBm	16.5 to 19.5 dBm	≈ 20 dBm ≈ 8 dBm ≈ 12 dBm
Phase Detector	16.5 to 19.5 dBm	0 Vdc Locked 0.7 Vpp Unlocked	

Table 80-24. SS38 Typical Filter Response

Filter	Cutoff Freq	Freq	Response
Sum Loop Low-Pass	24 MHz	10 MHz	< -2.0 dBc
		20 MHz	< -3 dBc
		30 MHz	< -20 dBc
		45 MHz	< -70 dBc
		≥ 100 MHz	< -70 dBc

SERVICE SHEET 39

Table 80-25. Internal Voltmeter Measurements

Enter Service Mode	Function	Line Label	Explanation
SHIFT SPCL 3 2	1 9 HZ	SUM OOL LINE (U10 pin4)	+5V (locked) 0V (unlocked)
	2 0 HZ	PRETUNE REFERENCE VOLTAGE) (U10 pin5)	≈ 6.2 Vdc
	2 1 HZ	PRETUNE VOLTAGE (U10 pin6)	≈ 8 to 49 Vdc m = 3.874
	2 2 HZ	INTEGRATOR SENSE POINT (U10 pin 7)	≈ 2 to 12V (locked)
	2 3 HZ	SHAPER VOLTAGE (U10 pin 12)	≈ 1.5 to 5.5V With A12A3S1 Open
	2 4 HZ	COMPARATOR SENSE	+ 5V (locked) 0V (unlocked)
	2 5 HZ	+5 VDC SUPPLY LINE (U10 pin 10)	≈ 5.10 Vdc

NOTE

Internal voltmeter measurements come from sense lines that are multiplexed by A12A3 U10 and displayed on the front panel. Some lines require scaling down before being multiplexed. The HP8642 firmware corrects this scaling factor before displaying the actual multiplexer output. If an external voltmeter were to be connected at A12A3 TP4 or A4 TP3 "VM OUT" you would need to multiply its reading by "m" (in the table) to match the reading on the HP8642 front panel. All measurements can be repeated by keying in 1 HZ.

Table 80-26. Setting Register Outputs in Serial Data Interface

Line Label	Bit Number	Decimal Value
NOT USED	0	1
NOT USED	1	2
NOT USED	2	4
NOT USED	3	8
NOT USED	4	16
DIAG. SEL. 0	5	32
DIAG. SEL. 1	6	64
DIAG. SEL. 2	7	128
VC0 #4 SEL.	8	256
VC0 #3 SEL.	9	512
VC0 #2 SEL.	10	1,024
VC0 #1 SEL.	11	2,048
PRETUNE BIT #5	12	4,096
PRETUNE BIT #4	13	8,192
PRETUNE BIT #3	14	16,384
PRETUNE BIT #2	15	32,768
PRETUNE BIT #1	16	65,536
PRETUNE BIT #0	17	131,072
SHAPER BIT #5	18	262,144
SHAPER BIT #4	19	524,288
SHAPER BIT #3	20	1,048,576
SHAPER BIT #2	21	2,097,152
SHAPER BIT #1	22	4,194,304
SHAPER BIT #0	23	8,388,608

To set the outputs of the Serial Data Interface registers (U5, U2, and U15 on SS39), key in: **SHIFT** **SPCL** **3** **6** **0** **6** **Decimal Value*** **HZ**

* To determine the decimal value to enter you must first know what you want each bit to be, high or low. This gives you a 24 bit binary coded decimal (BCD). Convert this BCD to its decimal equivalent by adding the Decimal Values (from Table 80-24) of the Lines you want to be high.

NOTE

To determine which bits are set, key in **SHIFT** **SPCL** **3** **6** **0** **3** **2** **HZ**, then convert the decimal number on the display to a binary number. For example, if 5592405 is displayed, the following bit numbers are set: 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, and 22.

To set all bits low, key in: **SHIFT** **SPCL** **3** **6** **0** **6** **0** **HZ**

To set all bits high, key in: **SHIFT** **SPCL** **3** **6** **0** **6** **16777215** **HZ**

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Table 80-27. Worst Case Divider Harmonics

HP 8642 Front Panel Setting	2 nd Harmonic Freq.	Power Level
1057.5 MHz	2115 MHz	< -6 dBc
528.75 MHz	1057.5 MHz	< -6 dBc
264.375 MHz	528.75 MHz	< -6 dBc
132.1875 MHz	264.375 MHz	< -6 dBc
66.09375 MHz	132.1875 MHz	< -6 dBc
33.046875 MHz	66.09375 MHz	< -6 dBc
16.5234375 MHz	33.046875 MHz	< -6 dBc
8.26171875 MHz	16.5234375 MHz	< -6 dBc

Table 80-28. A12 Divider Specifications

Divider Input (at A12A2J3)		
Power	Spurs	Harmonics
≥ 4 dBm	≤ -110 dBc	2 nd ≤ -10 dBc 3 rd ≤ -15 dBc 4 th ≤ -25 dBc 5 th ≤ -35 dBc
Divider Output (at A12A3J3)		
Freq	Power	Spurs
4.130860 to 8.261718 MHz 8.261719 to 920 MHz 920 to 1057.5 MHz	1 to 6 dBm 0 to 6 dBm 1 to 6 dBm	≤ -110 dBc

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Table 80-29. A12 Divider Control Logic (A12A3 U104)

HP 8642 Freq.	Inputs			Outputs							
	Div 2	Div 1	Div 0	0	1	2	3	4	5	6	7
640 MHz	1	1	1	0	1	1	1	1	1	1	1
320 MHz	1	1	0	1	0	1	1	1	1	1	1
160 MHz	1	0	1	1	1	0	1	1	1	1	1
80 MHz	1	0	0	1	1	1	0	1	1	1	1
40 MHz	0	1	1	1	1	1	1	0	1	1	1
20 MHz	0	1	0	1	1	1	1	1	0	1	1
10 MHz	0	0	1	1	1	1	1	1	1	0	1
5 MHz	0	0	0	1	1	1	1	1	1	1	0

Table 80–30. A12 Divide Band Frequencies

Divide #	Frequency
÷ 1	1057.5 to 528.750001 MHz
÷ 2	528.750 to 264.375001 MHz
÷ 4	264.375 to 132.187501 MHz
÷ 8	132.1875 to 66.093751 MHz
÷ 16	66.093750 to 33.046876 MHz
÷ 32	33.046875 to 16.023438 MHz
÷ 64	16.023437 to 8.261719 MHz
÷ 128	8.261718 to 4.130860 MHz

Table 80–31. A12 Power Supply Distribution Table

Supply	A17	A5 In	A5 Out	A12 Module
+50 Vdc	J2 pins 3,4	J12 pins 3,4	J5 pin 1	A12A3 J1 pin 1
+15 Vdc	J2 pins 9,18	J12 pins 9,18	J5 pins 2,4	A12A3 J1 pins 2,4
–5 Vdc	J2 pins 23,26	J12 pins 23,26	J5 pins 8,10	A12A3 J1 pins 8,10
+5 Vdc	J2 pins 35,50	J12 pins 35,50	J5 pins 5,7	A12A3 J1 pins 5,7
–15 Vdc	J2 pins 19,22	J12 pins 19,22	J5 pin 11	A12A3 J1 pin 11
GND			J3 pins 12,13,15,17, 19,21,23,25,26,	A12A3 J1 pins 12,13,15, 17,19,21,23,25,26

Table 80–32. Control Line Interconnections (Between Modules)

Line Label	A12	A5		A4	
	Input Connector Pin	Output Connector Pin	Input Connector Pin	Output Connector Pin	Latch IC Pin
OOL Disable*	A3J3 24	A5J19 24	A5J17 27	A4P4 27	U13 16
DIV 1	A12A3J1 22	A5J5 22	A5J15 3	A4P3 3	U14 12
DIV 0	A12A3J1 20	A5J5 20	A5J15 2	A4P3 2	U14 9
DIV 2	A12A3J1 24	A5J5 24	A5J16 37	A4P2 37	U14 15
SUM CLOCK	A12A3J1 16	A5J5 16	A5J16 49	A4P2 49	U16 12
SUM DATA	A12A3J1 18	A5J5 18	A5J16 48	A4P2 48	U16 5
SUM OOL	A12A3J1 14	A5J5 14	A5J16 6	A4P2 6	U35 17
* OOL Disable: Circuitry Located on A4. Disables all out of lock interrupts to the DCU.					

Table 80–33. Setting Control Lines

(Refer to Table 80–32 Control Line Interconnections, for line pin Numbers)

Enter Service Mode	Select a Function		Select a Line	
SHIFT SPCL 3	6 0 0	Reads line state	2 2 Hz	OOL Disable
	6 0 1	Sets Line to 1	2 7 Hz	DIV 1
	6 0 2	Sets Line to 0	2 8 Hz	DIV 0
	6 1 5	*Continuous Toggle	2 9 Hz 4 4 Hz 4 5 Hz 1 1 0 Hz	DIV 2 SUM CLOCK SUM DATA **SUM OOL

* Toggling continues until HP 8642 power is turned off

** Read is the only function that can be selected for REF OOL

Example: To set DIV0 to a TTL Low (0) key in SHIFT SPCL 3 602 28 Hz

Table 80–34. A12 Special Functions

Enter Service Mode	Select a Function	
SHIFT SPCL 3	7 0 2 Hz	Turns off Sum Loop Cal Data
	7 1 2 Hz	Turns on Sum Loop Cal Data
	6 2 0 1 Hz	Displays Reference Loop Frequency
	6 2 0 2 Hz	Displays Sum Loop Frequency
	6 2 0 3 Hz	Displays IF Frequency

Adjustments

DESCRIPTION OF A12 ADJUSTMENTS

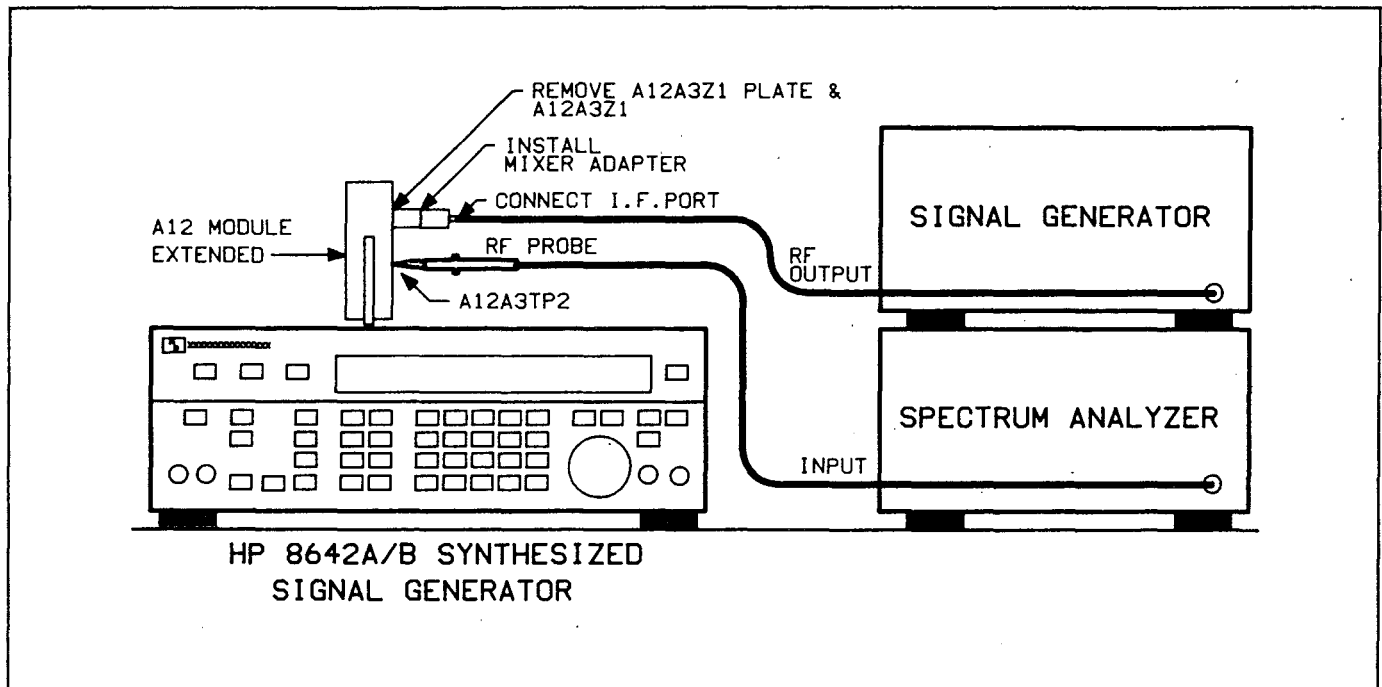
Overall Equipment List

Spectrum Analyzer	HP8566A/B
Signal Generator	HP 8642B
Measuring Receiver	HP8902A
Sensor Module	HP11722A
DVM	HP 3456A
HP-IB Printer	HP 2225A
HP 8642 Bench Service Kit	HP 11802A
34 dB Attenuator	08642-60239
2 each SMC 50 Ω Terminations	1250-0839
Power Splitter Adapter	08642-60079
8 Pin Mixer Adapter	08642-60078
RF Probe	08642-20089

NOTE

Each adjustment procedure assumes the HP 8642 internal cabling is connected normally and all circuitry is functioning properly.

There are two manual adjustment procedures for the A12 Module: the Loop Filter, and Beat Note Detector. The two adjustments can be done independently. The Loop Filter reduces the spurious signals above 45.0 MHz on the RF output of the module. The Beat Note Detector allows the module to acquire lock when the instrument is powered on. There are also VCO adjustments that are part of the Auto-Adjustment Procedure.

ADJUSTMENT 1: A12 MODULE*Figure 80-6.***Required Equipment:**

Spectrum Analyzer	HP8566A/B
Signal Generator	HP8642B
8 Pin Mixer Adapter	08642-60078
RF Probe	08642-20089

Procedure**Loop Filter Adjustment**

1. Setup:(Refer to Figures 80-6 to 80-8)

Switch the HP 8642 to Standby.

Extend the A12 module.

Remove phase detector cover and phase detector A12A3 Z1.

Set the Signal Generator power to 10 dBm and sweep from 7.5 to 100 MHz.

Set the Spectrum Analyzer to start freq: 7.5 MHz, stop freq: 100MHz, resolution BW: 100 kHz.

Install 8 Pin Mixer Adapter in place of A12A3 Z1 (notch goes towards the front of the instrument).

Connect the Signal Generator to the IF Port of the adapter.(center connector, pin 3)

Connect A12A3 TP2 to the spectrum analyzer using the RF Probe, 08642-20089.

Switch the HP 8642 ON.

2. Adjust Loop Filter Response:

Manually sweep the Signal Generator while adjusting A12A3 C17 for a response at 45.0 MHz that is less than -70 dBc. The stop band response should remain less than -60 dBc to at least 100 MHz.

Beat Note Detector Adjustment

3. Adjust Beat Note Detector Symmetry:

Ensure that no test equipment is connected to A12A3 TP2.

Move A12A3 S1 down to its OPEN position.

Adjust A12A3 R32 so that the out of lock LED, A12A3 DS1, is at about half intensity.

Restore Module

4. Switch the HP 8642 to Standby.
5. Move A12A3 S1 up to its CLOSED position.
6. Remove the 8 Pin Mixer Adapter
7. Re-install the phase detector and cover.
8. Re-install the Module.
9. Re-install the top cover.

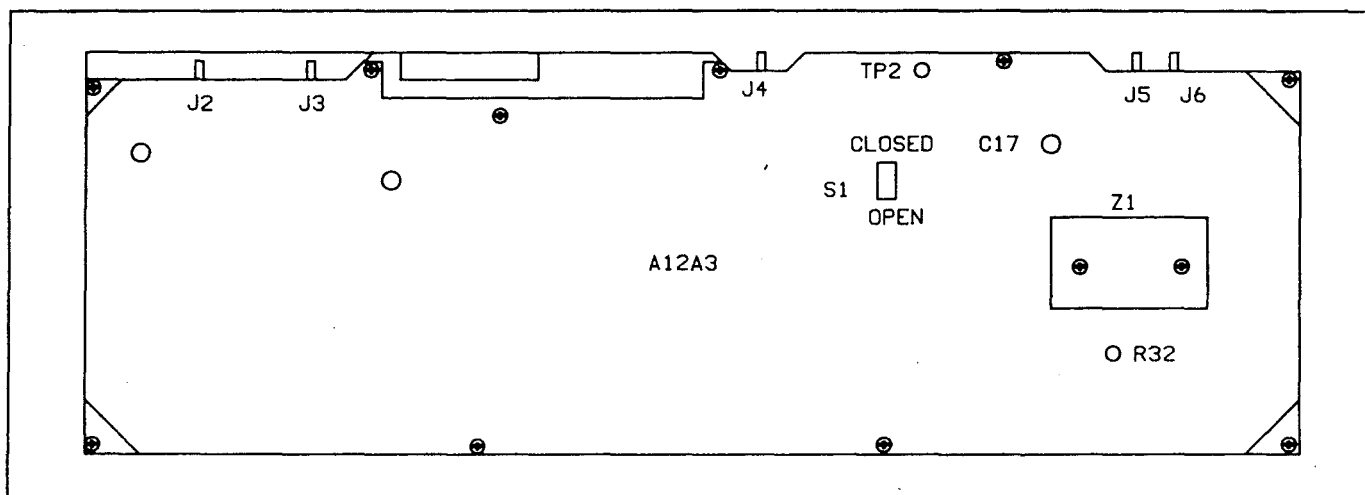


Figure 80-7.

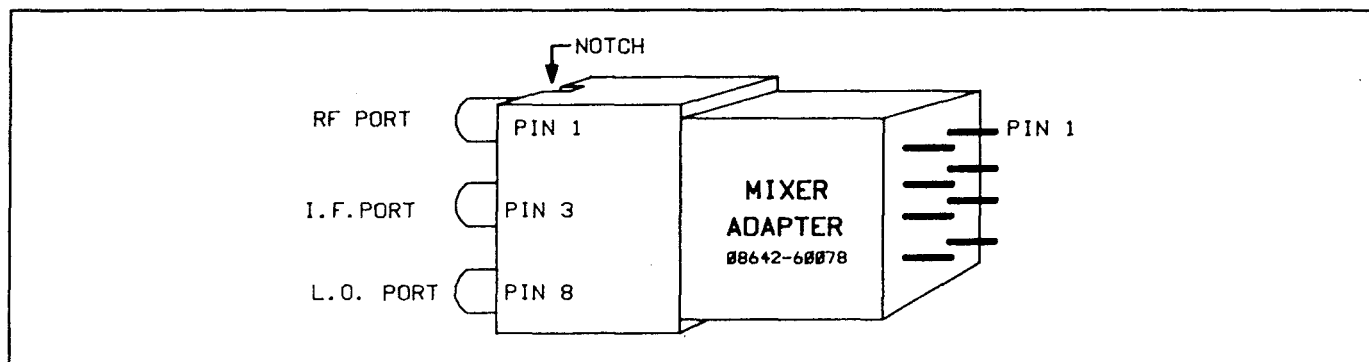


Figure 80-8.

A12 AUTO-ADJUSTMENTS

NOTE

Read section 5 before proceeding with this Auto-Adjustment procedure.

Description

The HP 8642A/B temperature must be allowed to stabilize with the covers on for one hour. Then the instrument top cover must be removed, A12 extended and the VCO frequencies must be adjusted and recorded (f_1) before temperature rise can cause significant drift. Now the temperature must be allowed to stabilize again for one hour. Once this is done, the VCO frequencies are measured again (f_2) and re-adjusted to the normal operating frequency (f_3). The Auto Adjust Routine is now run to generate data for the DAC's in the A12 Module. This consists of five setups and then the Cal Data transfer. After the Auto Adjust Routine has been finished, the VCO's are measured (f_4) and adjusted to the normal center frequency plus the frequency difference between normal and elevated temperature ($f_4 + f_2 - f_3$). The Instrument Level Diagnostics are run to insure that the HP 8642 is functional. Now the new A12 Cal Data is copied to the A20.

Required Equipment:

Measuring Receiver	HP8902A
Sensor Module	HP11722A
DVM	HP3456A
HP-IB Printer	HP2225A
34 dB Attenuator	08642-60239
2 each SMC 50 Ω Terminations	1250-0839
8 Pin Mixer Adapter	08642-60078
Power Splitter Adapter	08642-60079
Alignment Tool	8710-1515

Procedure

1. Before Beginning:

Insure that you will be performing this procedure in a temperature controlled environment. The procedure will take several hours (mostly unattended) and must be done continuously. It is important that the time periods in the temperature stabilization steps be followed closely. A significant change in temperature will cause the VCO's to drift in frequency and the HP 8642 will abort the procedure.

2. Temperature Stabilization:

With instrument power on and all internal and external covers in place, allow the instrument to warm up for 1 hour.

3. VCO Adjustment Setup: (Refer to Figures 80-9 to 80-11)

Connect the time base out from the HP 8642 to the HP 8902's 10 MHz time base in.

Disconnect cable W31 (901) from A12A2 J2 and connect a 50 Ω load termination to J2.

Disconnect W30 (956) from A12A3 J6 and connect a 50 Ω load termination to J6.

Extend A12 Module on extender posts.

Move LOOP SWITCH A12A3 S1, on right side of A12 Module, down to its OPEN position.

Remove power splitter cover (A12A2 Z2) from the left side of the A12 Module.

Remove power splitter (A12A2 Z2) by gently pulling out with needle nose pliers.

Connect the Power splitter Adapter (HP 08642-60079) to sockets on the board. (Position adapter in sockets so that the crescent-shaped notch by SMC connectors is on the side toward front of instrument.)

Connect Sensor Module to adapter, pin 1, using a short piece of flexible coax cable (2 inch).

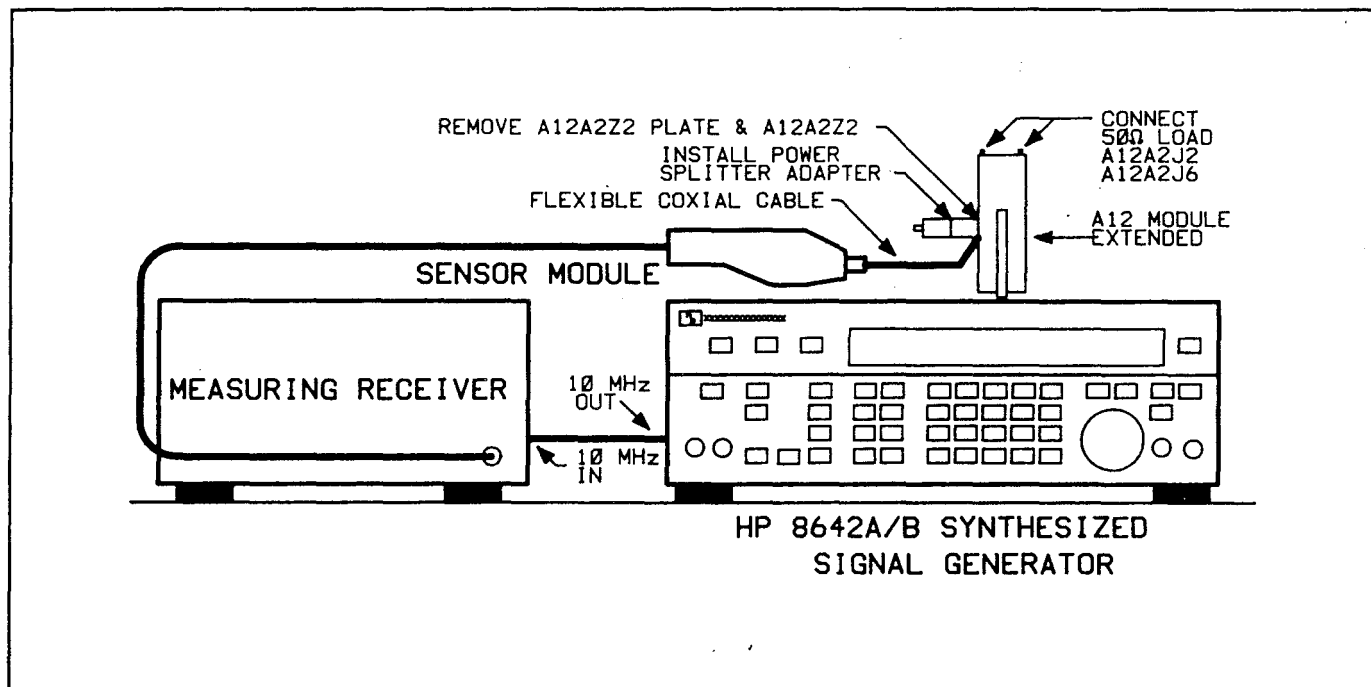


Figure 80-9. A12 VCO Adjustment Set-up 1

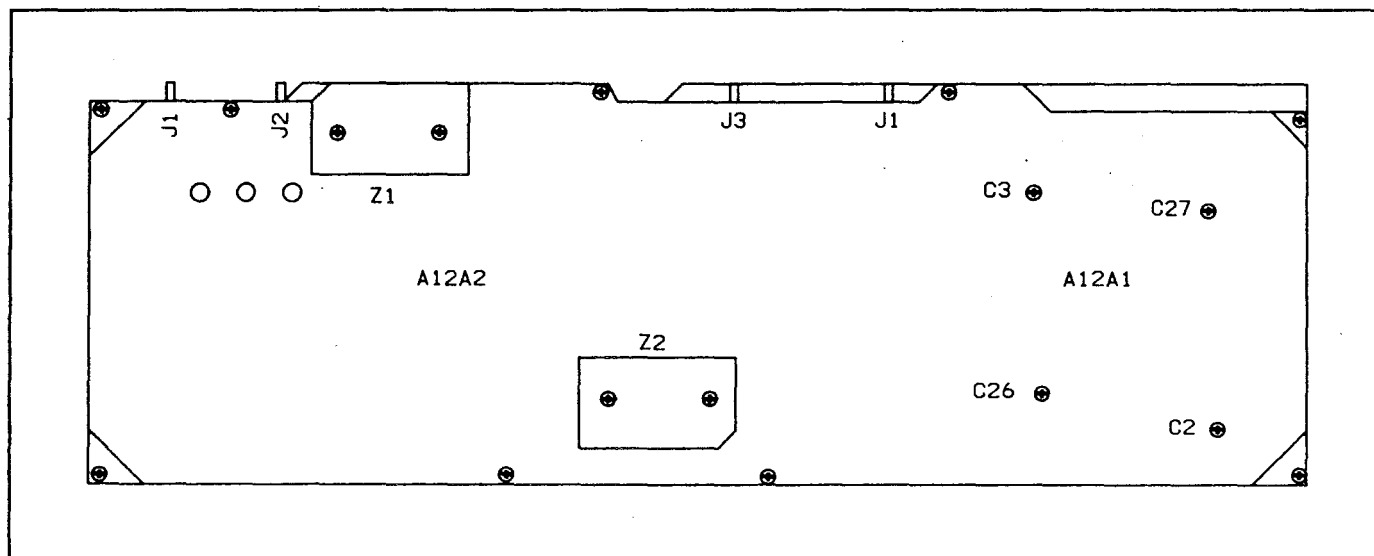


Figure 80-10. A12 Module left side. (Covers must be removed to access labeled components)

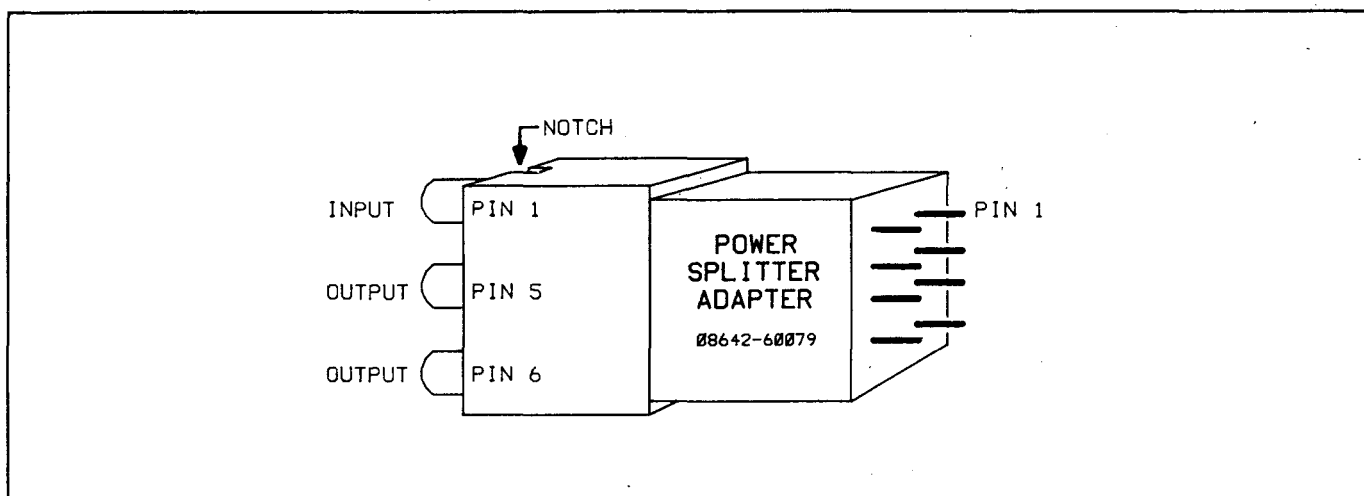


Figure 80-11.

4. Adjust Initial VCO Frequency:

(This must be done immediately after the module is extended so that the temperature is approximately the same as it is during normal operation.)

Enter the key sequence given in the table below for each of the A12A1 Adjustments. Adjust the component for each key sequence (A12A1 Adj column, use alignment tool) until the Measuring Receiver frequency reading (f_1) is within the limits given and record the value for later use. (Refer to Figure 80-10)

Use the measuring receiver to verify that the power level is greater than +4 dBm at each of the VCO frequencies.

HP 8642 Key Sequence	A12A1 Adj.	f_1 (MHz)		
		Min	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C2	652.750	___ . ___	665.750
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C3	787.250	___ . ___	800.750
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C27	921.750	___ . ___	935.750
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C26	1055.00	___ . ___	1070.000

5. Verify VCO Range:

Enter the key sequence given in the table below for each of the A12A1 VCO's.

Verify that the frequency reading is less than the Maximum given in the table below.

Verify that the power level is greater than +4 dBm at each of the VCO frequencies.

NOTE

If the Actual frequency is greater than Max, or power level is less than +4dBm, repeat steps 4 and 5.

HP 8642 Key Sequence	Frequency (MHz)	
	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 6338 Hz, 63432 Hz	_____	528.750
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63310 Hz, 63432 Hz	_____	653.750
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63312 Hz, 63432 Hz	_____	788.750
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63315 Hz, 63432 Hz	_____	923.750

6. Temperature Stabilization:

With instrument power on and the module extended, allow the instrument to warm up for 1 hour.

7. Measure Extended Module Operating Frequency:

After the 1 hour warm up, enter the key sequence given in the table below for each of the A12A1 VCO's. Record each VCO's Frequency (f_2) for later use.

HP 8642 Key Sequence	f_2 (MHz) Actual
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____

8. If any of the (f_2) frequencies are not within the given limits of the following table, Re-adjust the extended module to its normal operating frequency and record the actual Measuring Receiver reading (f_3) for later use.

HP 8642 Key Sequence	A12A1 Adj.	f_3 (MHz)		
		Min	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C2	652.750	_____	665.750
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C3	787.250	_____	800.750
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C27	921.750	_____	935.750
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C26	1055.00	_____	1070.00

9. Initialize Auto Adjust Routine:

Connect the Required Equipment to the HP 8642 via HP-IB. (Printer Measuring Receiver, and DVM, disconnect any HP-IB controller from the HP-IB bus.)

Key in: **INST PRESET**

Key in: **SHIFT SPCL 3 8 8 Hz 8 0 Hz**.

Key in: **2 Hz** when "ENTER ROUTINE NUMBER .G8000" appears.

Key in the the Day, Month, Year and Module Cal ID Number when prompted by the HP 8642 display. (See Section 5 for details.)

10. When "WAITING FOR SET-UP 1 .V24" appears: (refer to Figure 80-9)

Verify the setup is unchanged from Step 3.

Press **Hz** to continue. (Run time \approx 60 seconds)

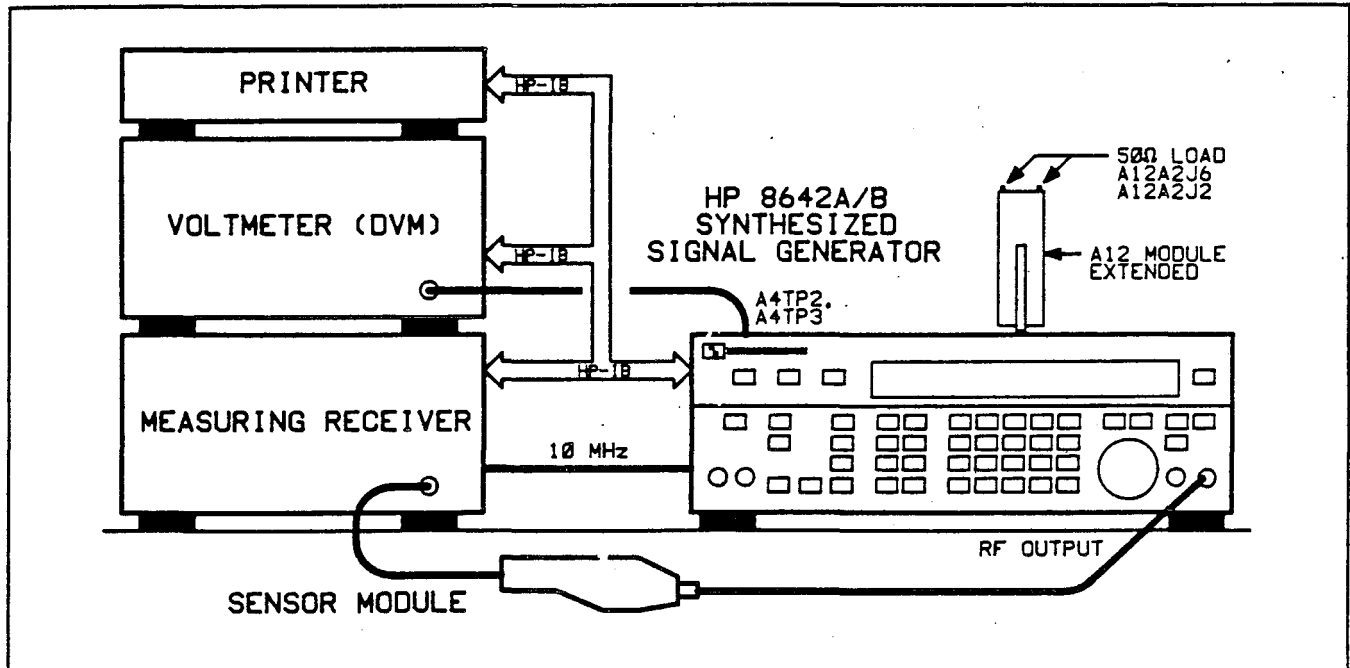


Figure 80-12. Set-up 2

11. When "WAITING FOR SET-UP 2 .V25" appears: (refer to Figure 80-12)

Replace the Power Splitter A12A2Z2. A12A2Z2 pin 1 (Pin with blue on it's base), plugs into the square pad on the A12A2 board..

Replace cover over Power Splitter.

Connect Sensor Module to RF OUTPUT on HP 8642 Front Panel.

Connect the DVM to the VM OUT (A4TP3) and ground test (A4TP2) points on the left side of the A4 Module.

Set the DVM to measure Volts DC.

Remaining set-up conditions from Step 10 are unchanged.

Press **Hz** to continue. (Run time ≈ 105 minutes)

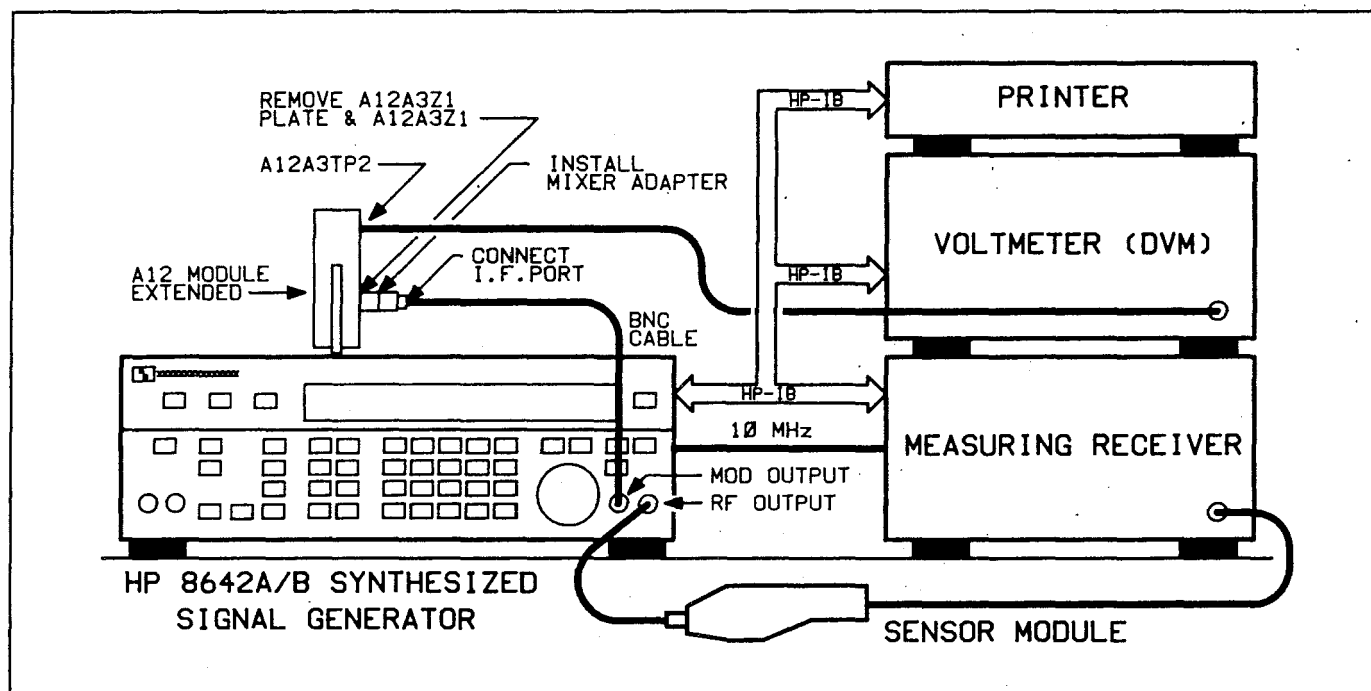


Figure 80-13. Set up 3

12. When "WAITING FOR SET-UP 3 .V26" appears: (refer to Figure 80-13 Set-up 3)

Remove the phase detector cover from right side of the A12 Module.

Remove the phase detector (A12A3 Z1) by gently pulling with needle nose pliers.

Connect the 8 Pin Mixer Adapter (HP 08642-60078) to sockets on the board. (Position adapter in sockets so that the crescent-shaped notch by SMC connectors is on the side toward front of instrument.)

Connect a BNC cable from MOD OUTPUT port to center SMC connector on 8 Pin Mixer Adapter.

Connect DVM to A12 Module at A12A3 TP2.

Set DVM to measure AC Volts.

All other Setup conditions are unchanged.

Press **[Hz]** to continue. (Run time \approx 30 seconds)

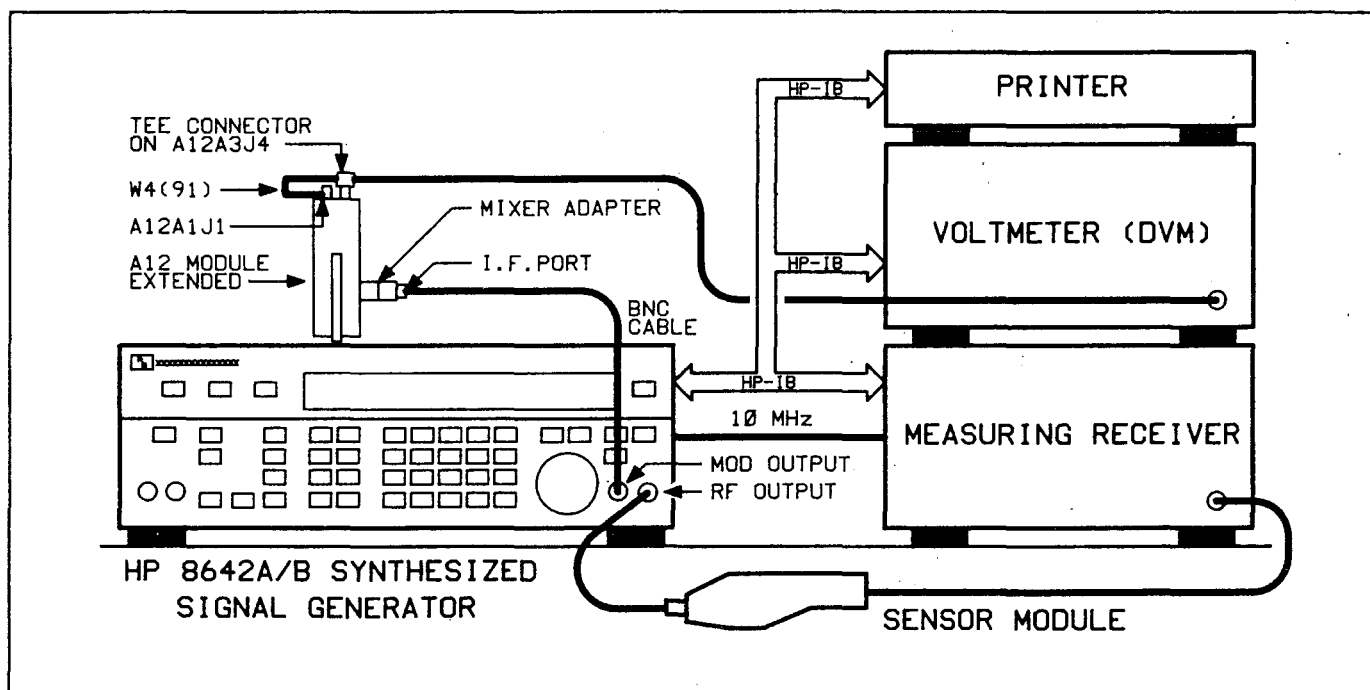


Figure 80-14. Set up 4

13. When **"WAITING FOR SET-UP 4 .V27"** appears: (refer to Figure 80-14 Set-up 4)

Disconnect cable A12 W4 (91) from A12A3 J4.

Connect an SMC Tee connector to A12A3 J4.

Connect cable A12 W4 to the Tee connector.

Connect the DVM to the Tee connector.

Set the DVM to measure AC Volts.

All other setup conditions are unchanged.

Press **[Hz]** to continue. (Run time \approx 10 minutes)

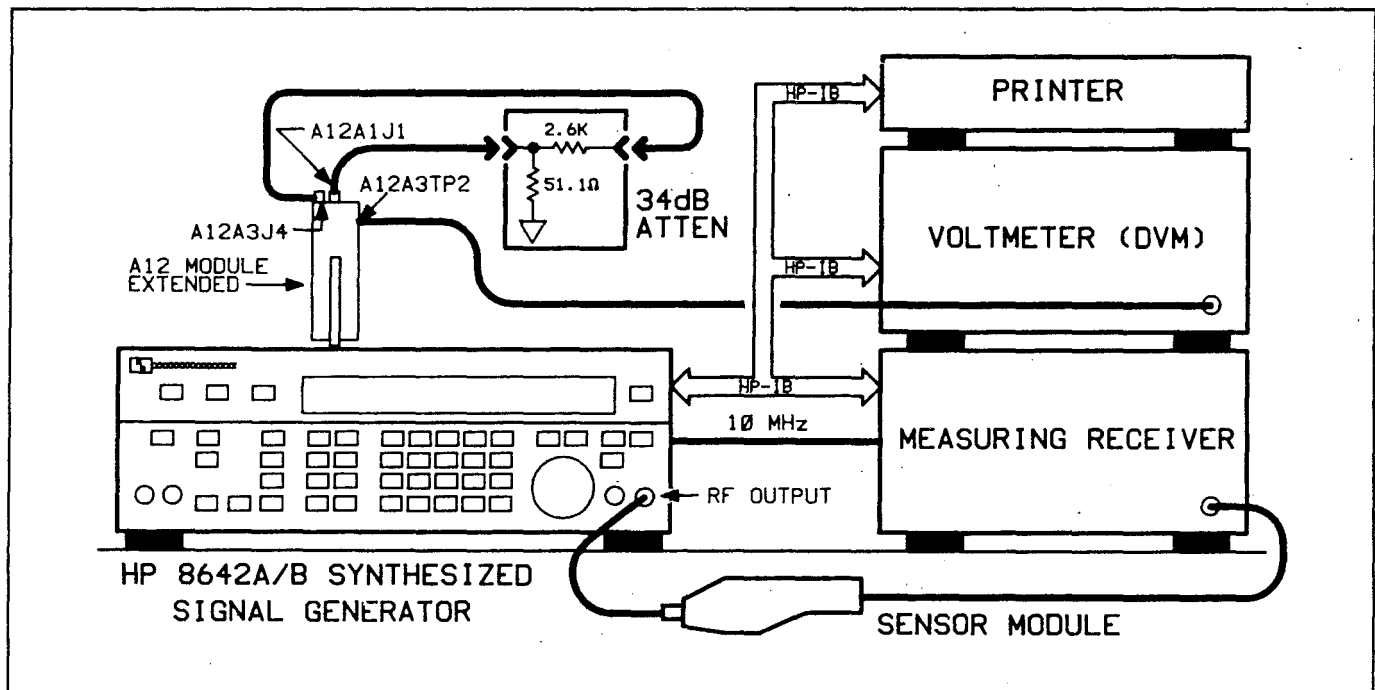


Figure 80-15. Set up 5

14. When "WAITING FOR SET-UP 5 .V28" appears: (refer to Figure 80-15 Set-up 5)

Disconnect MOD OUTPUT cable and mixer adapter from instrument.

Replace the phase detector (A12A3 Z1) in instrument: Align pin 1 on phase detector with square pad socket on board and insert.

Replace cover over phase detector.

Connect DVM to A12A3 TP2 on A12 Module.

Set DVM to measure AC Volts.

Press the **TRACK MODE** button on the Modulation Analyzer or Measuring Receiver. (Ensure that the light in the button is on, indicating Track Mode operation.)

Disconnect 50Ω terminations from A12A2 J2 and A12A3 J6.

Reconnect cable W31 (901) to A12A2 J2.

Reconnect cable W30 (956) to A12A3 J6.

Move A12A3 S1, on right side of module, up to its CLOSED position.

Remove SMC Tee connector from A12A3 J4.

Connect the 2600Ω end of the 34 dB attenuator to A12A3 J4.

Connect end of cable A12W4 from A12A1 J1 to the 51.1Ω input of the 34 dB attenuator.

Press **Hz** to continue. (Run time ≈ 8 minutes)

15. When **"UNPROTECT CAL. MEMORY .G8005"** appears:

Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.

Press **[Hz]** to Continue.

16. When **"PROTECT CAL. MEMORY .G8006"** appears:

Switch A3 S2 toward the front of the instrument to protect the EEPROM's.

Press **[Hz]** to Continue.

17. When **"RECONNECT ALL CABLES .V29"** appears:

Disconnect all test cables from the instrument.

Reconnect any instrument cables which are still disconnected.

Press **[Hz]** to Continue.

18. VCO Re-adjustment Setup:

PERFORM STEPS 18 through 22 FOR ANY VCO's THAT WERE RE-ADJUSTED DURING STEP 8.

Disconnect cable W31 (901) from A12A2 J2 and connect a 50K Ω load termination to J2.

Disconnect W30 (956) from A12A3 J6 and connect a 50 Ω load termination to J6.

Move LOOP SWITCH A12A3 S1, on right side of A12 Module, down to its OPEN position.

Disconnect cable W24 from A12A1 J3; terminate A12A1 J3 with 50 Ω .

Connect the Sensor Module to the front panel RF Output.

19. Measure VCO Frequencies:

Enter the key sequence given in the table below for each of the A12A1 VCO's. Record each VCO's Frequency (f_4).

HP 8642 Key Sequence	f_4 (MHz) Actual
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____ . _____
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____ . _____
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____ . _____
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	_____ . _____

20. Compute the correct re-adjustment frequency for any VCO's that were re-adjusted in step 8:

Adjustment C2: $(f_4 + f_2 - f_3) - (1\text{MHz}) = f_5 \text{ Min} = \text{_____} . \text{_____} \text{ MHz}$

$(f_4 + f_2 - f_3) + (1\text{MHz}) = f_5 \text{ Max} = \text{_____} . \text{_____} \text{ MHz}$

Adjustment C3: $(f_4 + f_2 - f_3) - (1\text{MHz}) = f_5 \text{ Min} = \text{_____} . \text{_____} \text{ MHz}$

$(f_4 + f_2 - f_3) + (1\text{MHz}) = f_5 \text{ Max} = \text{_____} . \text{_____} \text{ MHz}$

Adjustment C27: $(f_4 + f_2 - f_3) - (1\text{MHz}) = f_5 \text{ Min} = \text{_____} . \text{_____} \text{ MHz}$

$(f_4 + f_2 - f_3) + (1\text{MHz}) = f_5 \text{ Max} = \text{_____} . \text{_____} \text{ MHz}$

Adjustment C26: $(f_4 + f_2 - f_3) - (1\text{MHz}) = f_5 \text{ Min} = \text{---} . \text{---} \text{ MHz}$

$(f_4 + f_2 - f_3) + (1\text{MHz}) = f_5 \text{ Max} = \text{---} . \text{---} \text{ MHz}$

21. Re-adjust the extended module to its normal operating frequency and record the actual Measuring Receiver reading (f_5): (see Figure 80-4, for adjustment locations)

(Re-adjust only the VCO's that were re-adjusted during step 8.)

HP 8642 Key Sequence	A12A1 Adj.	f5 (MHz)		
		Min	Actual	Max
INST PRESET, 640 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C2	--- . ---	--- . ---	--- . ---
INST PRESET, 720 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C3	--- . ---	--- . ---	--- . ---
INST PRESET, 900 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C27	--- . ---	--- . ---	--- . ---
INST PRESET, 1050 MHz, SHIFT, SPCL, 3, 63361 Hz, 63463 Hz	C26	--- . ---	--- . ---	--- . ---

Restore Module

22. Close loop switch A12A3S1
23. Re-install Module.
24. Re-connect all cables.
25. Re-install top cover.
26. Allow the instrument to stabilize (with power on) for one hour.
27. Run the instrument level diagnostics to verify operation:

Key in: **SHIFT** **SPCL** **3** **3** **0** **Hz**.

When **"WAITING FOR SETUP 1 .Z24"** appears, connect the MOD OUT to the AM/PULSE INPUT and FM/ΦM INPUT.

Press **Hz** to Continue.

28. When **"DIAG DONE HIT MSSGS .V1"** appears:

Press the MSSG key to view the message buffer. If **"NO MESSAGES .00"** is contained in the message buffer, the HP 8642 is functioning properly.

29. Up Load Cal Data:

Now that the functionality of the HP 8642 has been verified, use the following procedure to up load the new cal data.

Switch the HP 8642 to standby.

Remove the A20 Cal Module. (See Disassembly Procedures).

Plug the A20 Module on to A3 J3.

Switch the HP 8642 on.

Switch A20 S1 to the CHANGE position.

Key in: **SHIFT** **SPCL** **3** **7** **2** **2** **Hz**.

When "**TRANSFER VERIFIED** **.U613**" appears on the display, move A20 S1 up to its **PROTECTED** position.

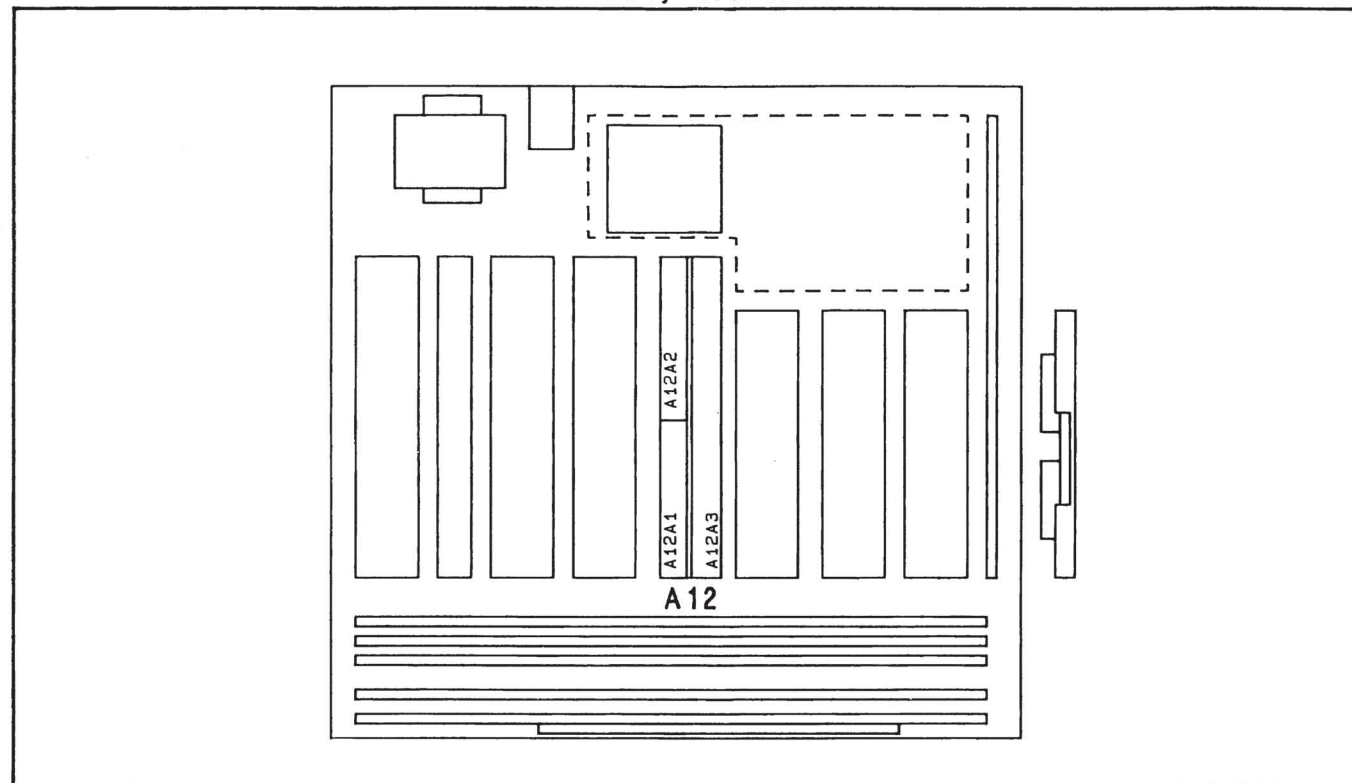
Key in: **Hz** to end the routine.

Switch the HP 8642 to Standby.

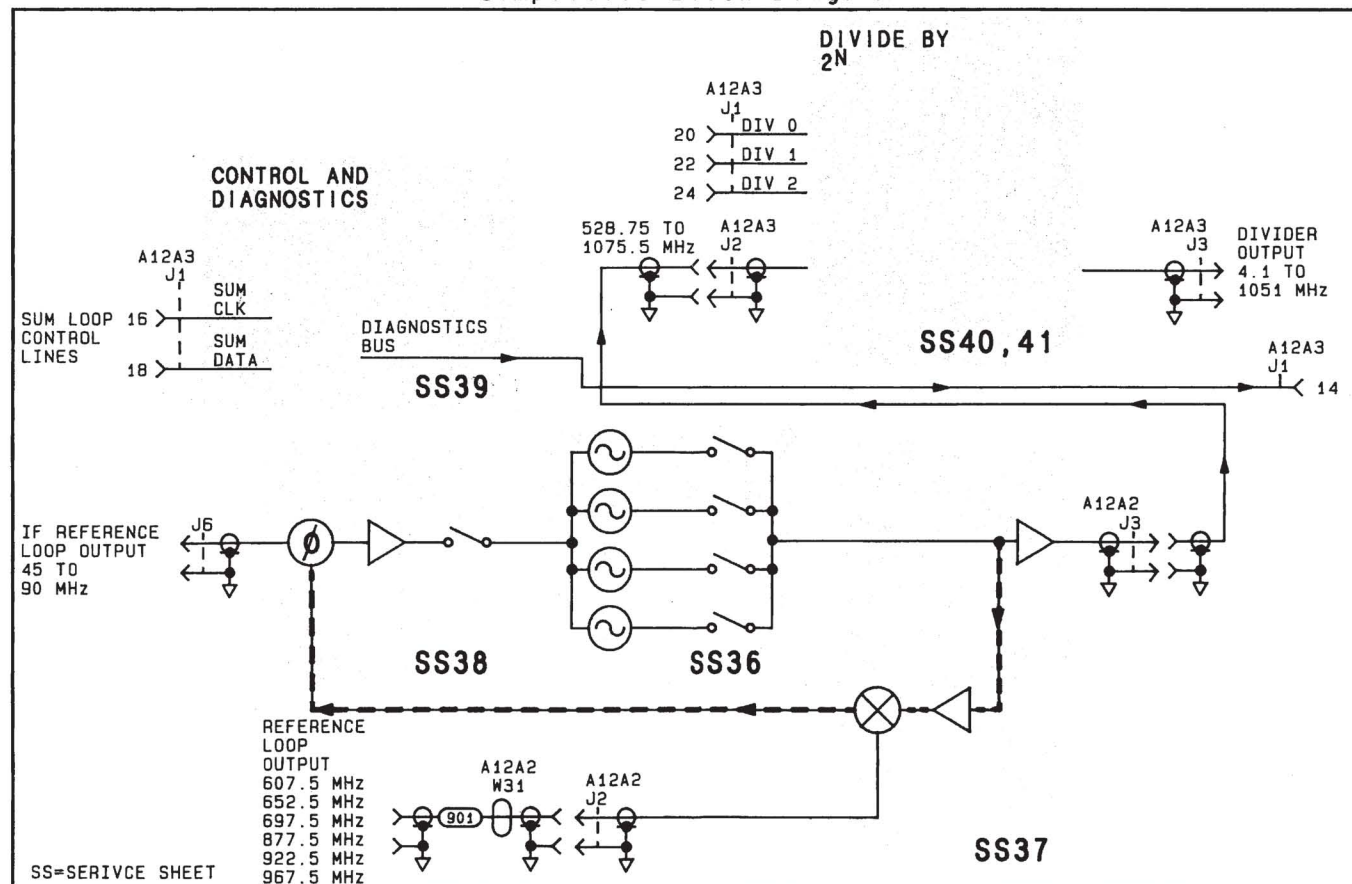
Reconnect the A20 module to the rear panel (See Disassembly Procedures).

Re-install the top cover.

Assembly Locator



Simplified Block Diagram



Module Test Point/Adjustment Locations

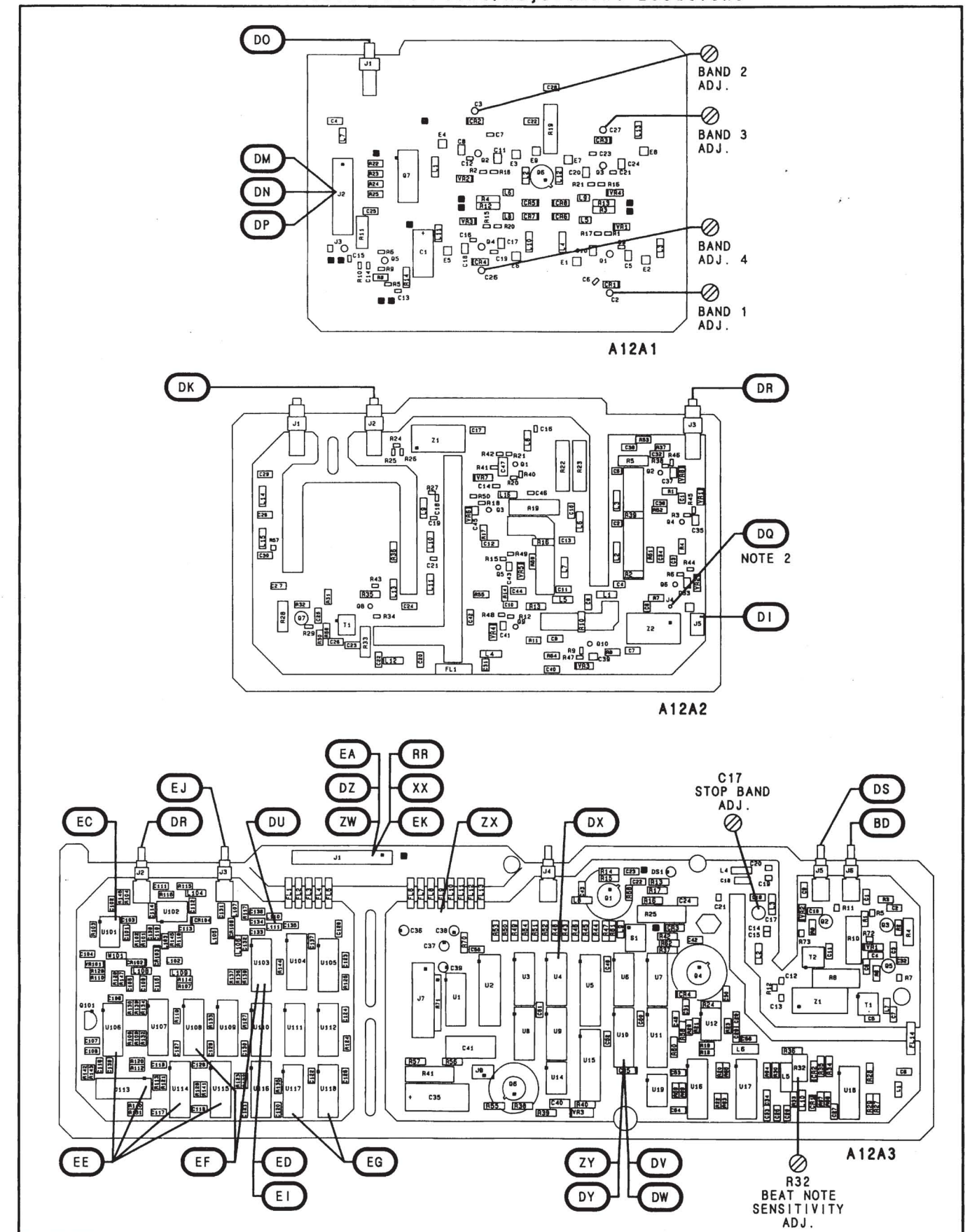


Figure 80-100 BD12,13 General Information.

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ARTEK-MANUALS**



Figure 80-101
80-101

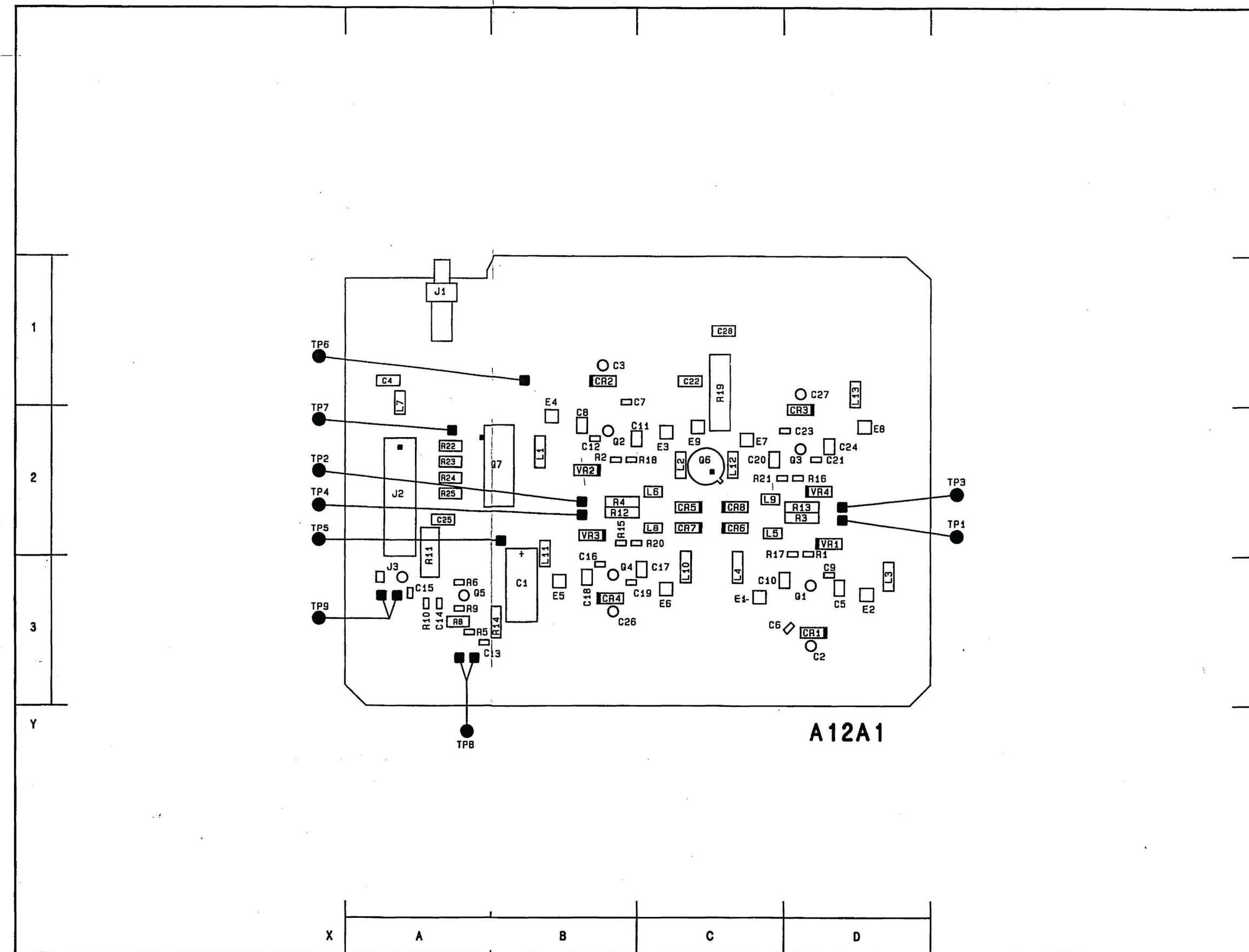
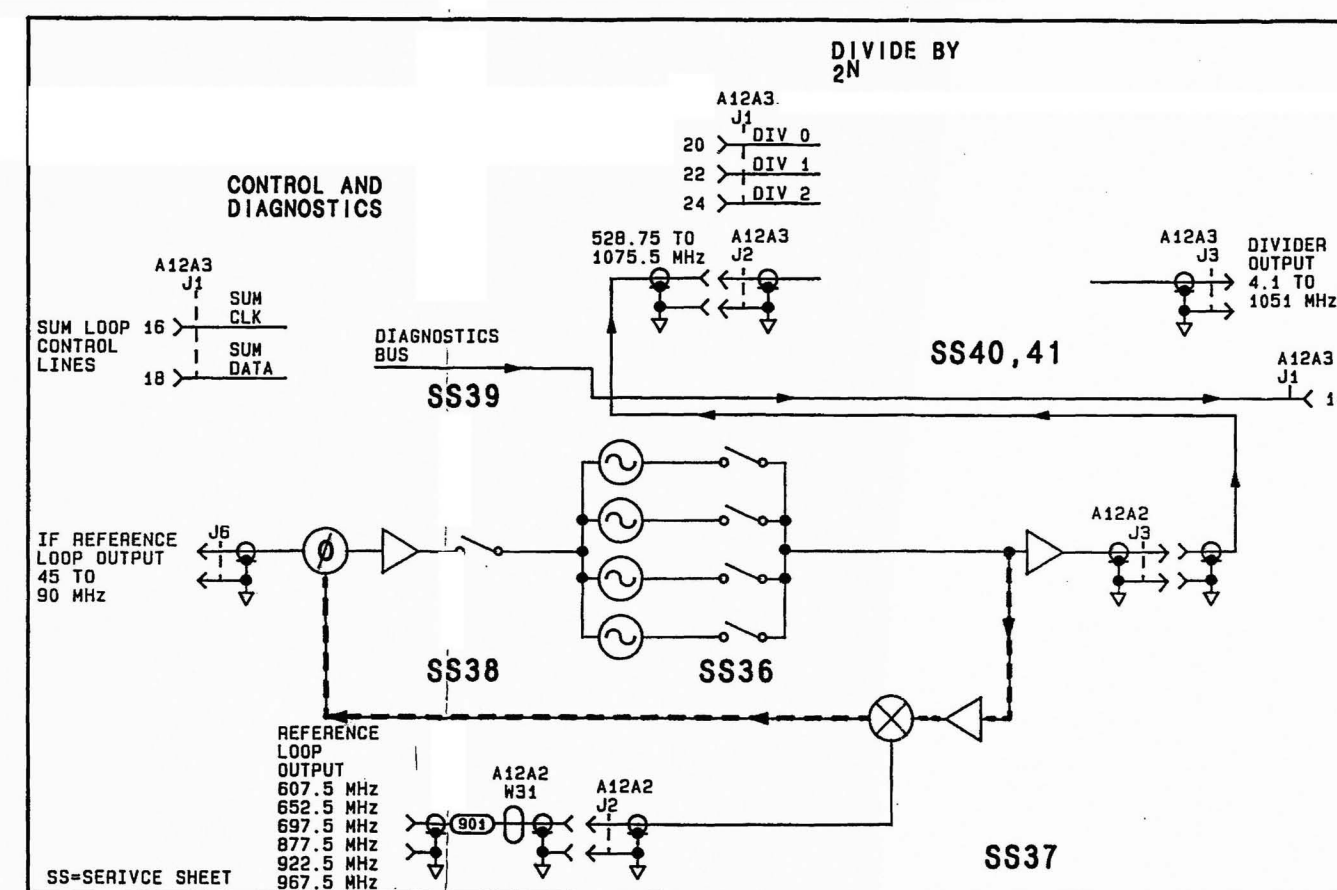


Figure 80-104. SERVICE SHEET 36 INFORMATION

Component Locator



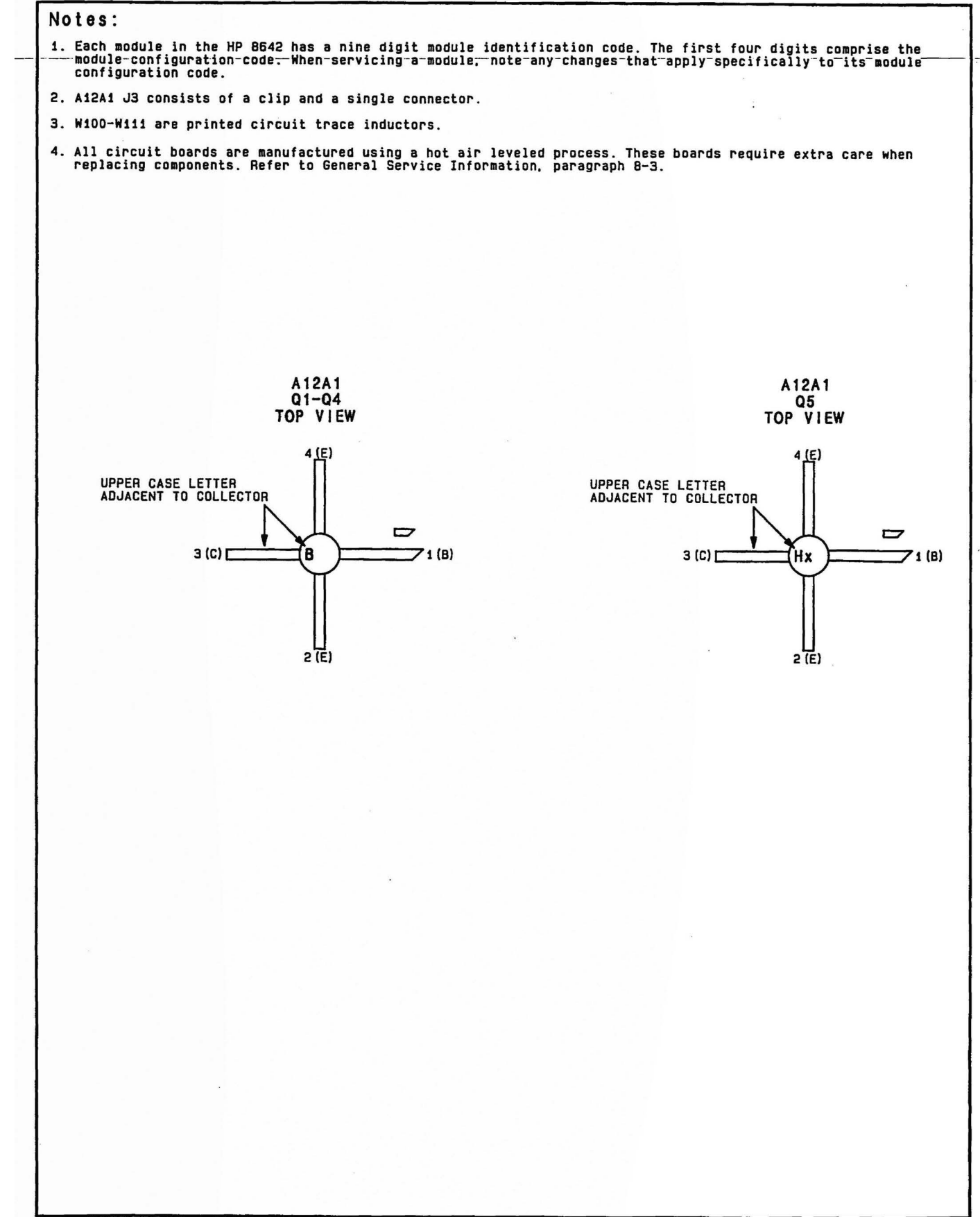
Reference Block Diagram

Component Coordinates

COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y
C1	B, 3	E1	C, 3	R1	D, 2	VR1	D, 2										
C2	D, 3	E2	C, 3	R2	B, 2	VR2	B, 2										
C3	B, 1	E3	C, 2	R3	D, 2	VR3	B, 2										
C4	A, 1	E4	B, 2	R4	B, 2	VR4	D, 2										
C5	D, 3	E5	B, 3	R5	A, 3												
C6	D, 3	E6	C, 3	R6	A, 3												
C7	B, 1	E7	C, 2	R7	A, 3												
C8	B, 2	E8	D, 2	R8	A, 3												
C9	D, 3	E9	C, 2	R9	A, 3												
C10	C, 3			R10	A, 3												
C11	B, 2	J1	A, 1	R11	A, 2												
C12	B, 2	J2	A, 2	R12	B, 2												
C13	A, 3	J3	A, 3	R13	D, 2												
C14	A, 3			R14	B, 2												
C15	A, 3	L1	B, 2	R15	B, 2												
C16	B, 3	L2	C, 2	R16	D, 2												
C17	C, 3	L3	D, 3	R17	D, 2												
C18	B, 3	L4	C, 3	R18	B, 2												
C19	B, 3	L5	C, 3	R19	C, 3												
C20	C, 2	L6	C, 2	R20	C, 2												
C21	D, 2	L7	A, 1	R21	C, 2												
C22	C, 1	L8	A, 2	R22	A, 2												
C23	D, 2	L9	C, 2	R23	A, 2												
C24	D, 3	L10	C, 3	R24	A, 2												
C25	A, 3	L11	B, 3	R25	A, 2												
C26	B, 3	L12	C, 2														
C27	D, 1	L13	D, 1	TP1	D, 2												
C28	C, 1			TP2	B, 2												
CR1	D, 3	Q1	D, 3	TP3	D, 2												
CR2	B, 1	Q2	B, 2	TP4	B, 2												
CR3	D, 2	Q3	D, 2	TP5	B, 2												
CR4	B, 3	Q4	B, 3	TP6	B, 1												
CR5	C, 2	Q5	A, 3	TP7	A, 2												
CR6	C, 2	Q6	C, 2	TP8	A, 3												
CR7	C, 2	Q7	B, 2	TP9	A, 3												
CR8	C, 2																

A12 MODULE BD 13

SEE REVERSE SIDE



Schematic General Information

CHANGES**2706A and above**

On the Component Locator:

- CR9 - To the immediate right of J1, add CR9. It should be positioned vertically with the striped (cathode) end pointing up.

In the Component Coordinates:

- CR9 - Add CR9 with grid coordinates A,1.

On the Schematic:

- Change the part number of the A12A1 Assembly to 08642-60209.
- CR9 - In **BUFFER**, to the left of E9, connect the cathode of CR9 to the main signal line (from J1), and connect the anode to ground.

2731A Only

On the A12A1 Component Locator:

- C29, C30 - Add C29 to the upper left side of C2, add C30 to the upper right side of C2.
- C31, C32 - Add C31 to the lower right side of C3, add C32 to the lower left side of C3.
- C33, C34 - Add C33 to the lower left side of C27, add C34 to the lower right side of C27.
- C35, C36 - Add C35 to the upper right side of C26, add C36 to the upper left side of C36.

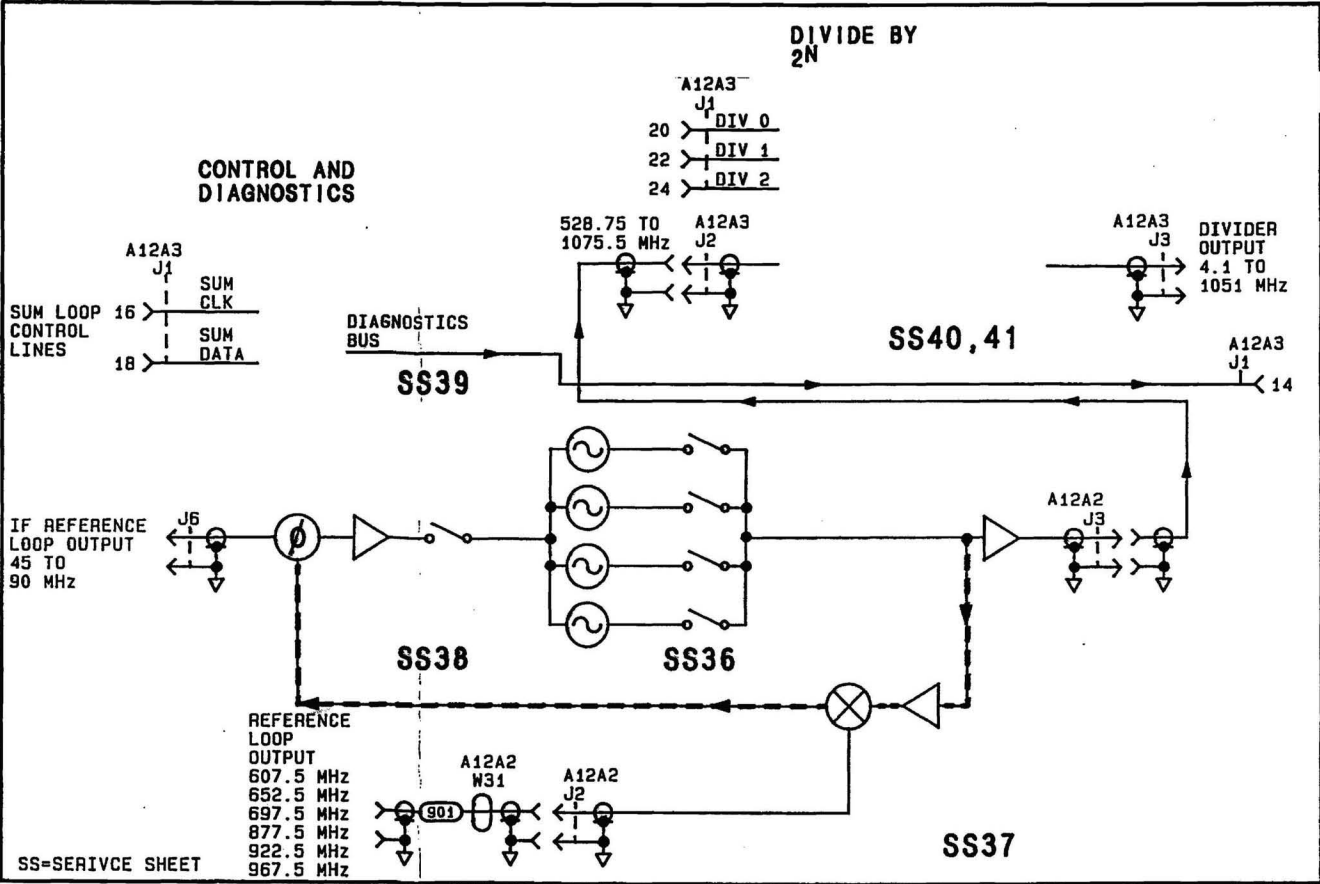
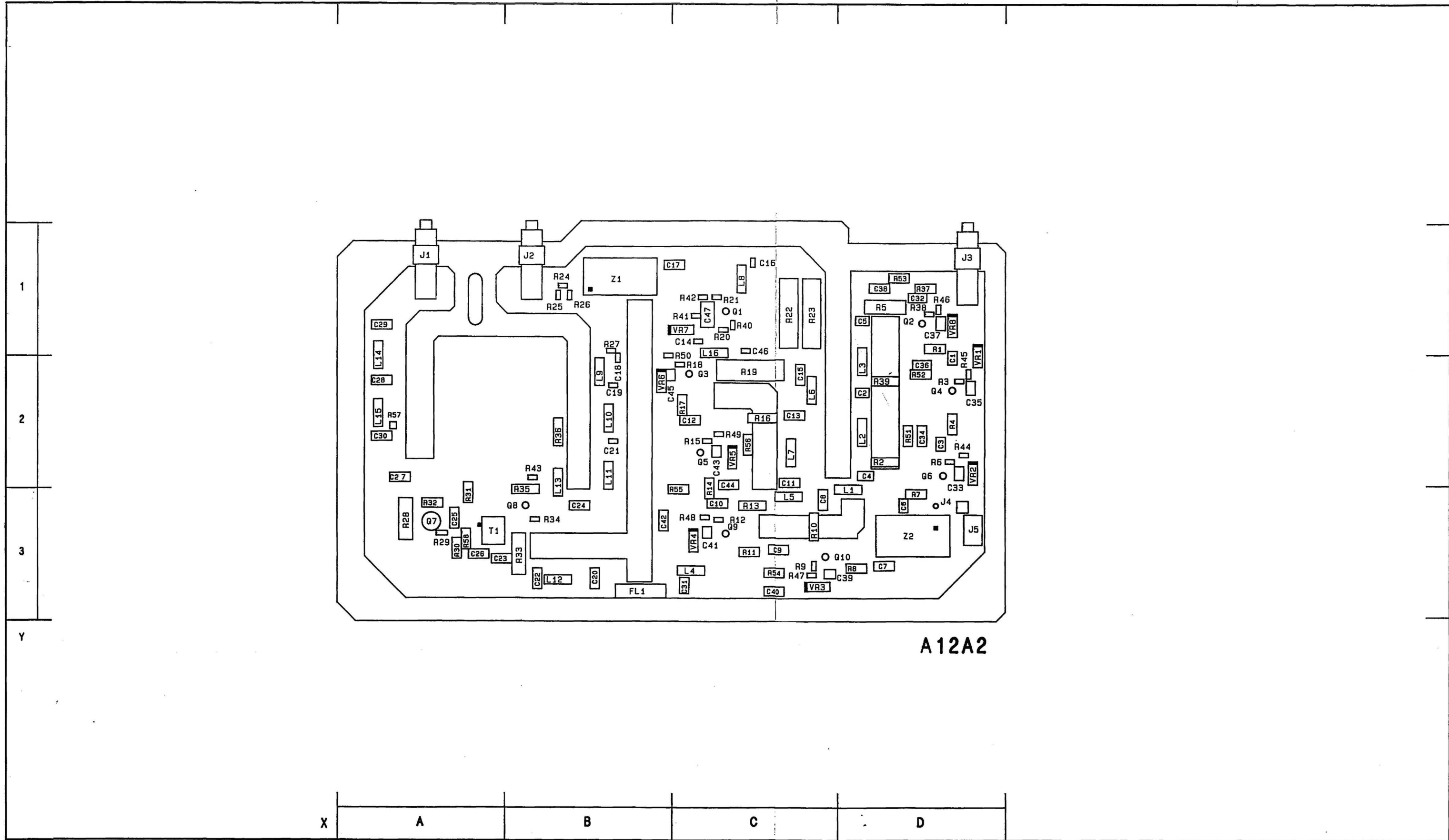
On the A12A1 schematic:

- C29, C30 - In **VCO BAND 1**, add C29 100p, in series with, and to the immediate left of C2, add C30 100p, in series with, and to the immediate right of C2.
- C31, C32 - In **VCO BAND 2**, add C31 100p, in series with, and to the immediate left of C3, add C32 100p, in series with, and to the immediate right of C3.
- C33, C34 - In **VCO BAND 3**, add C33 100p, in series with, and to the immediate left of C27, add C34 100p, in series with, and to the immediate right of C27.
- C35, C36 - In **VCO BAND 4**, add C35 100p, in series with, and to the immediate left of C26, add C36 100p, in series with, and to the immediate right of C26.

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**SCANS
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Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	D, 2	C38	D, 1	Q1	C, 1	R27	B, 1	VR1	D, 2								
C2	D, 2	C39	C, 3	Q2	D, 1	R28	A, 3	VR2	D, 2								
C3	D, 2	C40	C, 3	Q3	C, 2	R29	A, 3	VR3	C, 3								
C4	D, 2	C41	C, 3	Q4	D, 2	R30	A, 3	VR4	C, 3								
C5	D, 1	C42	B, 3	Q5	C, 2	R31	A, 3	VR5	C, 2								
C6	D, 3	C43	C, 2	Q6	D, 2	R32	A, 3	VR6	B, 2								
C7	D, 3	C44	C, 2	Q7	A, 3	R33	B, 3	VR7	C, 1								
C8	C, 3	C45	B, 2	Q8	B, 3	R34	B, 3	VR8	D, 1								
C9	C, 3	C46	C, 1	Q9	C, 3	R35	B, 2										
C10	C, 3	C47	C, 1	Q10	C, 3	R36	B, 2	Z1	B, 1								
C11	C, 2					R37	D, 1	Z2	D, 3								
C12	C, 2	FL1	B, 3	R1	D, 1	R38	D, 1										
C13	C, 2			R2	D, 2	R39	D, 2										
C14	C, 1	J1	A, 1	R3	D, 2	R40	C, 1										
C15	C, 2	J2	B, 1	R4	D, 2	R41	C, 1										
C16	C, 2	J3	D, 1	R5	D, 1	R42	C, 1										
C17	C, 1	J4	D, 3	R6	D, 2	R43	B, 2										
C18	B, 2	J5	D, 3	R7	D, 3	R44	D, 2										
C19	B, 2			R8	D, 3	R45	D, 2										
C20	B, 2	L1	D, 2	R9	C, 3	R46	D, 1										
C21	B, 2	L2	D, 2	R10	C, 3	R47	C, 3										
C22	B, 3	L3	D, 1	R11	C, 3	R48	C, 3										
C23	A, 3	L4	C, 3	R12	C, 3	R49	C, 2										
C24	A, 3	L5	C, 3	R13	C, 3	R50	B, 1										
C25	A, 3	L6	C, 2	R14	C, 2	R51	D, 2										
C26	A, 3	L7	C, 2	R15	D, 2	R52	D, 2										
C27	A, 2	L8	C, 1	R16	C, 2	R53	D, 1										
C28	A, 2	L9	B, 2	R17	C, 2	R54	C, 3										
C29	A, 1	L10	B, 2	R18	C, 2	R55	C, 3										
C30	A, 2	L11	B, 2	R19	C, 2	R56	C, 2										
C31	C, 3	L12	B, 2	R20	C, 1	R57	A, 3										
C32	D, 1	L13	B, 2	R21	C, 1	R58	A, 3										
C33	D, 2	L14	A, 2	R22	C, 1	T1	A, 3										
C34	D, 2	L15	A, 2	R23	C, 1												
C35	D, 2	L16	C, 1	R24	B, 1												
C36	D, 2			R25	B, 1												
C37	D, 1			R26	B, 1												

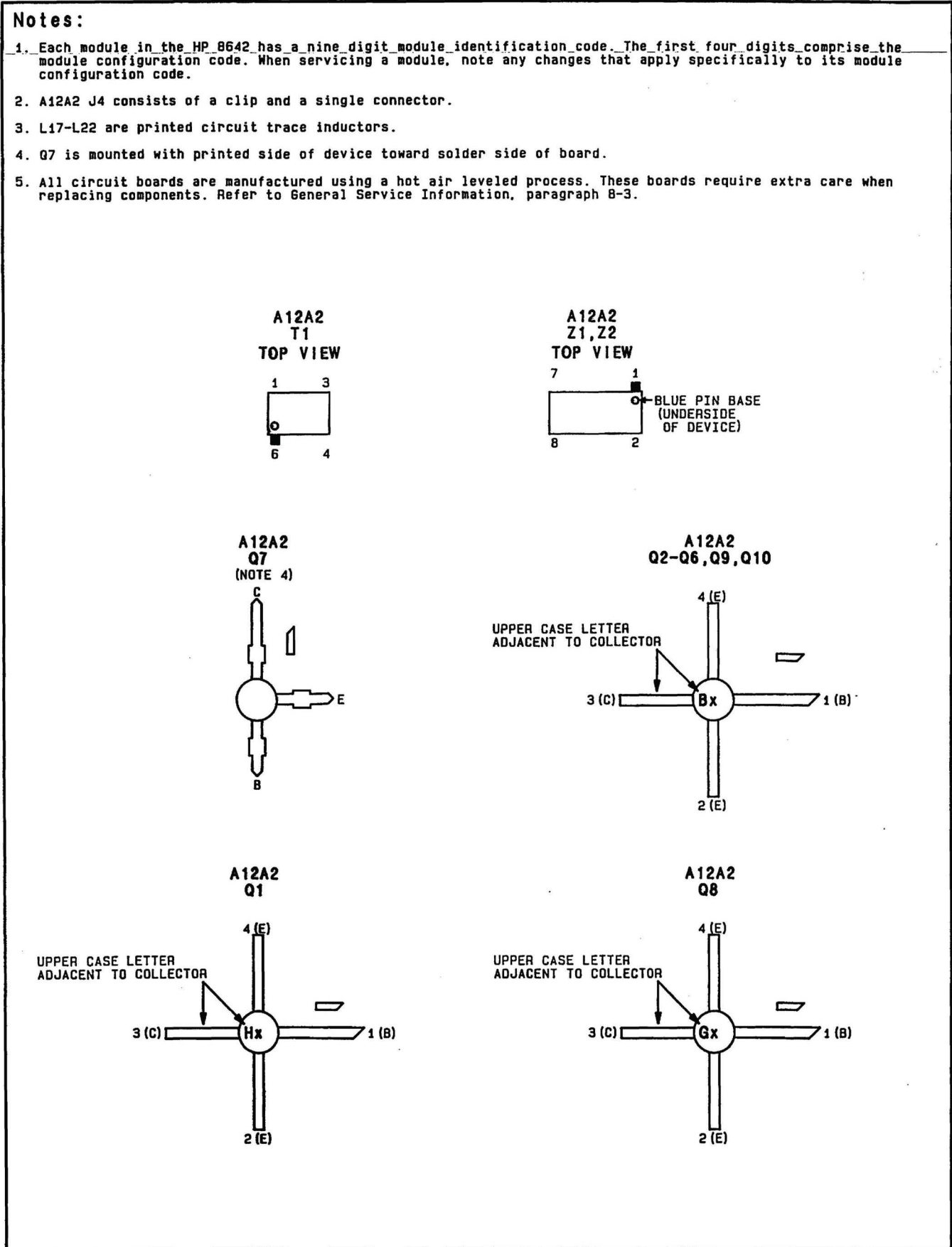


Figure 80-106 SERVICE SHEET 37 INFORMATION

Component Locator

A12A1 SUM LOOP V.C.O. ASSEMBLY SS36

CHANGES

2613A and above

On the schematic:

- In the upper left portion of the schematic change the A12 part number to 08642-60210.

CHANGES

All Serial Prefixes

On the schematic:

- In the lower right portion of the foldout, change the figure and page numbers for **SS40** to 8O-113.

2530A and above

On the Component Locator:

- R164, R165, R166, C145, C146, C147 - Replace the appropriate portion of the component locator with the partial on 8O-112.2

In Component Coordinates:

- Replace the Component Coordinates table with the one shown on page 8O-112.2

On the schematic:

- R103, R118, R146, R147, L112 - In **INPUT LIMITER**, change the value of R103 to 100 ohms. Change the value of R146 and R147 to 261 ohms. In **BUFFER/LIMITER**, change the value of R118 to 100 ohms. Change W101 symbol to an inductor. Label it L112, and assign it a value of 18n.
- R164, R165, R166, C145, C146, C147 - Replace the appropriate portion of **SS40** with the schematic partial on 8O-112.4

2543A and above

On the Component Locator:

- Replace the partial Component Locator shown on page 8O-112.2 with the partial on 8O-112.3

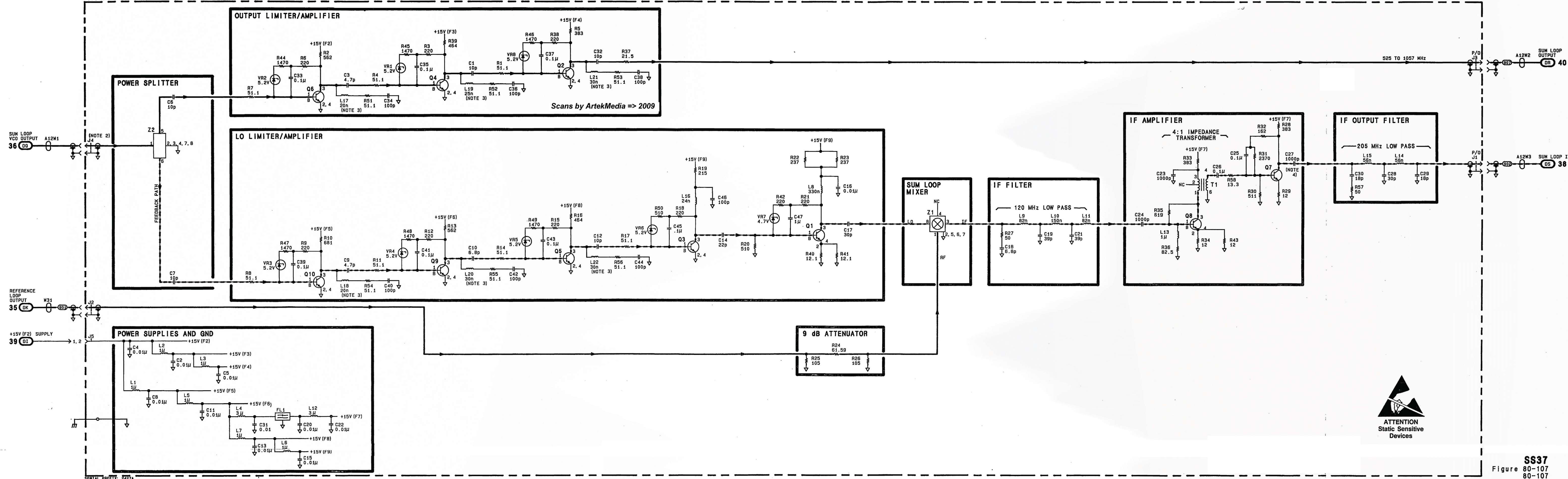
In Component Coordinates:

- Replace the Component Coordinates table on 8O-112.2 with the table on 8O-112.3

On the schematic:

- C133, C135, L111, R103, R147, L102, R118 - Replace the appropriate portion of **SS40** with the schematic partial on 8O-112.5. In **2N=0 DIVIDE**, change the value of L102 to 15u Farads. In **BUFFER/LIMITER**, change the value of R118 to 121 ohms. Note selection procedure for R147 in the table below.

A12A2 SUM LOOP POWER SPLITTER ASSEMBLY (08642-60110)



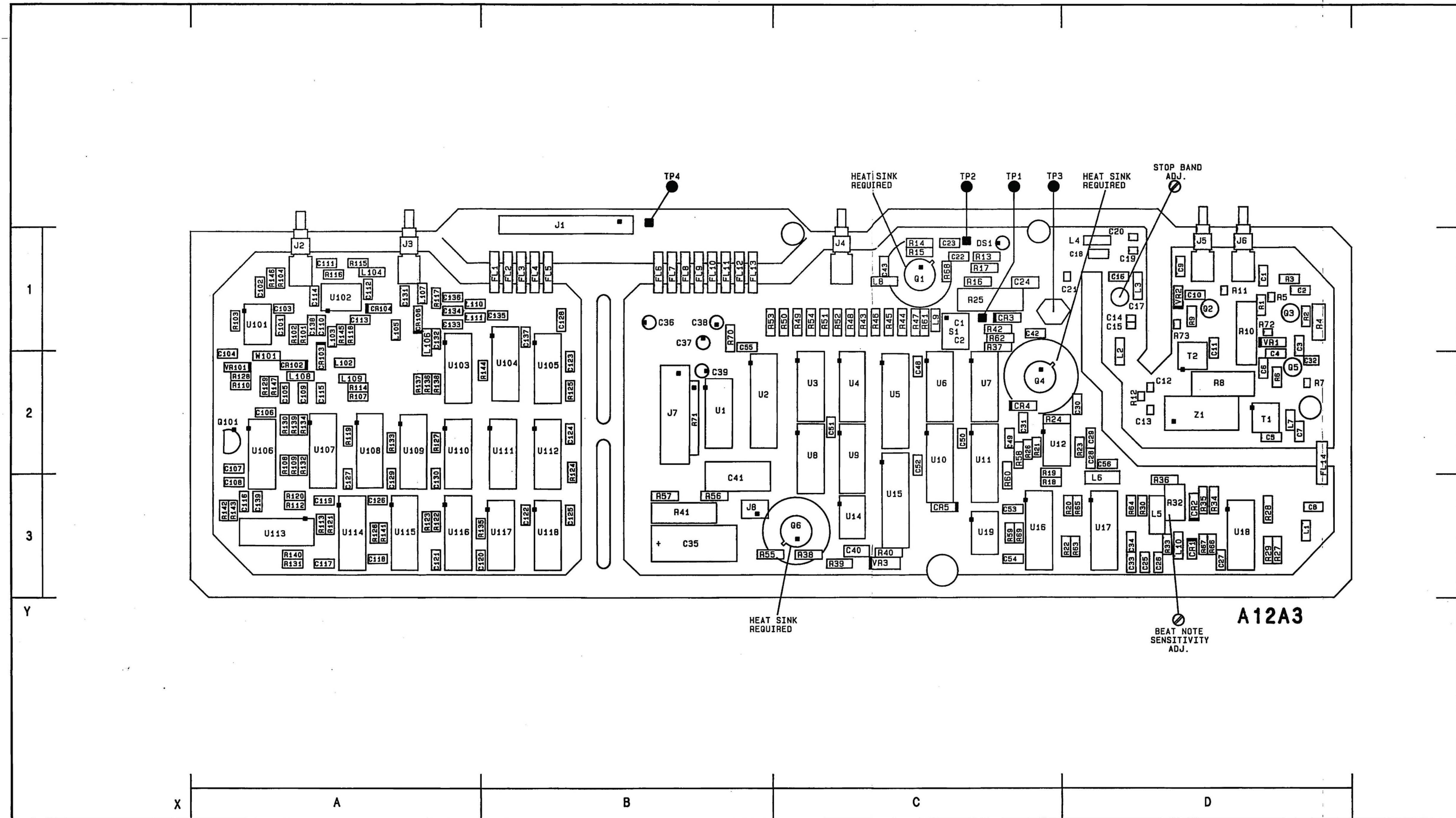
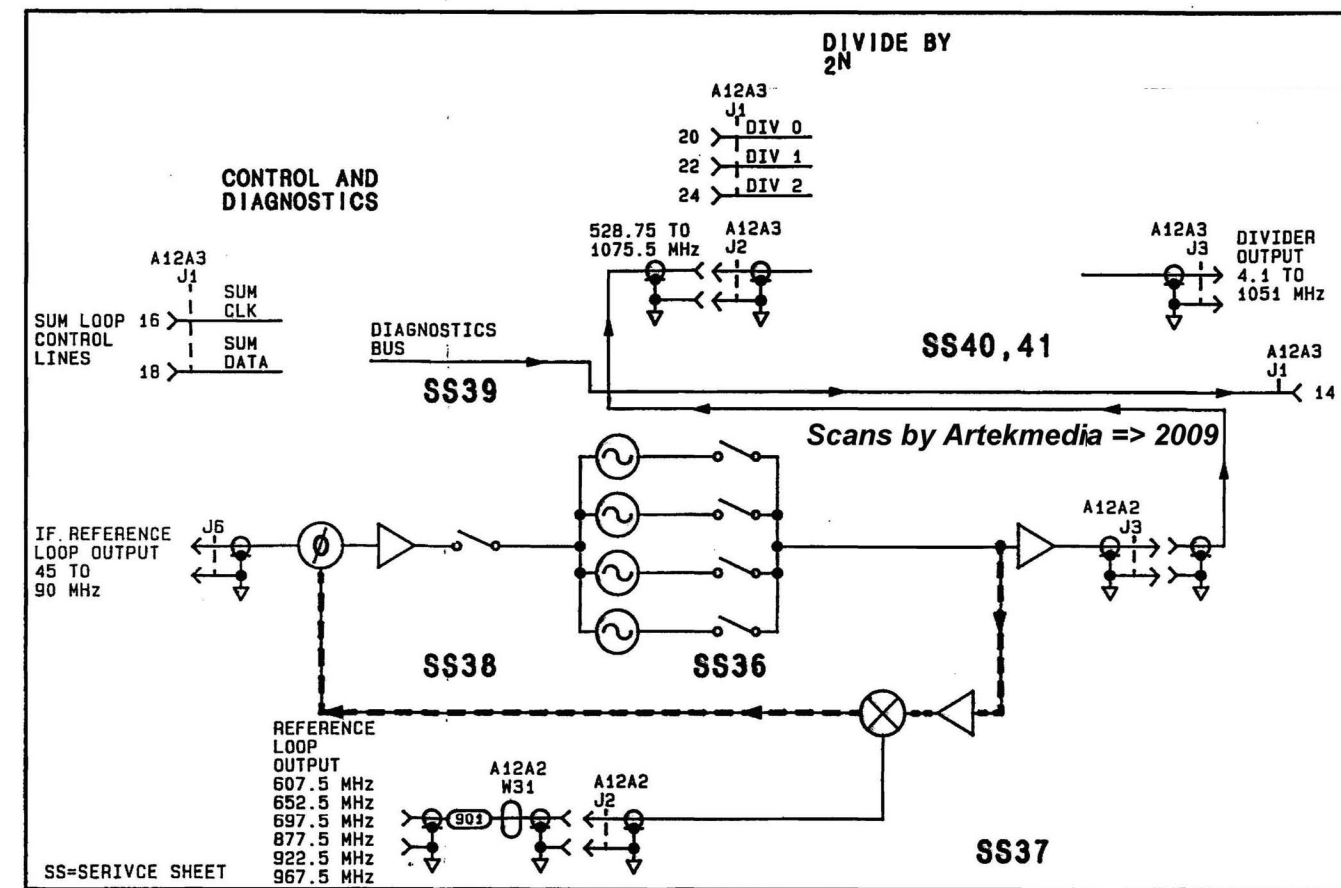


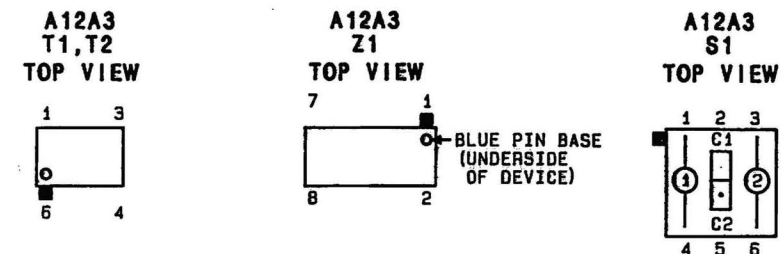
Figure 80-108. SERVICE SHEET 38 INFORMATION

COMPONENT LOCATOR

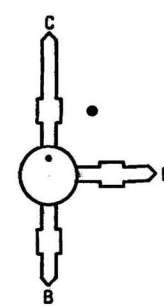


A12A2 SUM LOOP POWER SPLITTER ASSEMBLY SS37

- Notes:
- Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
 - Q2, Q3, Q5 are mounted with printed side of device toward solder side of board.
 - Test point requires high impedance (500 Ω) probe. See Bench Service Kit (HP part number 11802A).
 - All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.



A12A3 Q2, Q3, Q5



Schematic General Information

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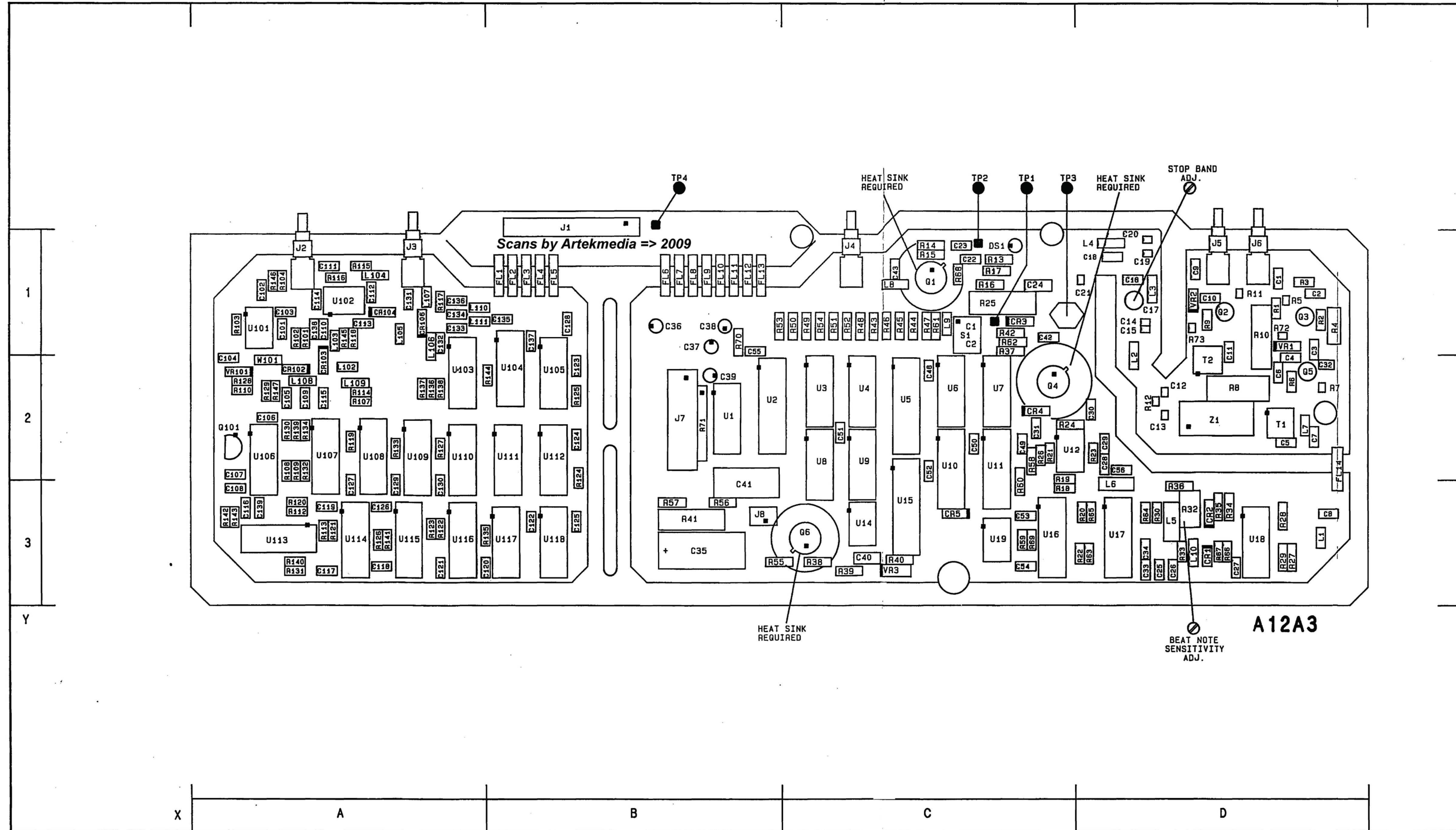
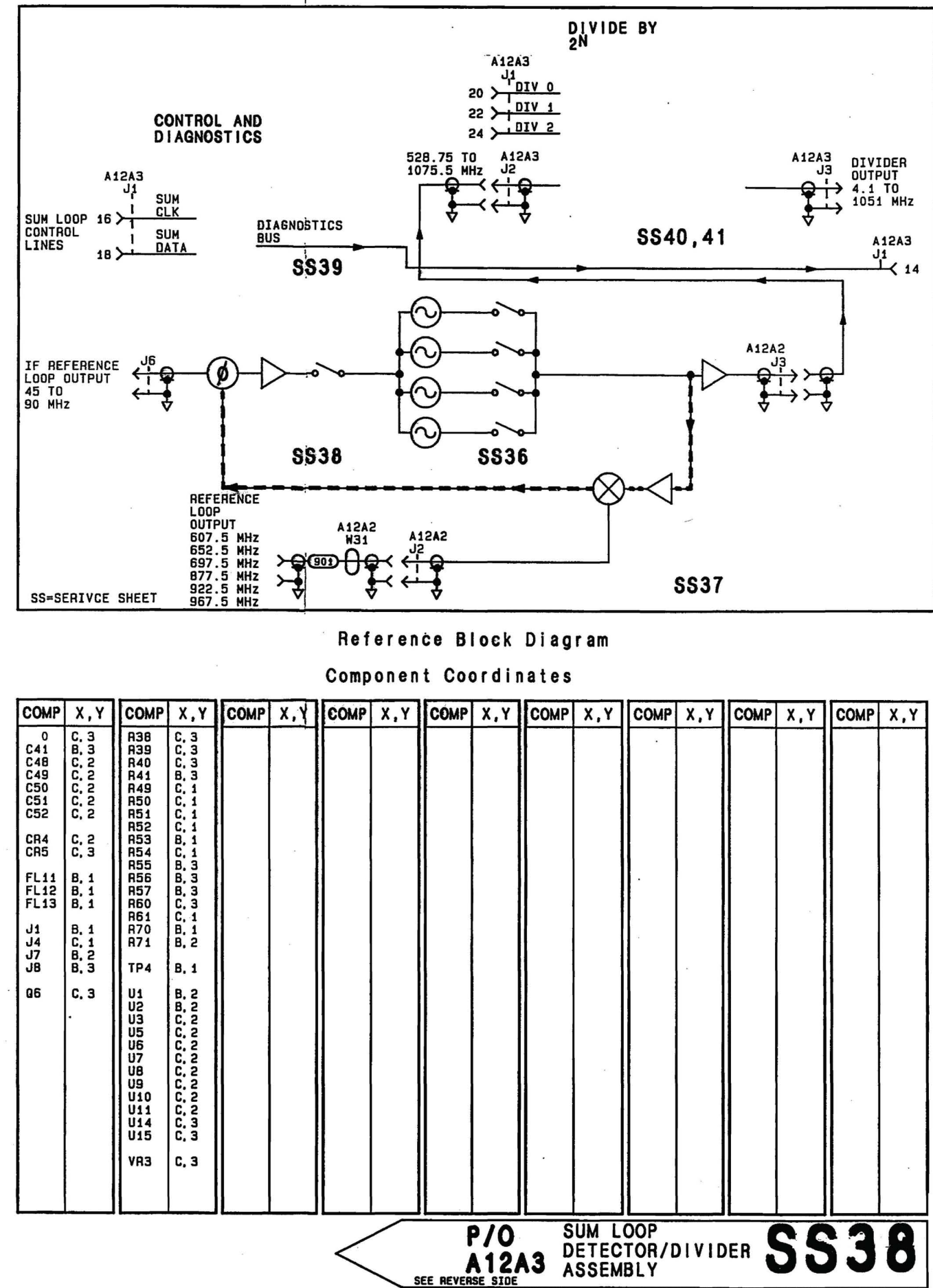


Figure 80-110. SERVICE SHEET 39 INFORMATION

Component Locator



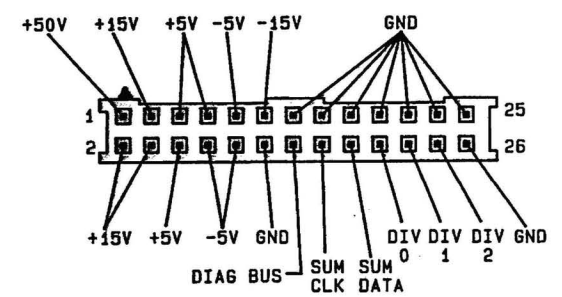
Service

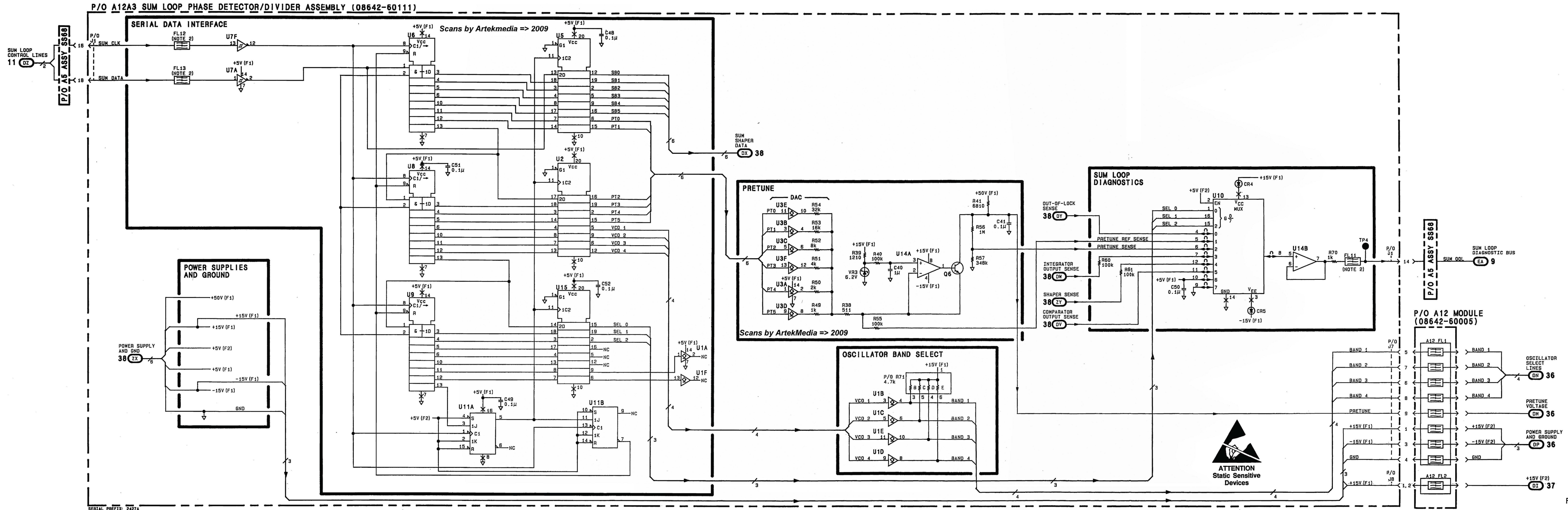
Model 8642A/B

Notes:

- Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- Feedthrough filter outer body must be soldered to the shielding in the area where shielding is notched.
- All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.

CABLE PLUG TO A12A3 J1





SS39
Figure 80-111
80-111

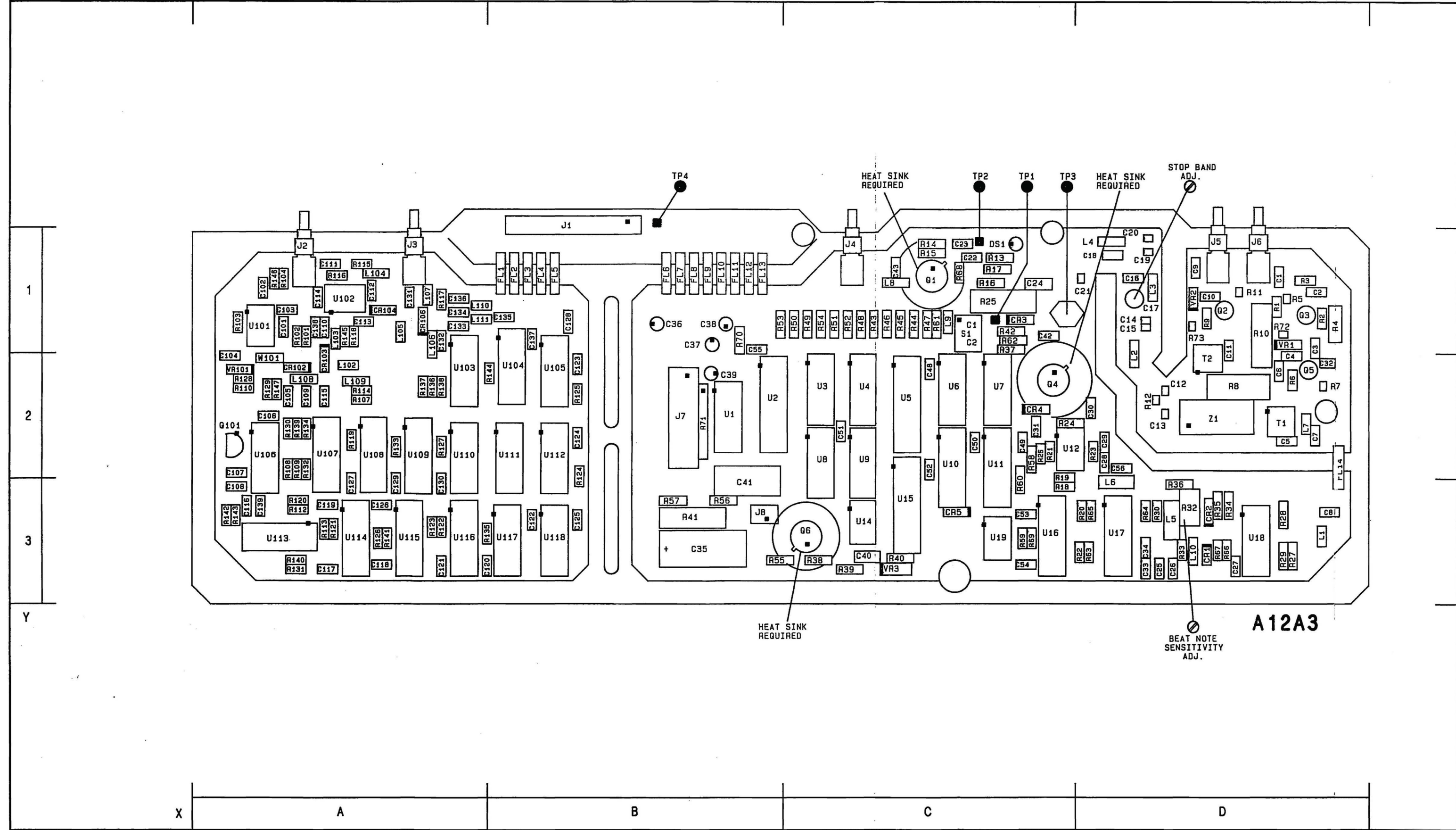
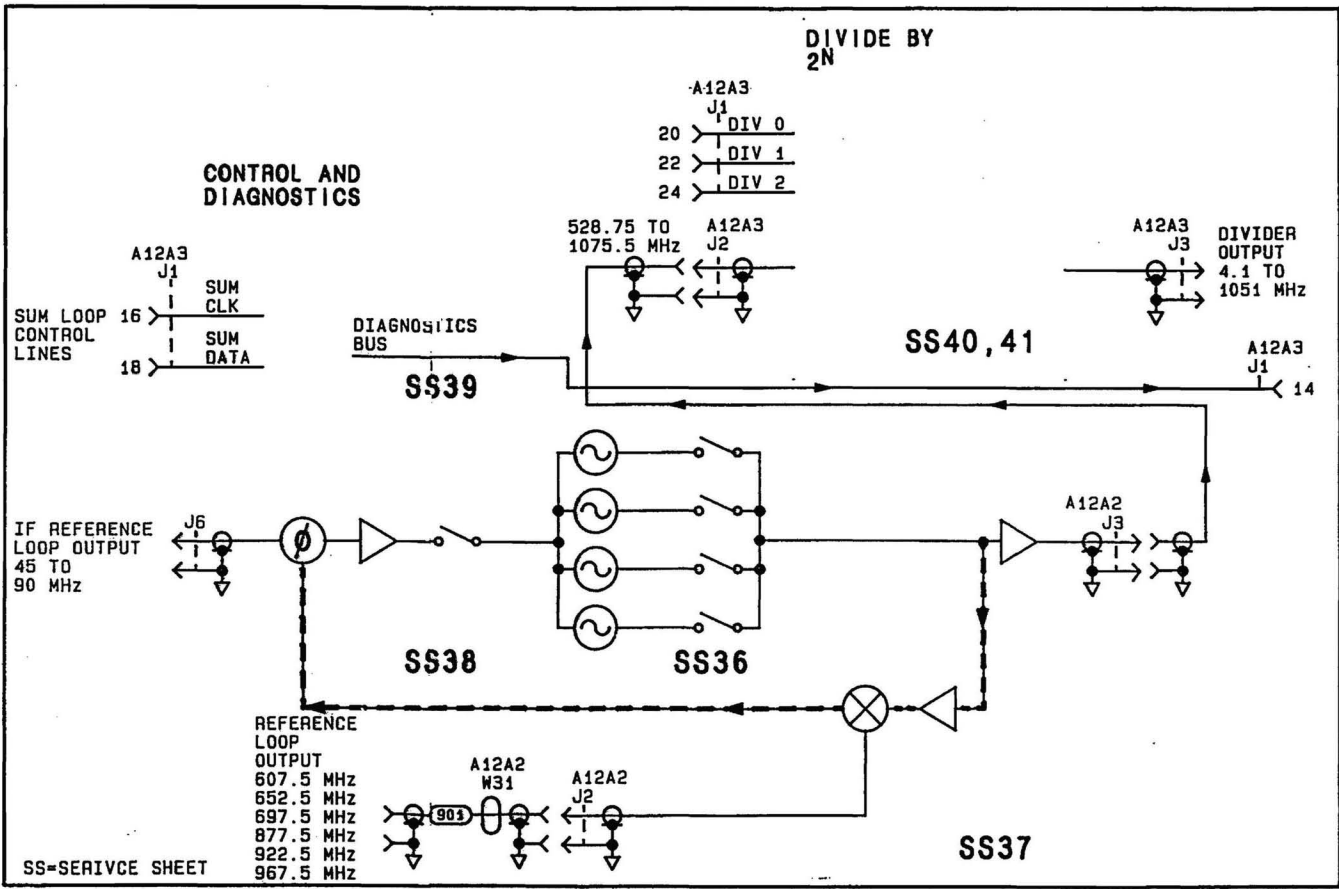


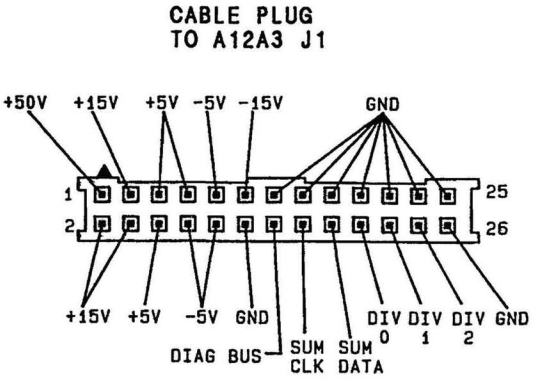
Figure 80-112. SERVICE SHEET 40 INFORMATION

Component Locator



P/O A12A3 SUM LOOP PHASE DETECTOR/DIVIDER ASSEMBLY **SS39**
SEE REVERSE SIDE

- Notes: Scans by Artekmedia => 2009
- Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
 - All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.



CHANGES

All Serial Prefixes

On the schematic:

- In the lower right portion of the foldout, change the figure and page numbers for **SS40** to 8O-113.

2530A and above

On the Component Locator:

- R164, R165, R166, C145, C146, C147 - Replace the appropriate portion of the component locator with the partial on 8O-112.2

In Component Coordinates:

- Replace the Component Coordinates table with the one shown on page 8O-112.2

On the schematic:

- R103, R118, R146, R147, L112 - In **INPUT LIMITER**, change the value of R103 to 100 ohms. Change the value of R146 and R147 to 261 ohms. In **BUFFER/LIMITER**, change the value of R118 to 100 ohms. Change W101 symbol to an inductor. Label it L112, and assign it a value of 18n.
- R164, R165, R166, C145, C146, C147 - Replace the appropriate portion of **SS40** with the schematic partial on 8O-112.4

2543A and above

On the Component Locator:

- Replace the partial Component Locator shown on page 8O-112.2 with the partial on 8O-112.3

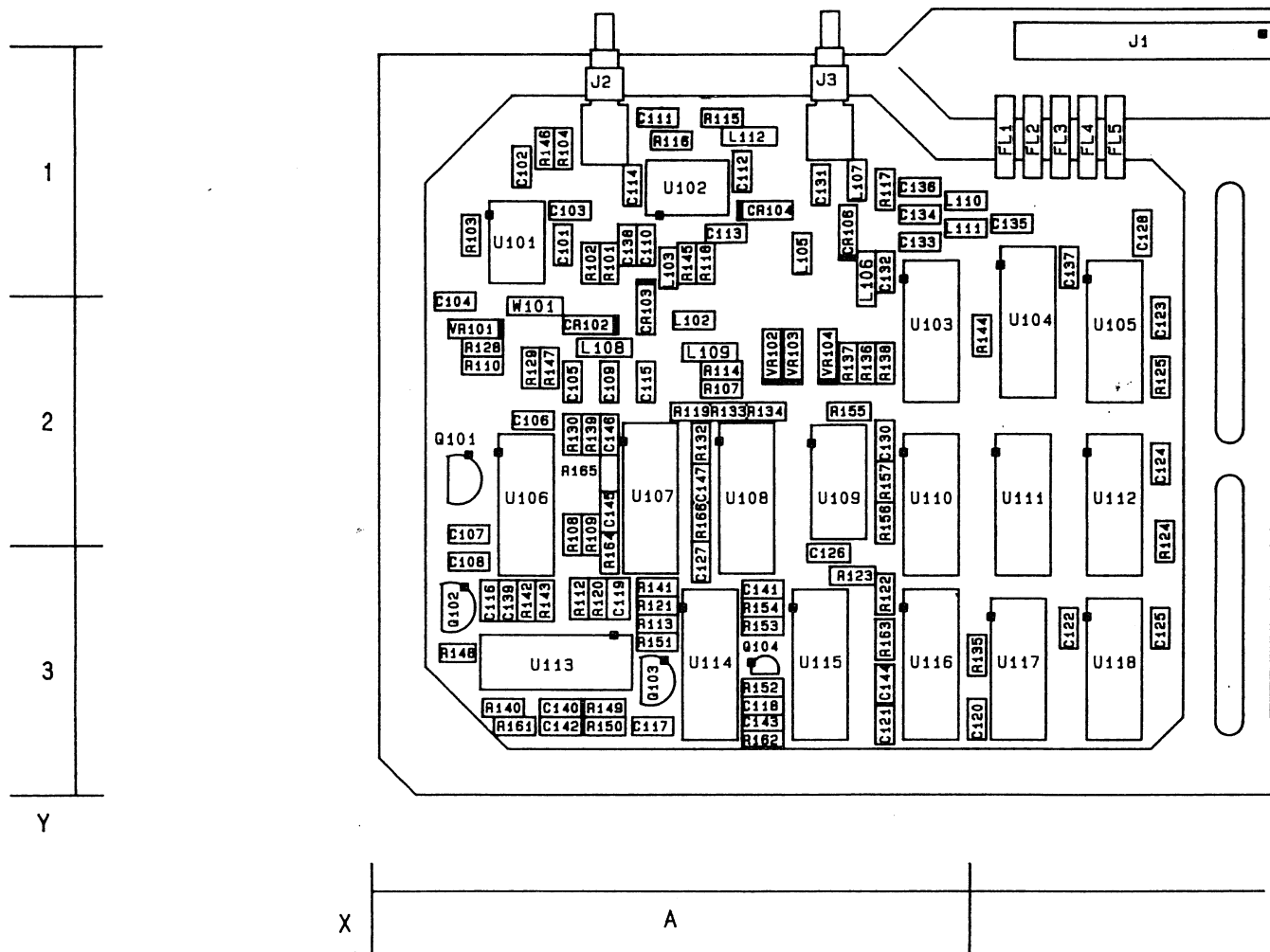
In Component Coordinates:

- Replace the Component Coordinates table on 8O-112.2 with the table on 8O-112.3

On the schematic:

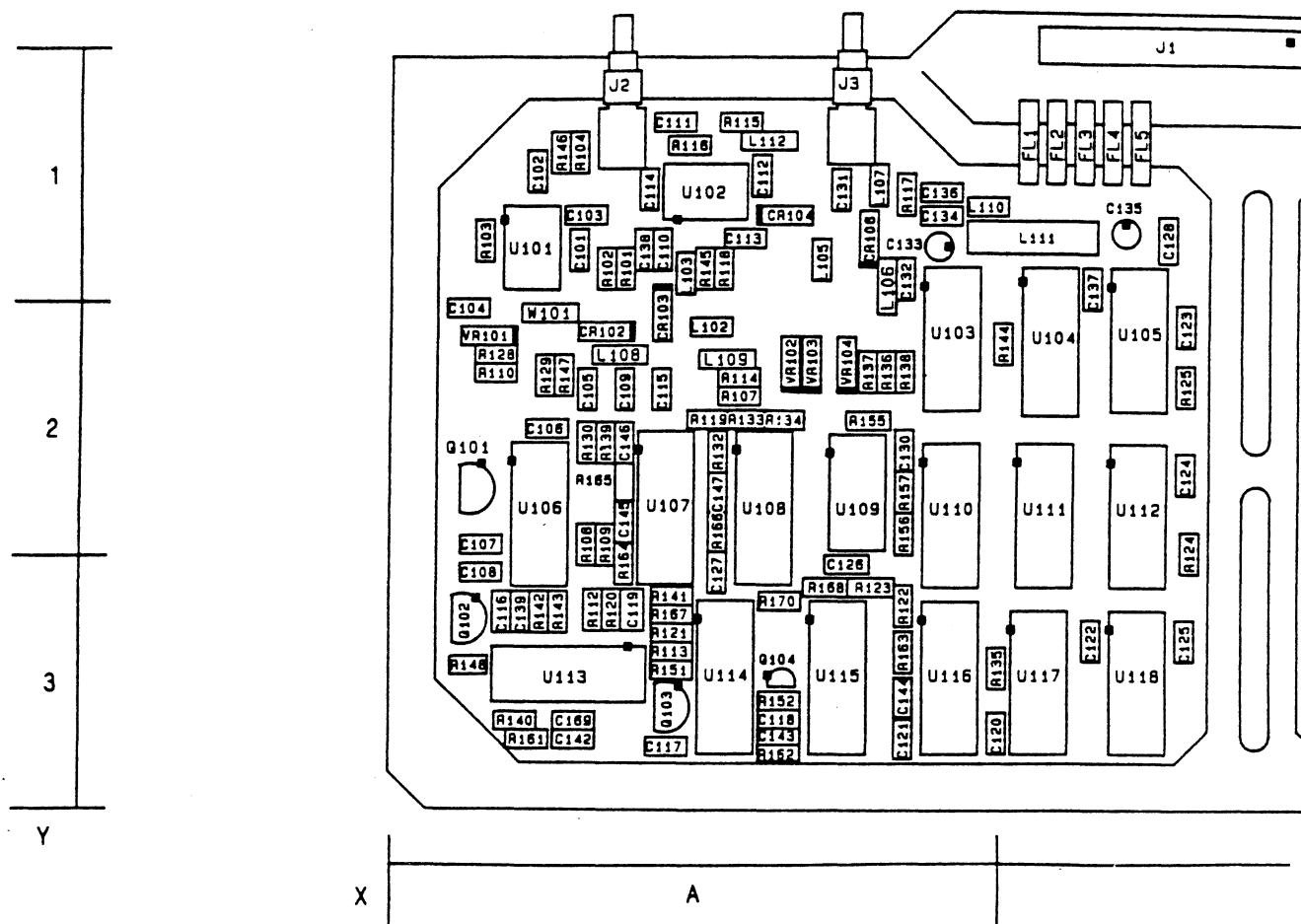
- C133, C135, L111, R103, R147, L102, R118 - Replace the appropriate portion of **SS40** with the schematic partial on 8O-112.5. In **2N=0 DIVIDE**, change the value of L102 to 15u Farads. In **BUFFER/LIMITER**, change the value of R118 to 121 ohms. Note selection procedure for R147 in the table below.

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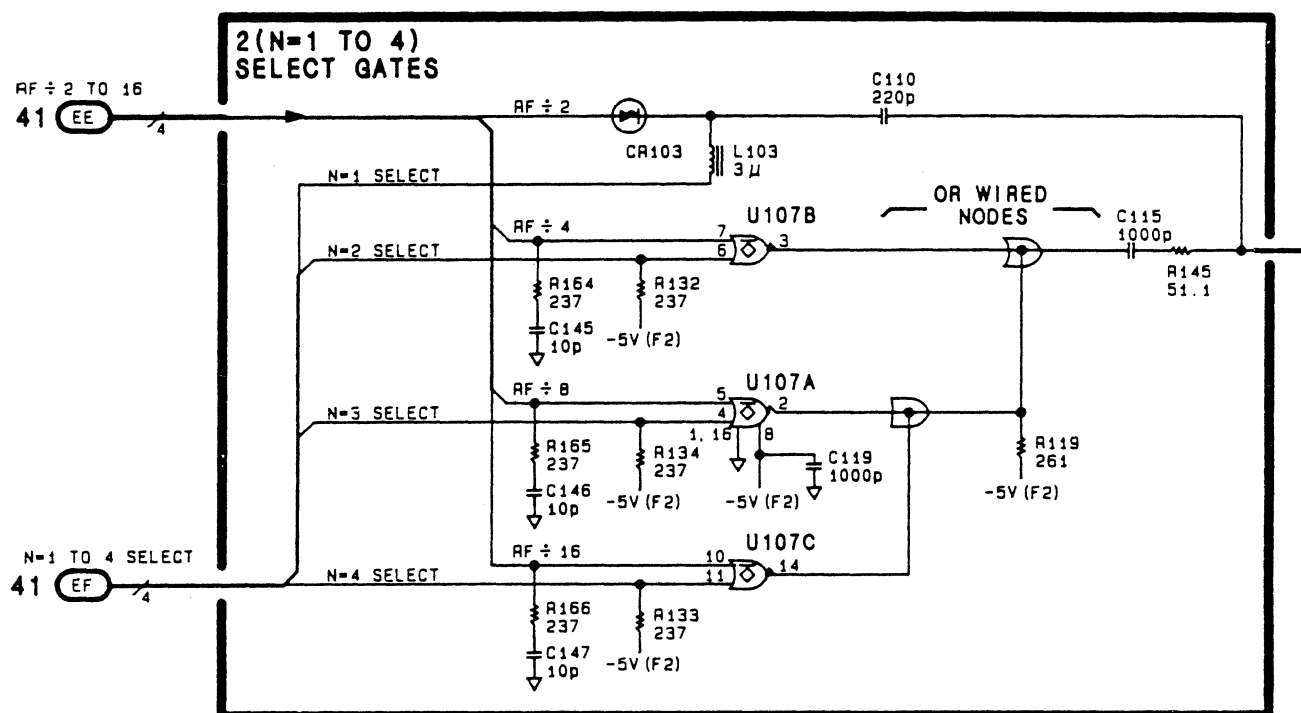
COMP	X, Y	COMP	X, Y	COMP	X, Y
C101	A, 1	L102	A, 2	U101	A, 1
C102	A, 1	L103	A, 1	U102	A, 1
C103	A, 1	L104	A, 1	U107	A, 2
C104	A, 2	L105	A, 1	U112	B, 2
C105	A, 2	L106	A, 1		
C110	A, 1	L107	A, 1		
C111	A, 1	L108	A, 2		
C112	A, 1	L110	A, 1		
C113	A, 1	L111	A, 1		
C114	A, 1	L112	A, 1		
C115	A, 2				
C119	A, 3	R101	A, 1		
C123	B, 2	R102	A, 1		
C124	B, 2	R103	A, 1		
C131	A, 1	R104	A, 1		
C132	A, 1	R107	A, 2		
C133	A, 1	R115	A, 1		
C134	A, 1	R116	A, 1		
C135	B, 1	R117	A, 1		
C136	A, 1	R118	A, 1		
C138	A, 1	R119	A, 2		
C145	A, 2	R124	B, 2		
C146	A, 2	R125	B, 2		
C147	A, 2	R129	A, 2		
		R132	A, 2		
CR102	A, 2	R133	A, 2		
CR103	A, 2	R134	A, 2		
CR104	A, 1	R145	A, 1		
CR106	A, 1	R146	A, 1		
		R147	A, 2		
FL1	B, 1	R164	A, 3		
FL2	B, 1	R165	A, 2		
		R166	A, 2		
J1	B, 1				
J2	A, 1				
J3	A, 1				

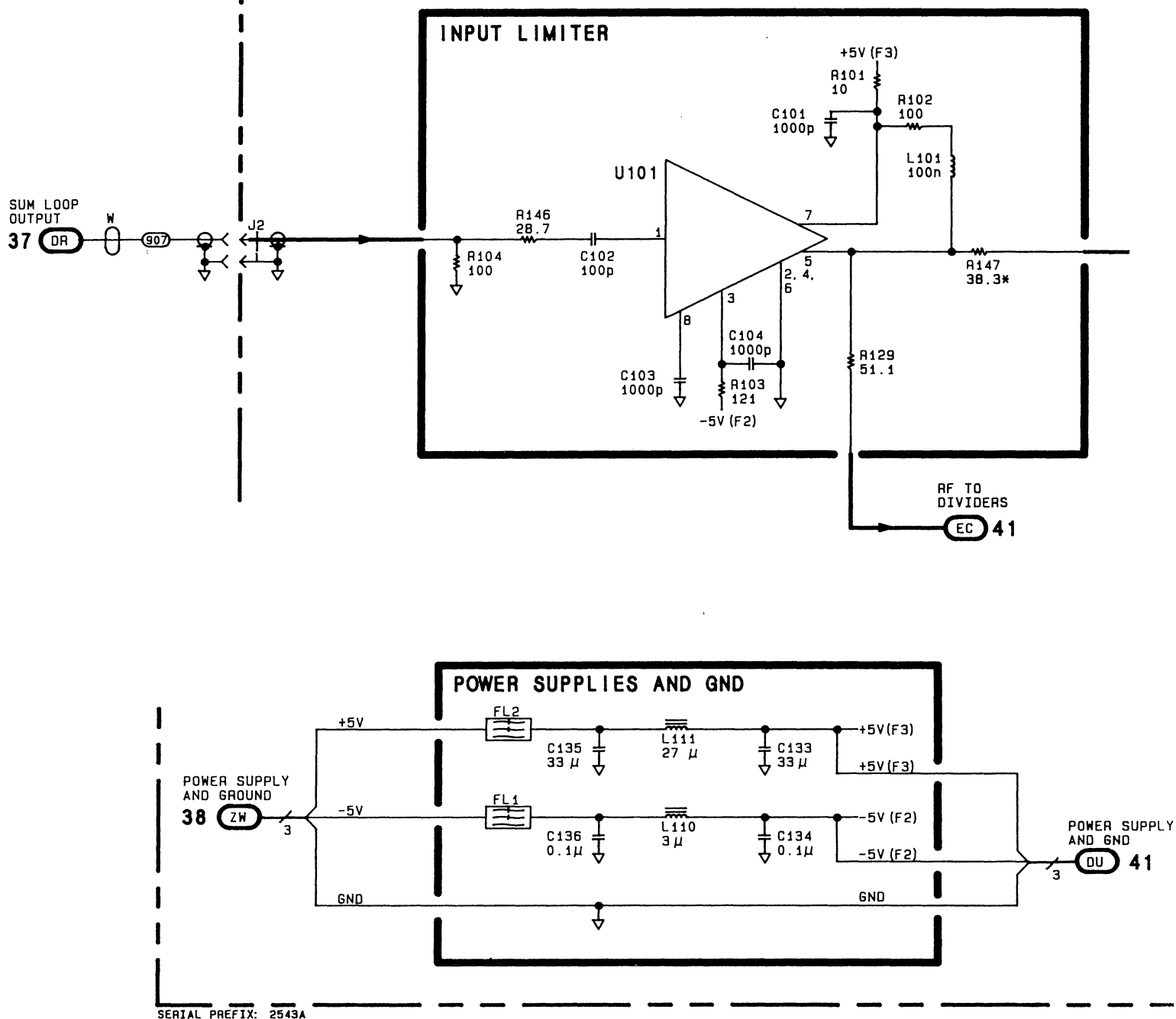
CHANGES TO FIGURE 80-112 (2530A to 2542A)



COMP	X, Y	COMP	X, Y	COMP	X, Y
C101	A. 1	L102	A. 2	U101	A. 1
C102	A. 1	L103	A. 1	U102	A. 1
C103	A. 1	L104	A. 1	U107	A. 2
C104	A. 2	L105	A. 1	U112	B. 2
C105	A. 2	L106	A. 1		
C110	A. 1	L107	A. 1		
C111	A. 1	L108	A. 2		
C112	A. 1	L110	A. 1		
C113	A. 1	L111	A. 1		
C114	A. 1	L112	A. 1		
C115	A. 2				
C119	A. 3	R101	A. 1		
C123	B. 2	R102	A. 1		
C124	B. 2	R103	A. 1		
C131	A. 1	R104	A. 1		
C132	A. 1	R107	A. 2		
C133	A. 1	R115	A. 1		
C134	A. 1	R116	A. 1		
C135	B. 1	R117	A. 1		
C136	A. 1	R118	A. 1		
C138	A. 1	R119	A. 2		
C145	A. 2	R124	B. 2		
C146	A. 2	R125	B. 2		
C147	A. 2	R129	A. 2		
		R132	A. 2		
CR102	A. 2	R133	A. 2		
CR103	A. 2	R134	A. 2		
CR104	A. 1	R145	A. 1		
CR106	A. 1	R146	A. 1		
		R147	A. 2		
FL1	B. 1	R164	A. 3		
FL2	B. 1	R165	A. 2		
J1	B. 1	R166	A. 2		
J2	A. 1				
J3	A. 1				

CHANGES TO FIGURE 80-112 (2543A and above)



P/O A12A3 SUM PHASE DETECTOR/DIVIDER ASSEMBLY (08642-60311)

CHANGES TO FIGURE 8O-113 (2543A and above)

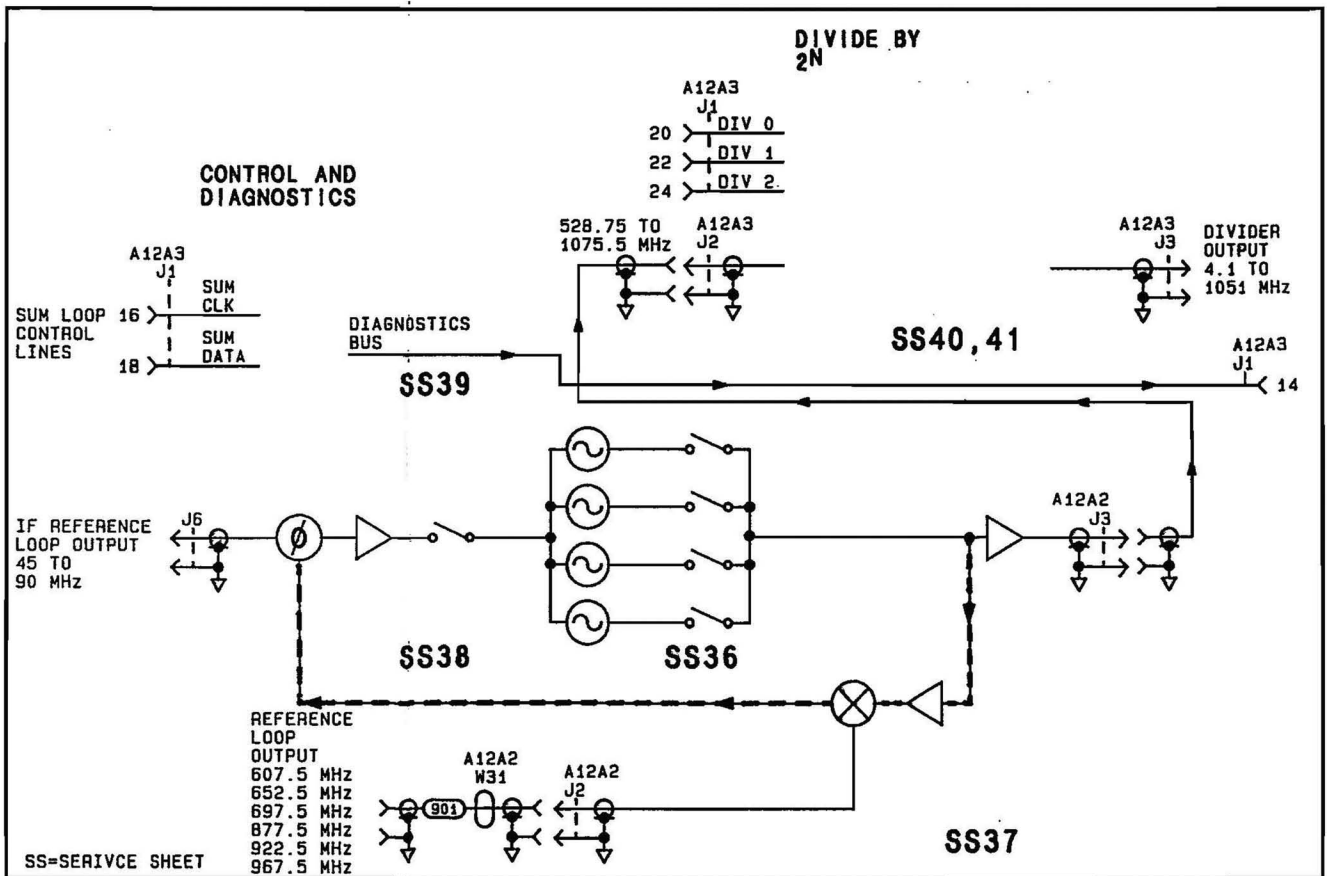
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Notes:

- Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph B-3.



P/O
A12A3
SUM LOOP PHASE
DETECTOR/DIVIDER
ASSEMBLY
SS40

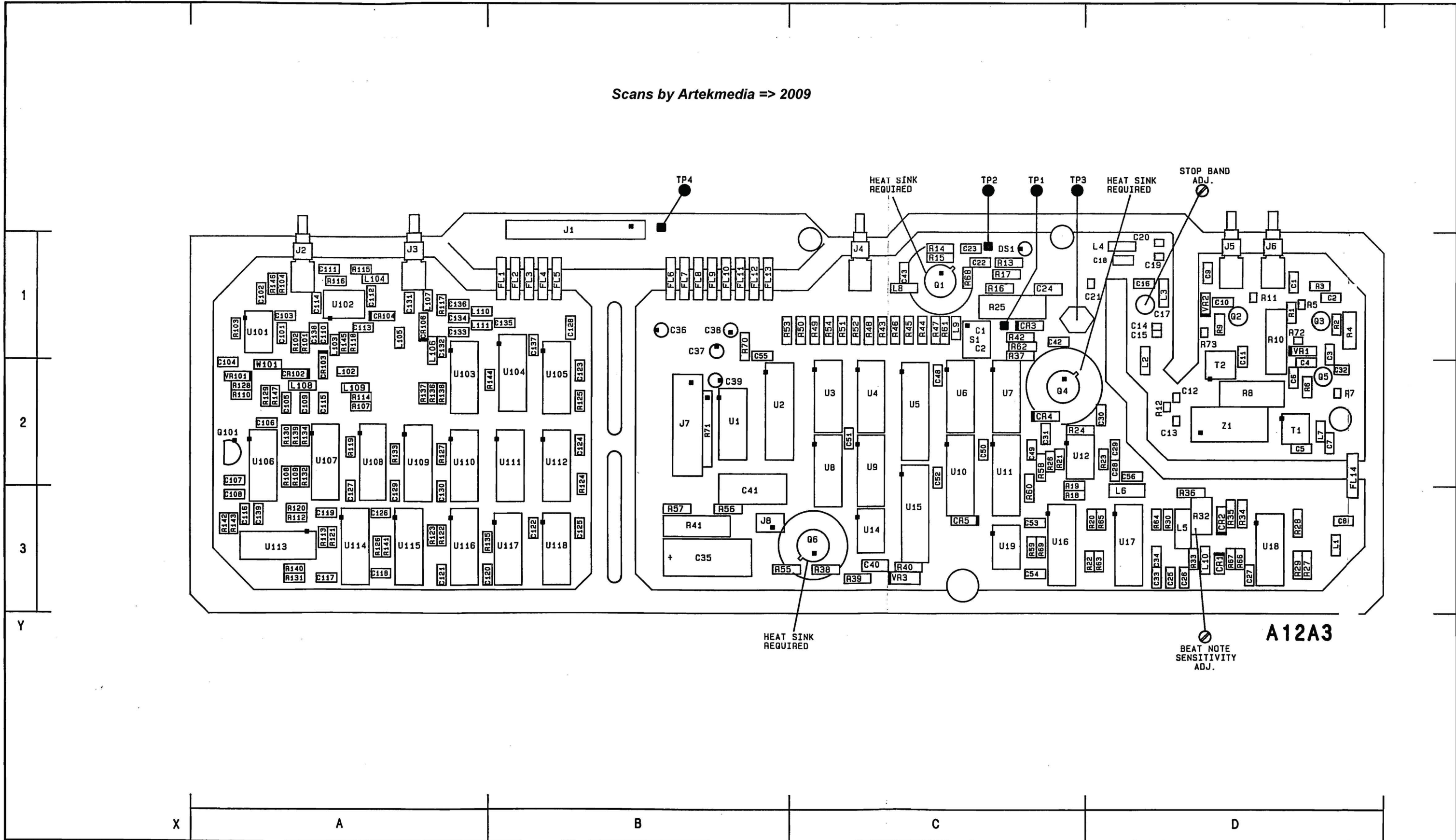


Figure 80-114. SERVICE SHEET 41 INFORMATION

Component Locator

Scans by Artekmedia => 2009

CHANGES**2427A to 2527A**

On the schematic:

- R131 - In $2^{N=2}$ **DIVIDE**, change R131 value to 261 ohms.
- U113, U114, U115 - In $2^{N=2}$ **DIVIDE**, extend pin 12 of U113 to connect with the node of R131 and U113 pin 9. Remove connection to pin 9 and label it NC. In $2^{N=3}$ **DIVIDE**, extend pin 12 of U114 to connect with the node of R126 and U114 pin 9. Remove connection to pin 9 and label it NC. In $2^{N=4}$ **DIVIDE**, extend pin 12 of U115 to connect with the node of R127 and U115 pin 9. Remove connection to pin 9 and label it NC.

2530A and above

On the Component Locator:

- C129, C140-147, Q102-104, R108-R110, R126-R128, R131-R134, R138, R140-R143, R148-R166, VR102-VR104 - Replace appropriate portion of the component locator with the partial on 8O-114.3

In Component Coordinates:

- Replace Component Coordinates table with the one shown on page 8O-114.3

On the schematic:

- C129, C140-C147, Q102-Q104, R108-R110, R126-R128, R131-R134, R138, R140-R143, R148-R166, VR102-VR104 - Replace **SS41** with the foldout on page 8O-114.5

2543A and above

On the Component Locator:

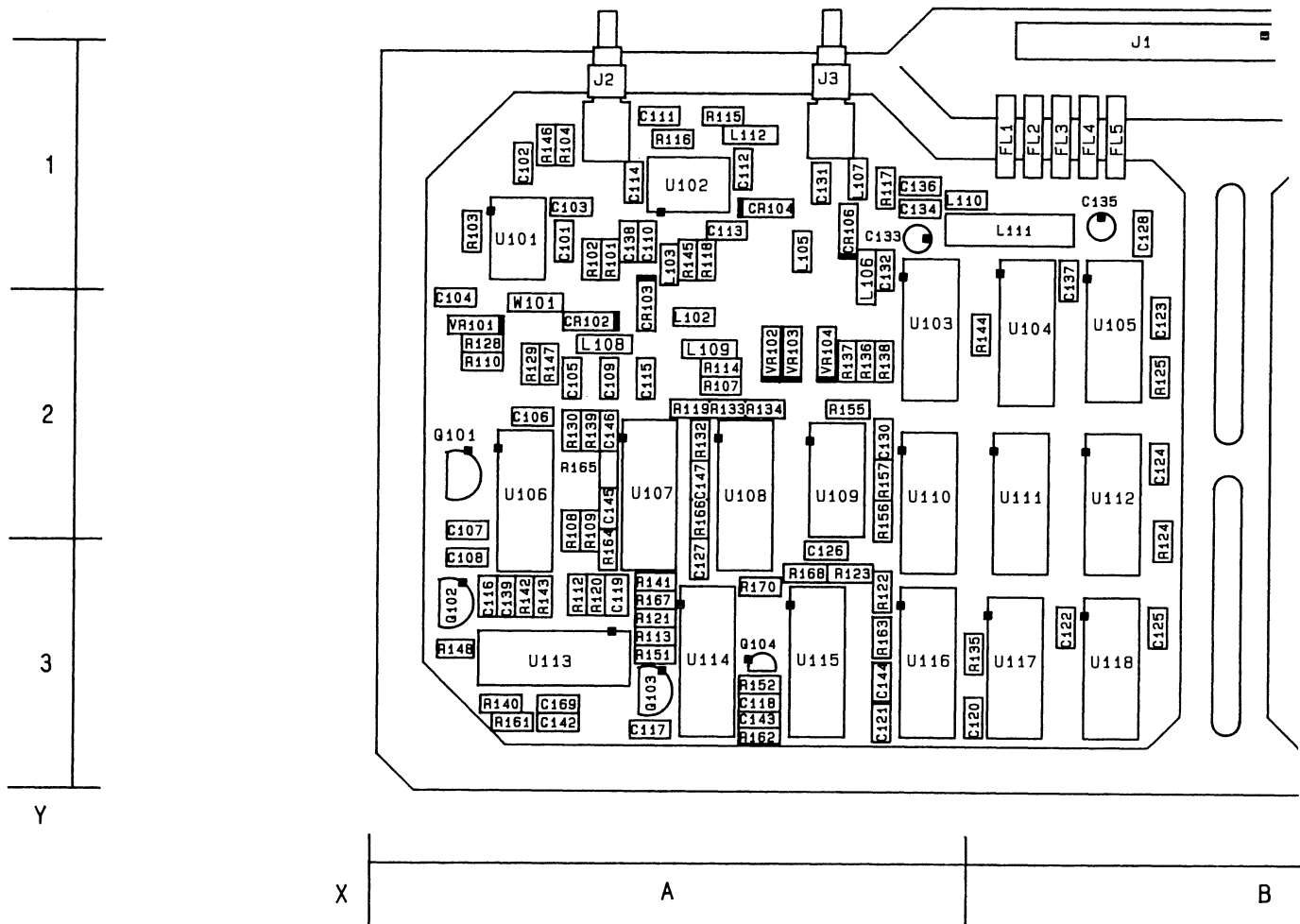
- R167, R168, R169, R170 - Replace the appropriate portion of the component locator with the partial on 8O-114.2

In Component Coordinates:

- Replace the Component Coordinates table with the one shown on page 8O-114.2

On the schematic:

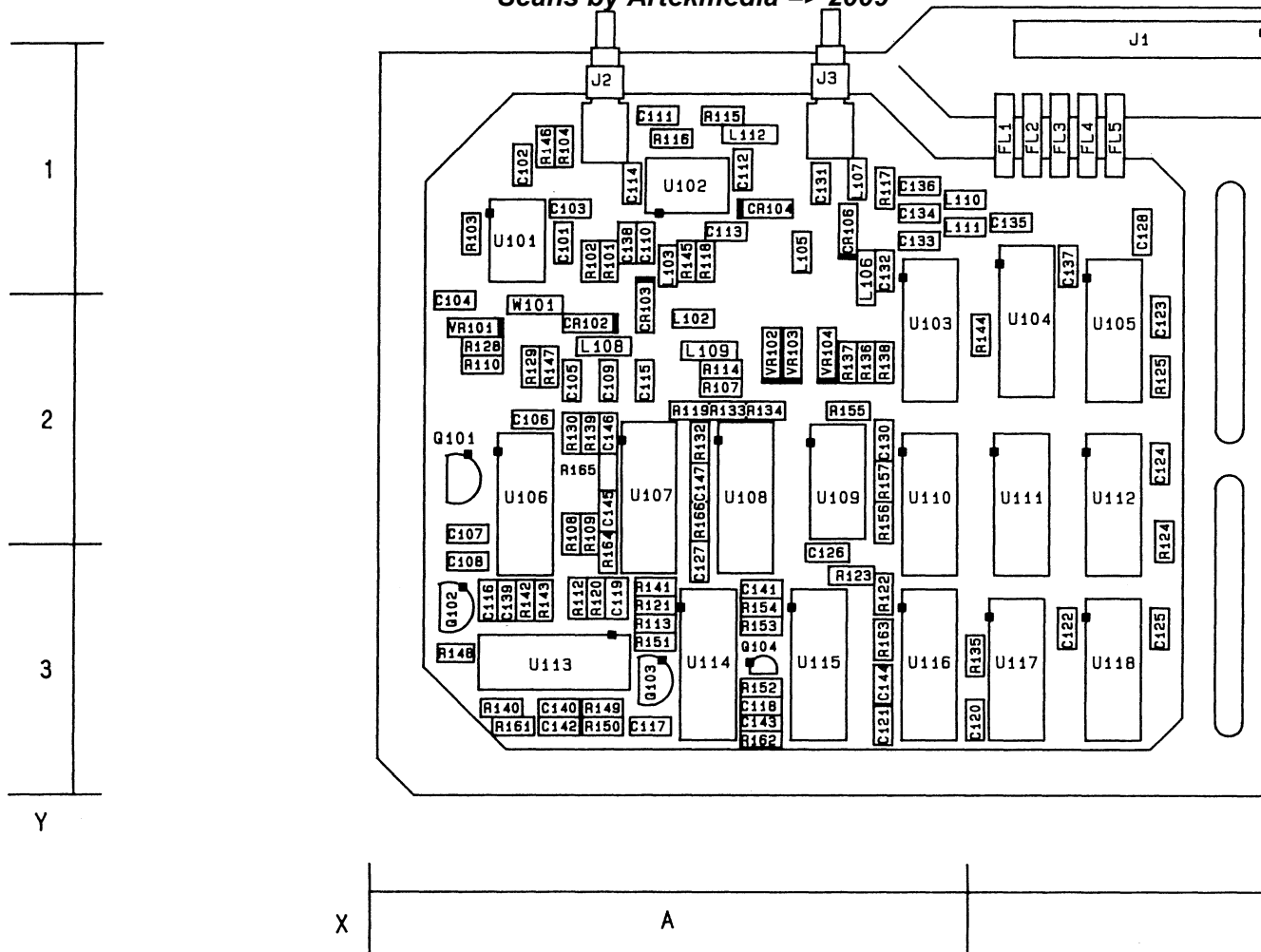
- C140, C141, R167, R168, R169, R170 - Replace the appropriate portion of Figure 8O-114.5 (page 8O-114.5), with the schematic partial on page 8O-114.4. Change the assembly part number from 08642-60211, to 08642-60311.



COMP	X, Y	COMP	X, Y	COMP	X, Y
C106	A, 2	R108	A, 2	U103	A, 2
C107	A, 2	R109	A, 2	U104	B, 2
C108	A, 3	R110	A, 2	U105	B, 2
C109	A, 2	R111	A, 3	U106	A, 2
C116	A, 3	R112	A, 3	U108	A, 2
C117	A, 3	R113	A, 3	U109	A, 2
C118	A, 3	R114	A, 2	U110	A, 2
C120	A, 3	R120	A, 3	U111	B, 2
C121	A, 3	R121	A, 3	U113	A, 3
C122	B, 3	R122	A, 3	U114	A, 3
C125	B, 3	R123	A, 3	U115	A, 3
C126	A, 3	R130	A, 2	U116	A, 3
C127	A, 3	R135	A, 3	U117	B, 3
C128	B, 1	R136	A, 2	U118	B, 3
C130	A, 3	R137	A, 2		
C137	B, 1	R138	A, 2		
C139	A, 3	R139	A, 2	VR101	A, 2
C142	A, 3	R140	A, 3	VR102	A, 2
C143	A, 3	R141	A, 3	VR103	A, 2
C144	A, 3	R142	A, 3	VR104	A, 2
		R143	A, 3		
		R144	A, 2		
FL3	B, 1	R148	A, 3		
FL4	B, 1	R151	A, 3		
FL5	B, 1	R152	A, 3		
		R155	A, 2		
J1	B, 1	R156	A, 2		
		R157	A, 2		
L109	A, 2	R161	A, 3		
		R162	A, 3		
Q101	A, 2	R163	A, 3		
Q102	A, 3	R167	A, 3		
Q103	A, 3	R168	A, 3		
Q104	A, 3	R169	A, 3		
		R170	A, 3		

CHANGES TO FIGURE 80-114 (2543A and above)

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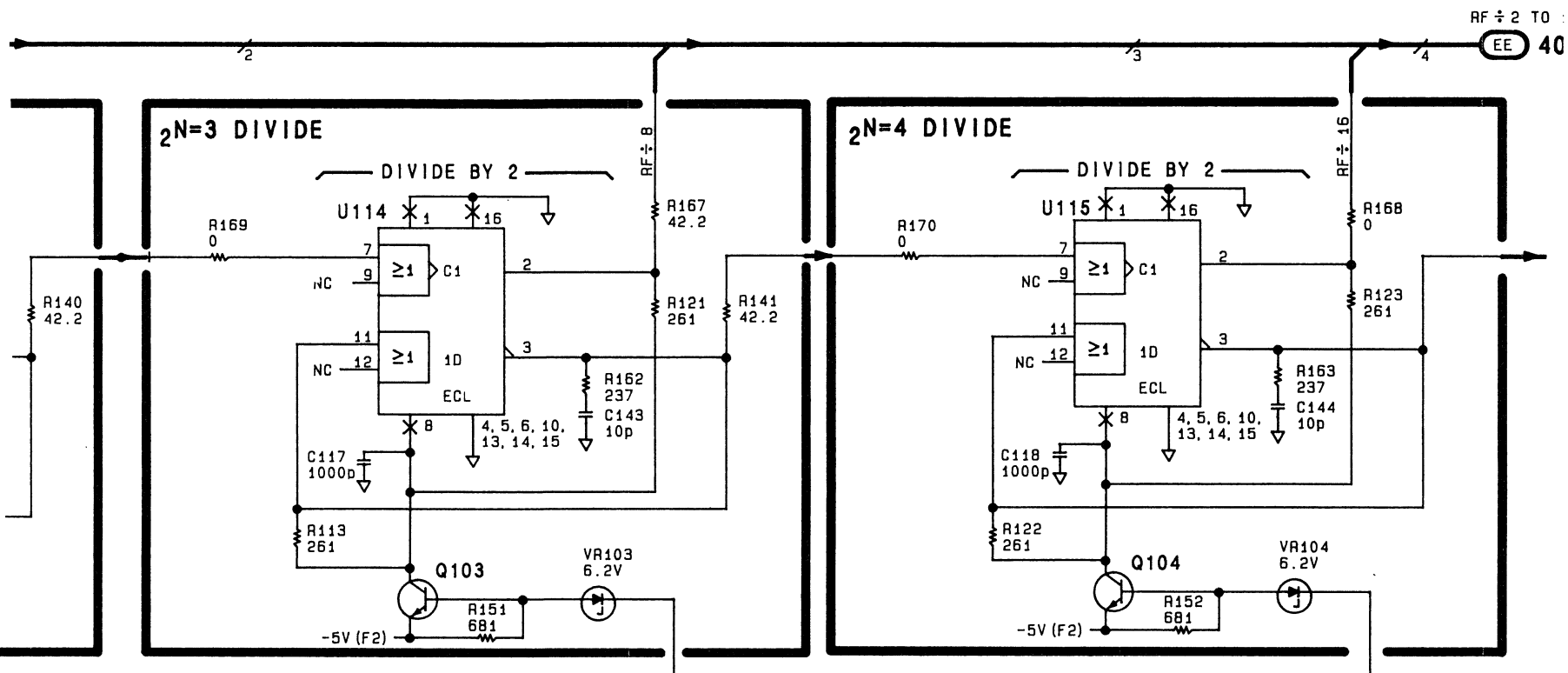


COMP	X, Y	COMP	X, Y	COMP	X, Y
C106	A, 2	R108	A, 2	U103	A, 2
C107	A, 2	R109	A, 2	U104	B, 2
C108	A, 3	R110	A, 2	U105	B, 2
C109	A, 2	R112	A, 3	U106	A, 2
C116	A, 3	R113	A, 3	U108	A, 2
C117	A, 3	R114	A, 2	U109	A, 2
C118	A, 3	R120	A, 3	U110	A, 2
C120	A, 3	R121	A, 3	U111	B, 2
C121	A, 3	R122	A, 3	U113	A, 3
C122	B, 3	R123	A, 3	U114	A, 3
C125	B, 3	R130	A, 2	U115	A, 3
C126	A, 3	R135	A, 3	U116	A, 3
C127	A, 3	R136	A, 2	U117	B, 3
C128	B, 1	R137	A, 2	U118	B, 3
C130	A, 3	R138	A, 2		
C137	B, 1	R139	A, 2	VR101	A, 2
C139	A, 3	R140	A, 3	VR102	A, 2
C140	A, 3	R141	A, 3	VR103	A, 2
C141	A, 3	R142	A, 3	VR104	A, 2
C142	A, 3	R143	A, 3		
C143	A, 3	R144	A, 2		
C144	A, 3	R148	A, 3		
		R149	A, 3		
FL3	B, 1	R150	A, 3		
FL4	B, 1	R151	A, 3		
FL5	B, 1	R152	A, 3		
J1	B, 1	R153	A, 3		
L109	A, 2	R154	A, 3		
Q101	A, 2	R155	A, 2		
Q102	A, 3	R156	A, 2		
Q103	A, 3	R157	A, 2		
Q104	A, 3	R161	A, 3		
		R162	A, 3		
		R163	A, 3		

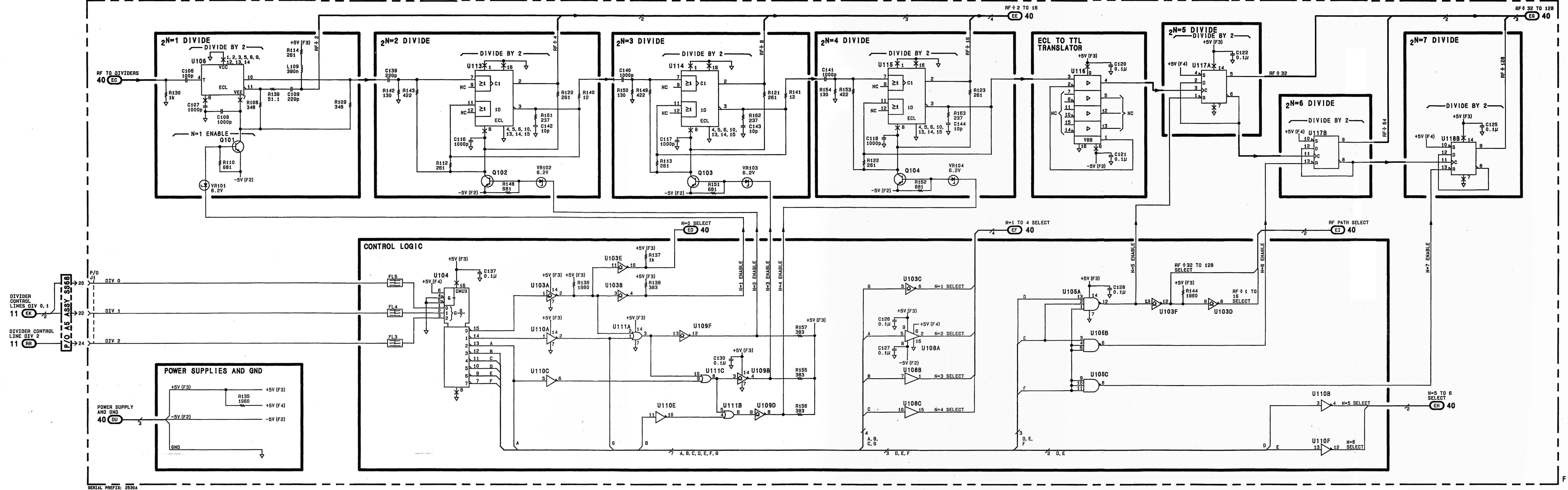
CHANGES TO FIGURE 80-114 (2530A to 2542A)

(08642-60311)

CHANGES TO FIGURE 80-114.5 (2543A and above)



P/O A12A3 SUM PHASE DETECTOR/DIVIDER ASSEMBLY (08642-60211)





A13 Module

Troubleshooting and Adjustments Contents

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Troubleshooting

A13 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A13 is the faulty module based on the results of Module Level Diagnostics (MLD).
- Open the manual to the foldout on page 8P-100. There are 3 diagrams of the A13 module. One of the diagrams is titled Simplified Block Diagram. It is intended to be used to understand the operation of A13. (There is a brief discussion of the circuit operation on page 8P-3).
- Open the next foldout on page 8P-101 (BD14). There, you will see a more detailed Block Diagram of the A13 Heterodyne Module. **This Block Diagram is meant to be used during Checks 1, 2 and 3.** Notice there are two assemblies shown, A13A2 and A13A3. These assemblies are shown on three Service Sheets, SS42, SS43 and SS44.
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustment Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No. 2	HP 8642A/B
Oscilloscope	HP 1980B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
Measuring Receiver	HP 8902A
HP 8642 Bench Service Kit	HP 11802A
Sensor Module	HP 11722A
Function Generator	HP 8116A

Essentials of A13 Module Operation

Refer to page 8P-100, SIMPLIFIED BLOCK DIAGRAM. The A13 Module contains the instrument ALC loop (SS43), Low Pass Filters (SS42), and a Serial Data Interface for control functions. The Low Pass Filters are one half octave filters used to filter out divider harmonics from the A12 Sum Loop/Divider Module. The Low Pass Filters are in the ALC Loop after the Amplitude Modulator. The Amplitude Modulator is used both for amplitude modulation and for level control.

The Serial Data Interface converts a 24 bit serial binary number into a latched 24 bit parallel binary output. These outputs are used to perform control functions in the A13 module.

CHECK 1: A13A2 CONTROL CIRCUITRY (SS44)

Essentials of SS44 Circuit Operation

Refer to BD14. Serial data comes from the microprocessor to the A13 Output Module and is received at J1 pins 13 and 15. Data is converted to a parallel bus in **SERIAL DATA INTERFACE** and sent to other functional blocks. The functional blocks labeled **OUT-OF-LOCK WINDOW COMPARATOR**, **ALC LOOP DIAGNOSTIC INTERFACE**, and **VERNIER DAC** perform control functions.

Description of Check 1

This check tests the control circuitry for the A13 module (Service Sheet 44). The A13 control circuitry is located on A13A2.

You will use the DVM to verify the output level of the **VERNIER DAC** as different bit numbers are input. Then, you will calculate the output level change. If a test fails during Check 1, refer to Component Level Repair Directory.

Required Equipment:

OscilloscopeHP1980B
DVMHP3456A

Test the Serial Data Interface

1. Setup:
- Switch the HP 8642 to standby (STBY).
- Extend A13 module on extender posts (refer to Disassembly Procedures if you are not familiar with module extension).
- Remove the A13A2 cover (see the assembly locator on the foldout opposite BD12 for location of A13A2 cover).
- Switch the HP 8642 ON.
2. Measure TTL levels:
- Key in Service Function 1 (SF1), use the Oscilloscope to verify TTL levels listed in Table 8P-1 in the column labeled SF1. Then key in Service Function (SF2), verify TTL levels listed in Table 8P-1 in the column labeled SF2.
- SF1 = SHIFT SPCL 360811184810 Hz
- SF2 = SHIFT SPCL 36085592405 Hz

Table 8P-1. Output Module Control Lines

Line Label	A13A2 REF.Des.	Bit No.	TTL Levels*	
			SF1	SF2
F3	U10 pin 16	0	L	H
F2	U10 pin 15	1	H	L
F1	U10 pin 6	2	L	H
F0	U10 pin 9	3	H	L
CW Bandwidth	U10 pin 12	4	L	H
Amp Sweep	U10 pin 5	5	H	L
MUX	U10 pin 2	6	L	H
200 kHz BW	U10 pin 19	7	H	L
DAC 10	U13 pin 5	8	L	H
DAC 9	U13 pin 15	9	H	L
DAC 8	U13 pin 12	10	L	H
DAC 7	U13 pin 9	11	H	L
DAC 6	U13 pin 6	12	L	H
DAC 5	U13 pin 16	13	H	L
DAC 4	U13 pin 2	14	L	H
DAC 11	U13 pin 19	15	H	L
DAC 3	U7 pin 5	16	L	H
DAC 2	U7 pin 6	17	H	L
DAC 1	U7 pin 9	18	L	H
DAC 0	U7 pin 12	19	H	L
MUX(LSB)	U7 pin 15	20	L	H
PULSE CNTRL	U7 pin 16	21	H	L
LOOP SWTCH	U7 pin 2	22	L	H
MUX(MSB)	U7 pin 19	23	H	L
* TTL High (H) = 2.0 to 5.0 VDC TTL Low (L) = 0.0 to 0.8 VDC				

Test the Vernier DAC

3. Setup:

Key in: **INST PRESET**.

Connect the DVM to A13A2 TP7. (Located at the top of the A13A2 board to the right of ribbon connector J1.)

Set the DVM to measure Vdc.

4. Measure Voltages:

Key in **SHIFT SPCL 3** to enter Service Mode.

Key in each Service Function from Table 8P-2 and record the DVM measurement in the column labeled "Voltage At TP7". Then calculate the Upper and Lower limits as indicated.

NOTE

For the first Service Function, verify that the voltage measurement V1 is between the upper and lower limits given. For the rest of the settings, calculate the upper and lower limits by multiplying V1 times the factors given in the table.

Table 8P-2. VERNIER DAC Voltages

Service Function	DAC Setting	Lower Limit	Voltage At TP7	Upper Limit
6 3 5 4 0 9 5 HZ	4095	8.90 Vdc	V 1 _____ Vac	9.10 Vdc
6 3 5 2 0 4 8 HZ	2048	$V1 \times .5$	V 2 _____ Vac	$V1 \times .5003$
6 3 5 1 0 2 4 HZ	1024	$V1 \times .2499$	V 3 _____ Vac	$V1 \times .2502$
6 3 5 5 1 2 HZ	512	$V1 \times .1249$	V 4 _____ Vac	$V1 \times .1252$
6 3 5 2 5 6 HZ	256	$V1 \times .06239$	V 5 _____ Vac	$V1 \times .06264$
6 3 5 1 2 8 HZ	128	$V1 \times .03114$	V 6 _____ Vac	$V1 \times .03138$
6 3 5 6 4 HZ	64	$V1 \times .01551$	V 7 _____ Vac	$V1 \times .01575$
6 3 5 3 2 HZ	32	$V1 \times .007692$	V 8 _____ Vac	$V1 \times .007937$
6 3 5 1 6 HZ	16	$V1 \times .003785$	V 9 _____ Vac	$V1 \times .004029$
6 3 5 8 HZ	8	$V1 \times .001832$	V 10 _____ Vac	$V1 \times .002076$
6 3 5 4 HZ	4	$V1 \times .0008547$	V 11 _____ Vac	$V1 \times .001099$
6 3 5 2 HZ	2	$V1 \times .0003663$	V 12 _____ Vac	$V1 \times .0006105$
6 3 5 1 HZ	1	$V1 \times .0001221$	V 13 _____ Vac	$V1 \times .0003663$
6 3 5 0 HZ	0	-.035 Vac	V 14 _____ Vac	.025 Vac

Test the Out-Of-Lock Window Comparator

5. Setup:

Connect the DVM to A13A2 TP3.

Connect A13A2 TP6 to ground.

6. Test Out-Of-Lock Window Comparator:

Press **INST PREST** on the HP 8642.

The DVM should measure approximately +5 Vdc.

Remove the ground from A13A2 TP6. Press **SHIFT** **PULSE** (AM key) **ON**. The HP 8642 should display PULSE.

The DVM should measure approximately -0.5 Vdc.

NOTE

If the comparator output fails to go to -0.5 Vdc, the problem may be with the ALC OFF or PULSE MODULATION CONTROL circuitry on SS43.

Test ALC Loop Diagnostic Interface

7. Setup:

Key in **INST PRESET**

Connect the DVM to A13A2 FL3.

8. Test Diagnostic Interface:

Key in **SHIFT SPCL 3 2 5 Hz** to enter Service Mode and enable internal voltmeter measurements. Then key in the Service Functions from Table 8P-3 and verify that the HP 8642 displays a voltage between the typical limits given in the Table.

NOTE

If a voltage is not within the typical limits listed, a fault may exist in the circuitry which supplies the sense line to the ALC Loop Diagnostic Interface. To verify this measure the voltage at A13A2 FL3 and then at the A13A2 U1 pin that the sense line in question is connected. The two voltage measurements should be the same.

Table 8P-3. ALC Loop Diagnostic Line Enable

Enter Service Mode	Service Function	Line Label	Typical Limits
	3 0 HZ	Out-Of-Lock Sense	+5 Locked 0 Vdc Unlocked
	3 1 HZ	Driver Bias Sense	Typ. 6 to 6.9 Vdc
SHIFT	3 2 HZ	Baseband Drive Sense	Typ. 0 to 13 Vdc
SPCL	3 3 HZ	AMP BIAS 1	Typ. -5.3 to -4.9 Vdc
3 2	3 4 HZ	Mod Drive Sense	Typ. 0 to 9 Vdc
	3 5 HZ	AMP BIAS 2	TYP. -27 to -1.9 Vdc
	3 6 HZ	Peak Detector Sense	Typ. -13 to 0 Vdc
	3 7 HZ	Vernier DAC Sense	Typ. $-.030$ to 9.1 Vdc

Restore Module

9. Do not perform these steps if continuing with Check 2.
10. Remove test equipment from the A13 module.
11. Re-install the A13A2 cover.
12. Re-install the A13 module in the HP 8642.
13. Reconnect all HP 8642 internal cabling.

CHECK 2: A13A1 LOW PASS FILTER ASSEMBLY (SS42)

NOTE

*Use the Module Test Point/Adjustment Locations diagram on the fold-out opposite BD14 to locate test points on A13A1. Test point designators (**XX**) will be used when applicable. Points not located on the Module Test Point/Adjustment Locations diagram can be found using the Component Locator diagrams opposite SS42.*

Essentials of A13A1 Operation

Refer to SS42. The input to the A13A1 Low Pass Filter Assembly is on J1 from the output of the Amplitude Modulator on SS43. The output is on J2 from the RF Output Amplifier. This output drives the RF Power Amplifier on SS43.

The Low Pass Filter Assembly A13A1 contains 16 one half octave low pass filters for harmonic rejection. The filters are arranged in two banks of eight, **SWITCHED LOW FREQUENCY FILTERS** and **SWITCHED HIGH FREQUENCY FILTERS**. The **RF INPUT AMPLIFIER** and **RF OUTPUT AMPLIFIERS** compensate for the low pass filter insertion loss and for the **INPUT PATH SWITCH** and **OUTPUT PATH SWITCH** insertion loss. The low pass filters and input and output switches use pin diode switches.

The **SWITCH DRIVE LOGIC** converts Filter Select Lines F0 through F3 to -5 Vdc logic, where -5 Vdc = logic 1. This is accomplished by comparators U6A through U6D. The outputs from the comparators supply the address and select lines for decoders U2 and U3. The F3 line (U6C) is used to switch the input and output path switches and to select either U2 or U3 for address selection.

The **RF OUTPUT AMPLIFIER** circuit also contains the pulse modulator. The pulse modulator consists of CR48, CR49, and CR50. The pulse signal comes from SS43. The pulse modulator is a single pole single throw pin diode switch with one shunt diode (CR50) for better on/off ratio performance.

Description of Check 2

In this check the power supplies are first measured with the DVM. Next the F0 through F3 lines are checked with the DVM. The RF Input and Output Amplifiers, Input and Output Path Switches, Switched High and Low Frequency Filters, and Switch Drive Logic are checked next by measuring the frequency response of each low pass filter and checking the overall circuit gain. Then the pulse modulator is checked last.

Required Equipment:

Signal Generator No. 2	HP 8642A/B
Spectrum Analyzer	HP 8566A/B
DVM	HP 3456A

Test the F0 through F3 and Power Supply Lines

1. Setup:

Set the HP 8642 POWER switch to STDBY.

Extend the A13 module. (Refer to instrument disassembly procedures if you are not familiar with module extension.)

Remove the A13A1 cover. (Refer to the inside of the top cover to determine A13A1 position.)

CAUTION

When removing the A13A1 cover, first remove A13A1 Q1's heatsink. This heatsink is located a little below and to the left of A13A1 J2. It is round (2cm diameter) with a slot for a screw driver. UNSCREW A13A1 Q1's HEATSINK FIRST THEN REMOVE THE A13A1 COVER SCREWS. After removing the cover screw the heatsink back onto A13A1 Q1.

Set the HP 8642 POWER switch to ON.

2. Measure A13A1 Power Supply Lines:

Use the DVM to measure and verify the power supply lines listed in Table 8P-4 at A13A1 J3.

Table 8P-4. A13 Power Supply Lines

A13A1 J3	Nominal Voltage
pin 3	$\approx +15V$
pin 4	$\approx -5V$

3. Measure F0 through F3 Lines:

Set the HP 8642 to each frequency shown in Table 8P-5, and verify with the DVM that the voltages are correct at each A13A1J3 pin listed for each front panel setting.

Table 8P-5. F0 through F3 Lines Measurements

HP 8642 Frequency Setting	A13A1J3 Pin 8 (F3)	A13A1J3 Pin 6 (F2)	A13A1J3 Pin 7 (F1)	A13A1J3 Pin 5 (F0)
1000 MHz	L	L	L	L
700 MHz	L	L	L	H
500 MHz	L	L	H	L
200 MHz	L	H	L	L
60 MHz	H	L	L	L
* TTL High (H) = 2.0 to 5.0 VDC TTL Low (L) = 0.0 to 0.8 VDC				

Verify RF Input and Output Amplifiers, Input and Output Path Switches, Switch Drive Logic, Switched High and Low Frequency Filters.

4. Setup:

Disconnect A13W1 from A13A1 J1.

Disconnect A13W2 from A13A1 J2.

Set Signal Generator No.2 to 4.0 MHz, -10 dBm output.

Connect Signal Generator No.2 to A13A1 J1.

Connect the Spectrum Analyzer to A13A1 J2.

5. Measure RF Input and Output Amplifiers, Input and Output Path Switches, Switch Drive Logic, and Switched High and Low Frequency Filters:

For Table 8P-6 through Table 8P-21, key in the HP 8642 Front Panel Frequency, then set Signal Generator No.2 to each frequency listed for it and verify that the level is correct at the A13A1 output using the Spectrum Analyzer.

Table 8P-6. LF8 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
4.5 MHz	4.13 MHz	0 dBm +/– 2 dB
	5.85 MHz	0 dBm +/– 2 dB
	8.26 MHz	< –20 dBm
	11.7 MHz	< –45 dBm

Table 8P-7. LF7 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
6 MHz	5.85 MHz	0 dBm +/– 2 dB
	8.26 MHz	0 dBm +/– 2 dB
	11.7 MHz	< –20 dBm
	16.5 MHz	< –45 dBm

Table 8P-8. LF6 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
9 MHz	8.26 MHz	0 dBm +/– 2 dB
	11.7 MHz	0 dBm +/– 2 dB
	16.5 MHz	< –20 dBm
	23.4 MHz	< –45 dBm

Table 8P-9. LF5 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
14 MHz	11.7 MHz	0 dBm +/– 2 dB
	16.5 MHz	0 dBm +/– 2 dB
	23.4 MHz	< –20 dBm
	33.0 MHz	< –45 dBm

Table 8P-10. LF4 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
20 MHz	16.5 MHz	0 dBm +/– 2 dB
	23.4 MHz	0 dBm +/– 2 dB
	33.0 MHz	< –20 dBm
	46.7 MHz	< –45 dBm

Table 8P-11. LF3 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
25 MHz	23.4 MHz	0 dBm \pm 2 dB
	33.0 MHz	0 dBm \pm 2 dB
	46.7 MHz	< -20 dBm
	66.1 MHz	< -45 dBm

Table 8P-12. LF2 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
37 MHz	33.0 MHz	0 dBm \pm 2 dB
	46.7 MHz	0 dBm \pm 2 dB
	66.1 MHz	< -20 dBm
	93.5 MHz	< -45 dBm

Table 8P-13. LF1 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
50 MHz	46.7 MHz	0 dBm \pm 2 dB
	66.1 MHz	0 dBm \pm 2 dB
	93.5 MHz	< -20 dBm
	132.2 MHz	< -45 dBm

Table 8P-14. HF8 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
80 MHz	66.1 MHz	0 dBm \pm 2 dB
	93.5 MHz	0 dBm \pm 2 dB
	132.2 MHz	< -20 dBm
	187 MHz	< -45 dBm

Table 8P-15. HF7 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
115 MHz	93.5 MHz	0 dBm \pm 2 dB
	132.2 MHz	0 dBm \pm 2 dB
	187 MHz	< -20 dBm
	264.4 MHz	< -45 dBm

Table 8P-16. HF6 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
150 MHz	132.2 MHz	0 dBm \pm 2 dB
	187 MHz	0 dBm \pm 2 dB
	264.4 MHz	< -20 dBm
	373.9 MHz	< -45 dBm

Table 8P-17. HF5 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
210 MHz	187 MHz	0 dBm \pm 2 dB
	246.4 MHz	0 dBm \pm 2 dB
	373.9 MHz	< -30 dBm
	528.75 MHz	< -45 dBm

Table 8P-18. HF4 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
300 MHz	246.4 MHz	0 dBm \pm 2 dB
	373.9 MHz	0 dBm \pm 2 dB
	528.75 MHz	< -20 dBm
	747.8 MHz	< -45 dBm

Table 8P-19. HF3 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
450 MHz	373.9 MHz	0 dBm \pm 2 dB
	528.75 MHz	0 dBm \pm 2 dB
	747.8 MHz	< -20 dBm
	1057.5 MHz	< -45 dBm

Table 8P-20. HF2 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
650 MHz	528.75 MHz	0 dBm \pm 2 dB
	747.8 MHz	0 dBm \pm 2 dB
	1057.5 MHz	< -20 dBm
	1495.6 MHz	< -40 dBm

Table 8P-21. HF1 Filter Response

HP 8642 Front Panel Frequency	Signal Generator No.2 Frequency	A13A1 Output Level
900 MHz	747.8 MHz	0 dBm \pm 2 dB
	1057.5 MHz	0 dBm \pm 2 dB
	1495.6 MHz	< -20 dBm
	2115 MHz	< -40 dBm

Verify Pulse Modulator On/Off Ratio

6. Setup:

Ensure that the setup has not changed from the above filter checks.

7. Measure Pulse Modulator On/Off Ratio:

Set the HP 8642 front panel frequency to 1057 MHz.

Set Signal Generator No.2 to 1057 MHz, -10 dBm output.

Measure the 1057 MHz signal with the Spectrum Analyzer. It should be 0 dBm \pm 2 dBm.

Key in **[SHIFT] [PULSE]** (AM key) **[ON]** on the HP 8642. Ensure that the display on the HP 8642 displays PULSE.

The 1057 MHz signal on the Spectrum Analyzer should now measure less than -30 dBm (HP 8642 serial prefixes below 2511A) or less than -40 dBm (HP 8642 serial prefixes 2511A and above).

Press the **[OFF/ON]** key on the HP 8642. Ensure that the display on the HP 8642 displays PL.OFF.

Restore Module

8. Set the HP 8642 POWER switch to STBY.
9. Remove test cables from the A13A1 assembly.
10. Re-install the A13A1 cover.

CAUTION

When re-installing the A13A1 cover, first set the cover in place and install all of it's screws. Then install A13A1 Q1's heatsink. ONLY TIGHTEN A13A1 Q1's HEATSINK FINGER TIGHT.

11. Re-connect the A13 module cables removed previously.

CHECK 3: A13A2 ALC/POWER AMPLIFIER CIRCUITRY (SS43)

NOTE

*Use the Module Test Point/Adjustment Locations diagram on the fold-out opposite BD15 to locate test points on A13A2. Test point designators (**XX**) will be used when applicable. Points not located on the Module Test Point/Adjustment Locations diagram can be found using the Component Locator diagrams opposite SS45.*

Essentials of SS43 Circuit Operation

The A13A2 ALC/Power Amplifier Assembly receives its RF input from the A12 Summation Module on A13A2 J5. The input frequency is between 4.13 to 1057 MHz at a level between 0 dBm and +4 dBm. The input is amplified by the **MODULATOR RF DRIVER** which supplies RF drive for the **AMPLITUDE MODULATOR**. The Amplitude Modulator is a ring type with the single ended RF input converted to a balanced input in Balun Z3. The ring modulators, Z1 and Z2, receive bias current through Balun Z4. Balun Z4 converts the balanced signal back to a single ended signal. The output from the Amplitude Modulator goes to the A13A1 Low Pass Filters and then to the **RF POWER AMPLIFIER AND PEAK DETECTOR**. The RF Power Amplifier (U3) provides the RF output from the A13 Module. The RF Power Amplifier also contains a peak detector diode, which along with U9, CR6, CR1, and CR2, provides the ALC Feedback signal to the Integrator. The Non-Linearity Compensation composed of CR1, CR2, R48, R77, R49, R53, and R59 reduces AM distortion at low ALC levels with large AM depths.

The **INTEGRATOR** drives the Amplitude Modulator through the **ALC INVERTER** and **BASEBAND DRIVE AND ALC LOOP SWITCH** until the sum of the signals at its inverting input equal zero. The inputs to the Integrator are the ALC Feedback, Vernier DAC, and Amplitude Modulation base band signals. The integrator has three bandwidths dependent on instrument setup. When in CW mode C6 is the selected integration capacitor through Q9. The ALC Loop bandwidth in CW mode is 200 Hz. When AM is selected with the output frequency less than 33.04 MHz, C5 is selected through Q7. The loop bandwidth is then 35 KHz. When AM is selected for frequencies above 33.04 MHz neither C6 or C5 are selected and C4 is the only feedback capacitor. The loop bandwidth is then 340 KHz.

The ALC Loop Switch Q4 (in the **BASEBAND DRIVE AND ALC LOOP SWITCH** block) opens the ALC Loop for ALC off operation and Pulse Modulation. When in ALC off, the Vernier DAC (SS44) controls the ALC Loop output level through the **AMPLITUDE SWEEP AND PULSE MODULATION SWITCH** Q3.

The **PULSE MODULATION CONTROL** comparator U8B supplies a fast rise and fall time pulse to the pulse modulator on SS42. The comparator is set to trip at +0.4 Vdc.

Description of Check 3

The power supply inputs are first checked for proper voltages with the DVM. Next the Amplitude Modulator dynamic range is checked using the Spectrum Analyzer and instrument special functions to control the Vernier DAC. Then the ALC Loop bandwidths are checked using the Function Generator and the Measuring Receiver. Then the Pulse Modulation Control comparator is checked. Then the last thing checked is the ALC Loop range and maximum power output.

Required Equipment:

Signal Generator No. 2	HP 8642
Oscilloscope	HP 1980B
Spectrum Analyzer	HP 8566A/B
Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
DVM	HP 3456A
Function Generator	HP 8116A

Test the Power Supplies

1. Setup:

Set the HP 8642 POWER switch to STBY.

Extend the A13 Module. (Refer to instrument disassembly procedures if unfamiliar with module extension.)

Remove the A13A2 cover. (Refer to inside of the top cover for A13A2 location.)

Set the HP 8642 POWER switch to ON.

2. Measure Voltages:

Use the DVM to measure the power supply voltages listed in Table 8P-22.

Table 8P-22. A13 Power Supply Lines

Component	Nominal Voltage
FL4	$\approx -15V$
FL5	$\approx -5V$
FL6	$\approx +5V$
FL11	$\approx +15V$
FL8	$\approx +50V$

Test ALC Loop Circuitry

3. Setup:

NOTE

This procedure assumes the A12 Summation Module is functioning properly and that the HP 8642 cabling is connected normally. Only remove the cables needed to make connections specified during this procedure.

On the HP 8642 key in **INST PRESET** **SHIFT** **SPCL** **4**. (This opens the ALC loop with the ALC LOOP SWITCH.)

On the HP 8642 key in **FREQ** **1057** **MHz**.

Set the Spectrum Analyzer center frequency to 1057 MHz, frequency span to 1 MHz, and reference level to +30 dBm.

Connect the Spectrum Analyzer to A13A2 J3.

4. Measure Amplitude Modulator Dynamic Range and ALC Loop Maximum Power Output:

On the HP 8642 key in **SHIFT** **SPCL** **3** **6354095** **Hz**. This sets the Vernier DAC (SS 44) to it's maximum output. Service special function 635 sets the Vernier DAC to the number following it. i.e. 6354095 sets the Vernier DAC to 4095.

The 1057 MHz signal should measure greater than +20 dBm on the Spectrum Analyzer. Record this level for reference.

On the HP 8642 key in **SHIFT** **SPCL** **3** **6350** **Hz**. This sets the Vernier DAC to it's minimum output.

The 1057 MHz signal should measure at least -36 dB less than the signal with the Vernier DAC set to maximum.

Measure ALC Loop Bandwidths**5. Setup:**

On the HP 8642 key in **INST PRESET** **33** **MHz** **RF OFF/ON**. Ensure that the HP 8642 displays RF.OFF.

Set the Function Generator to frequency to 20 Hz, amplitude to 1.00V, offset to 0.00V, and select sinewave output.

Connect the Function Generator to A13A2 J4.

Disconnect the Spectrum Analyzer from A13A2 J3 and connect the Measuring Receiver to A13A2 J3.

Set the Measuring Receiver to measure AM.

Press the **RF OFF/ON** key and verify that the HP 8642 displays -140.0 DM.

6. Measure ALC 200 Hz Bandwidth:

Adjust the Function Generator amplitude for an AM measurement on the Measuring Receiver of 90% \pm 1%.

Set the Measuring Receiver for a RATIO measurement in LOG terms. The Measuring Receiver should now be displaying 0.00 dB.

Change the Function Generator frequency to 100 Hz. The Measuring Receiver should now display less than -1 dB.

Change the Function Generator frequency to 200 Hz. The Measuring Receiver should now display less than -3 dB.

7. Measure ALC 35 kHz Bandwidth:

On the HP 8642 key in **AM** **ON**. This turns on AM modulation and increases the ALC bandwidth to 35 kHz for frequencies below 33.04 MHz. (The HP 8642 should display 50.0 PC.)

The Measuring Receiver display should return to 0.00 dB \pm 1.25 dB.

Turn the ratio off on the Measuring Receiver and re-adjust the Function Generator amplitude for an AM measurement on the Measuring Receiver of 90% \pm 1%.

Set the Measuring Receiver for a RATIO measurement in LOG terms. The Measuring Receiver should now be displaying 0.00 dB.

Set the Function Generator frequency to 20 Hz. The Measuring Receiver should display 0.00 dB \pm 0.5 dB.

Set the Function Generator frequency to 1 kHz. The Measuring Receiver should display 0.00 dB \pm 0.5 dB.

Set the Function Generator frequency to 10 kHz. The Measuring Receiver should display 0.00 dB \pm 1.0 dB.

Set the Function Generator frequency to 20 kHz. The Measuring Receiver should display between 0.00 dB and -1.5 dB.

Set the Function Generator frequency to 35 kHz. The Measuring Receiver should display less than -2.0 dB.

8. Measure ALC 340 kHz Bandwidth:

On the HP 8642 key in **FREQ** **33.1** **MHz**. This increases the ALC bandwidth to 340 kHz for frequencies above 33.04 MHz. (The HP 8642 should still display 50.0PC.)

The Measuring Receiver display should return to 0.00 dB \pm 1.25 dB.

Turn the ratio off on the Measuring Receiver and re-adjust the Function Generator amplitude for an AM measurement on the Measuring Receiver of 90% \pm 1%.

Set the Measuring Receiver for a RATIO measurement in LOG terms. The Measuring Receiver should now be displaying 0.00 dB.

Set the Function Generator frequency to 20 Hz. The Measuring Receiver should display 0.00 dB \pm 0.5 dB.

Set the Function Generator frequency to 1 kHz. The Measuring Receiver should display 0.00 dB \pm 0.5 dB.

Set the Function Generator frequency to 10 kHz. The Measuring Receiver should display 0.00 dB \pm 0.5 dB.

Set the Function Generator frequency to 100 kHz. The Measuring Receiver should display between +1.0 dB and -2.0 dB.

Check Pulse Modulation Control

9. Setup:

Ensure that the setup has not changed from the above ALC Loop Bandwidth checks.

Set the Function Generator frequency to 50 kHz, amplitude to 800 mVpp.

Set the Oscilloscope to 10.0 uS per division, and 5 Volts per division.

Connect the Oscilloscope to the anode of A13A2 VR1.

10. Measure Pulse Modulation Control comparator:

On the HP 8642 key in **INST PRESET** **SHIFT** **PULSE** (the AM key) **ON**.

The Oscilloscope should display a 50 kHz (20 uS period) square wave with an amplitude between approximately +4 Vdc and -14.8 Vdc.

Measure ALC Loop Range and Maximum Power

11. Setup:

On the HP 8642 key in **INST PRESET** **10** **MHz** **AMPTD** **5** **dBm**.

Disconnect the Function Generator from A13A2 J4.

Ensure that the Sensor Module is connected to the Measuring Receiver and that the Measuring Receiver power meter is zeroed and calibrated.

Connect the Sensor Module to A13A2 J3.

Set the Measuring Receiver to measure RF Power.

Set the DVM to measure DC Volts and connect the DVM to A13A2 TP3 (SS44). This is the output of the OUT-OF-LOCK WINDOW COMPARATOR.

12. Measure ALC Loop Output Power:

Set the HP 8642 to the Frequencies and Amplitudes listed in Tables 8P-23 through 8P-26. Key the HP 8642 Frequency into the Measuring Receiver and verify that the ALC Loop output power is within the limits listed in the tables.

Check the DVM reading for each HP 8642 amplitude setting. The voltage on A13A2 TP3 should read approximately +5.2 Vdc. This indicates that the ALC Loop is locked. A reading of 0 Vdc indicates an out of lock condition.

Table 8P-23. ALC Loop Check at 10 MHz

HP 8642 Frequency	HP 8642 Amplitude	Lower Limit	Measured Level	Upper Limit
10 MHz	+5 dBm	+4 dBm	_____ dBm	+7 dBm
	+10 dBm	+9 dBm	_____ dBm	+12 dBm
	+15 dBm	+14 dBm	_____ dBm	+17 dBm
	+20 dBm	+19 dBm	_____ dBm	+22 dBm

Table 8P-24. ALC Loop Check at 264 MHz

HP 8642 Frequency	HP 8642 Amplitude	Lower Limit	Measured Level	Upper Limit
264 MHz	+5 dBm	+4 dBm	_____ dBm	+8 dBm
	+10 dBm	+9 dBm	_____ dBm	+13 dBm
	+15 dBm	+14 dBm	_____ dBm	+18 dBm
	+20 dBm	+19 dBm	_____ dBm	+23 dBm

Table 8P-25. ALC Loop Check at 528 MHz

HP 8642 Frequency	HP 8642 Amplitude	Lower Limit	Measured Level	Upper Limit
528 MHz	+5 dBm	+4 dBm	_____ dBm	+8 dBm
	+10 dBm	+9 dBm	_____ dBm	+13 dBm
	+15 dBm	+14 dBm	_____ dBm	+18 dBm
	+19 dBm	+18 dBm	_____ dBm	+22 dBm

Table 8P-26. ALC Loop Check at 1057 MHz

HP 8642 Frequency	HP 8642 Amplitude	Lower Limit	Measured Level	Upper Limit
1057 MHz	+5 dBm	+4 dBm	_____ dBm	+9 dBm
	+10 dBm	+9 dBm	_____ dBm	+14 dBm
	+15 dBm	+14 dBm	_____ dBm	+19 dBm
	+17 dBm	+16 dBm	_____ dBm	+20 dBm

Restore Module

13. Remove test equipment from the A13 Module.
14. Reconnect A13 cables.
15. Re-install the A13A2 cover.

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

- * Special function codes relevant to the module.
- * Transistor emitter, base and collector voltages.
- * Frequency and power levels at different circuit points.
- * Module control line and power supply interconnections in the module and instrument.

NOTE

*Start with the tables that are labeled with a Service Sheet number (Example: **Table 8P-27 SS42 Filter Control Selects**). Other tables are more general and are to be used at your discretion. It is suggested that you familiarize yourself with the contents of these tables so you can determine if they will be effective in solving your particular troubleshooting need.*

Table 8P-27 SS42 Filter Control Selects	8P-20
Table 8P-28 SS42 DC Voltage	8P-20
Table 8P-29 SS42 Stage Gains	8P-21
Table 8P-30 SS42 Low Pass Filter Insertion Loss	8P-21
Table 8P-31 SS43 Setting Serial Data Interface (Clock and Data Input Lines)	8P-21
Table 8P-32 SS43 Stage Gains, ALC On Maximum Vernier	8P-22
Table 8P-33 SS43 Stage Gains, ALC Off Maximum Vernier	8P-22
Table 8P-34 SS43 Stage Gains, ALC Off Minimum Vernier	8P-22
Table 8P-35 SS43 DC Voltages	8P-23
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Table 8P-37 SS43 Truth Table For A13 Line Selects	8P-23
Table 8P-38 SS43 Power Supply Line Interconnections	8P-23
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Table 8P-40 SS44 ALC Loop Diagnostic Line Enable	8P-25
Table 8P-41 SS44 Setting Control Lines	8P-25
Table 8P-42 Control Line Interconnections	8P-26
Table 8P-43 Special Functions	8P-26

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Table 8P-27. SS42 Filter Control Selects

Enter Service Mode	Function	F3	F2	F1	F0	Filter Selected	Path Switch Selects		Filter Selects	
							LF*	HF*	LF*	HF*
SHIFT SPCL 3	6 0 8 0 HZ	0	0	0	0	HF1	1	0	1	0
	6 0 8 1 HZ	0	0	0	1	HF2	1	0	1	0
	6 0 8 2 HZ	0	0	1	0	HF3	1	0	1	0
	6 0 8 3 HZ	0	0	1	1	HF4	1	0	1	0
	6 0 8 4 HZ	0	1	0	0	HF5	1	0	1	0
	6 0 8 5 HZ	0	1	0	1	HF6	1	0	1	0
	6 0 8 6 HZ	0	1	1	0	HF7	1	0	1	0
	6 0 8 7 HZ	0	1	1	0	HF8	1	0	1	0
	6 0 8 8 HZ	1	0	0	0	LF1	0	1	0	0
	6 0 8 9 HZ	1	0	0	1	LF2	0	1	0	1
	6 0 8 1 0 HZ	1	0	1	0	LF3	0	1	0	1
	6 0 8 1 1 HZ	1	0	1	1	LF4	0	1	0	1
	6 0 8 1 2 HZ	1	1	0	0	LF5	0	1	0	1
	6 0 8 1 3 HZ	1	1	0	1	LF6	0	1	0	1
	6 0 8 1 4 HZ	1	1	1	0	LF7	0	1	0	1
	6 0 8 1 5 HZ	1	1	1	1	LF8	0	1	0	1

* U6 A thru D are level shifting inverters. A TTL low input, results in ≈ 0 Vdc out (high) and a TTL high input results in ≈ -5 Vdc out (low). For U1,U2,U3, and U4 1 = ≈ 0 Vdc 0 = ≈ -5 Vdc

Table 8P-28. SS42 DC Voltages

Transistor	Base	Emitter	Collector
Q1	2 to 2.5 Vdc	1.3 to 1.8 Vdc	10.6 to 11.1 Vdc
Q2	9.9 to 10.6 Vdc	10.6 to 11.1 Vdc	3 to 3.5 Vdc
Q3	1.2 to 1.7 Vdc	.6 to .9 Vdc	6 to 7 Vdc

Table 8P-29. SS42 Stage Gains

Stage	Gain
Input RF Amplifier	≈ 6 dBm
Low Pass Filters	≈ -4 dBm
Output RF Amplifier	≈ 7 dBm

Table 8P-30. SS42 Low Pass Filter Insertion Loss

Filter	Frequency Range	Insertion Loss
HF1	747.800001 to 1057.5 MHz	≈ 4 dBc
HF2	528.750001 to 747.8 MHz	≈ 4 dBc
HF3	373.900001 to 528.75 MHz	≈ 4 dBc
HF4	264.400001 to 373.9 MHz	≈ 4 dBc
HF5	187.000001 to 264.4 MHz	≈ 4 dBc
HF6	132.200001 to 187 MHz	≈ 4 dBc
HF7	93.500001 to 132.2 MHz	≈ 4 dBc
HF8	66.100001 to 93.5 MHz	≈ 4 dBc
LF1	46.700001 to 66.1 MHz	≈ 4 dBc
LF2	33.050001 to 46.7 MHz	≈ 4 dBc
LF3	23.400001 to 33.05 MHz	≈ 4 dBc
LF4	16.500001 to 23.4 MHz	≈ 4 dBc
LF5	11.700001 to 16.5 MHz	≈ 4 dBc
LF6	8.260001 to 11.7 MHz	≈ 4 dBc
LF7	5.850001 to 8.26 MHz	≈ 4 dBc
LF8	4.130001 to 5.85 MHz	≈ 4 dBc

SERVICE SHEET 43**Table 8P-31. SS43 Setting Serial Data Interface (Clock and Data Input Lines)**

Enter Service Mode	Function	Description	DVM Measurements	
			A13A2FL1	A13A2FL2
SHIFT	6 0 1 4 0 HZ	Sets Clock Bit To 1	1	-
SPCL	6 0 2 4 0 HZ	Sets Clock Bit To 0	0	-
3	6 0 1 4 1 HZ	Sets Data Bit To 1	-	1
	6 0 2 4 1 HZ	Sets Data Bit To 0	-	0

Table 8P-32. SS43 Stage Gains, ALC On Maximum Vernier

Stage	Gain/Voltage
A13A2 ALC/Power Amplifier Assembly	
Modulator/RF Driver	≈ 15 dBm
Amplitude Modulator	≈ -4 dBm
Voltage At TP4	≈ 9.6 Vdc
Voltage At TP8	≈ 10.8 Vdm
A13A1 Low Pass Filters*	≈ 9 dBm
RF Power Amplifier And Peak Detector	≈ 7 dBm
* Stage gains are given with input levels so as not to drive the stage into compression (-10 dBm).	

Table 8P-33. SS43 Stage Gains, ALC Off Maximum Vernier

Stage	Gain/Voltage
A13A2 ALC/Power Amplifier Assembly	
Modulator/RF Driver	≈ 15 dBm
Amplitude Modulator	≈ -4 dBm
A13A1 Low Pass Filters*	≈ 9 dBm
RF Power Amplifier And Peak Detector	≈ 7 dBm
*A13A1 Low Pass Filters	
Input RF Amplifier	≈ 6 dBm
Low Pass Filters	≈ -4 dBm
Output RF Amplifier	≈ 7 dBm
Base Band Drive Voltages	
TP4	≈ 7.5 Vdc
TP8	≈ 8 Vdc
* Stage gains are given with input levels so as not to drive the stage into compression.	

Table 8P-34. SS43 Stage Gains, ALC Off Minimum Vernier

Stage	Gain/Voltage
A13A2 ALC/Power Amplifier Assembly	
Modulator/RF Driver	≈ 15 dBm
Amplitude Modulator	≈ -70 dBm
Voltage At TP4	≈ -30 MVdc
Voltage At TP8	≈ -30 MVdm
A13A1 Low Pass Filters*	≈ 9 dBm
RF Power Amplifier And Peak Detector	≈ 7 dBm
* Stage gains are given with input levels so as not to drive the stage into compression.	

Table 8P-35. SS43 DC Voltages

Test Point	Voltage
TP1	-2.7 to -1.9 Vdc
TP2	-5.3 to -4.9 Vdc
TP10	-13 to 0 Vdc

Table 8P-36. SS43 DC Voltages

Transistor	Collector	Base
Q1 (TP5)	5.9 to 6.8 Vdc	.9 to 1.4 Vdc
Q5 (TP9)	6.0 to 6.9 Vdc	1.2 to 1.7 Vdc
Q2 (Selected)	≈ 0 Vdc	-.9 to -.6 Vdc
Q2 (Not Selected)	≈ 0 Vdc	≈ 0 Vdc
Q8 (Selected)	.8 to 1.3 Vdc	≈ 0 Vdc
Q8 (Not Selected)	.2 to .6 Vdc	≈ 5 Vdc
Q10 (Selected)	.8 to 1.3 Vdc	≈ 0 Vdc
Q10 (Not Selected)	.2 to .6 Vdc	≈ 5 Vdc

Table 8P-37. SS43 Truth Table For A13 Line Selects

Conditions	ALC Loop Switch <input type="checkbox"/> GY *	Pulse Control <input type="checkbox"/> GV	200 kHz Select <input type="checkbox"/> HB	ALC Off Select <input type="checkbox"/> GU	CW Bandwidth Select <input type="checkbox"/> HE
Bands 1 Thru 4 etc.					
No AM Bands 1-4	0	0	0	0	0
No AM Bands 5-9	0	0	1	0	0
AM Bands 1-4	0	0	0	0	1
AM Bands 5-9	0	0	1	0	1
Amplitude Sweep	1	0	1	1	1
Pulse Mode	1	1	X	1	X
ALC Off Mode	1	0	X	1	X
Heterodyne Bands					
No AM	0	0	1	0	1
AM	0	0	1	0	1
Amplitude Sweep	1	0	1	1	1
Pulse Mode	1	1	X	1	X
ALC Off Mode	1	0	X	1	X

* 0 is the active state when this line is selected.
0 = 0.0 to 0.8 Vdc 1 = 2.0 to 6.0 Vdc X = don't care

Table 8P-38. SS43 Power Supply Lines Interconnections

Supply	A17 Output	A5		A13A2 Input
		Input	Output	
+50 Vdc	J2 Pins 3-4	J12 Pins 3-4	J6 Pin 16	J1 Pin 1
+15 Vdc	J2 Pins 9-18	J12 Pins 9-18	J6 Pins 14,15	J1 Pin 2,3
+5 Vdc	J2 Pins 35-50	J12 Pins 35-50	J6 Pins 12,13	J1 Pins 4,5
-5 Vdc	J2 Pins 23-26	J12 Pins 23-26	J6 Pins 10,11	J1 Pins 6,7
-15 Vdc	J2 Pins 19-22	J12 Pins 19-22	J6 Pins 8,9	J1 Pins 8,9
GND		Chassis GND	J6 Pins 1,3,5,7	J1 Pins 10,12,14,16

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Table 8P-39. SS44 Setting Register Outputs In Serial Data Interface

Line Label	Bit #	Decimal Value
Filter SEL. F3 (MSB) <input type="button" value="GP"/>	0	1
Filter SEL. F2 <input type="button" value="GP"/>	1	2
Filter SEL. F1 <input type="button" value="GP"/>	2	4
Filter SEL. F0 (LSB) <input type="button" value="GP"/>	3	8
CW Bandwidth Select <input type="button" value="HE"/>	4	16
ALC Off Select <input type="button" value="GU"/>	5	32
MUX A1	6	64
200 kHz BW SELECT <input type="button" value="HB"/>	7	128
DAC Bit 0 (LSB)	8	256
DAC Bit 1	9	512
DAC Bit 2	10	1024
DAC Bit 3	11	2048
DAC Bit 4	12	4096
DAC Bit 5	13	8192
DAC Bit 6	14	16384
DAC Bit 7	15	32768
DAC Bit 8	16	65536
DAC Bit 9	17	131072
DAC Bit 10	18	262144
DAC Bit 11 (MSB)	19	524288
MUX A0 (LSB)	20	1048576
Pulse Control <input type="button" value="GV"/>	21	2097152
ALC Loop Switch <input type="button" value="GY"/>	22	4194304
MUX A2 (MSB)	23	8388608

To set the outputs of the Serial Data Interface registers (U7, U13, and U10 on SS44), key in: **SHIFT**
SPCL **3** **6** **0** **8** **Decimal Value*** **HZ**

* To determine the decimal value to enter you must first know what you want each bit to be, high or low. This gives you a 24 bit binary coded decimal (BCD). Convert this BCD to its decimal equivalent by adding the Decimal Values (from Table 24) of the Lines you want to be high.

NOTE

To determine which bits are set, key in **SHIFT** **SPCL** **3** **6** **0** **3** **4** **HZ**, then convert the decimal number on the display to a binary number. For example, if 5592405 is displayed, the following bit numbers are set: 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, and 22.

To set all bits low, key in: **SHIFT** **SPCL** **3** **6** **0** **8** **0** **HZ**

To set all bits high, key in: **SHIFT** **SPCL** **3** **6** **0** **8** **16777215** **HZ**

Table 8P-40. SS44 ALC Loop Diagnostic Line Enable

Enter Service Mode	Function	Line Label	Explanation
<div>SHIFT</div> <div>SPCL</div> <div>3 2</div>	3 0 HZ	Out-Of-Lock Sense	+5 Locked 0 Vdc Unlocked
	3 1 HZ	Driver Bias Sense	Typ. 6 to 6.9 Vdc
	3 2 HZ	Baseband Drive Sense	Typ. 0 to 13 Vdc
	3 3 HZ	AMP BIAS 1	Typ. -5.3 to -4.9 Vdc
	3 4 HZ	Mod Drive Sense	Typ. 0 to 9 Vdc
	3 5 HZ	AMP BIAS 2	TYP. -27 to -1.9 Vdc
	3 6 HZ	Peak Detector Sense	Typ. -13 to 0 Vdc
	3 7 HZ	Vernier DAC Sense	Typ. -.030 to 9.1 Vdc

Table 8P-41. SS44 Setting Control Lines

Enter Service	Select a Function		Select a Line	
<div>SHIFT</div> <div>SPCL</div> <div>3</div>	6 0 0	Reads line state	1 7 HZ	A13 OOL Disable
	6 0 1	Sets line to 1	4 0 HZ	A13 CLK
	6 0 2	Sets line to 0	4 1 HZ	A13 Data
	6 1 5	*Continuous Toggle	1 0 5 HZ	**A13 OOL
* Toggling continues until HP 8642 power is turned off				
** Read is the only function that can be selected for A13 OOL				

Example: To read A13 DATA line state, key in: **SHIFT SPCL 3 6 0 0 4 1 HZ**

Table 8P-42. Control Line Interconnections

Line Label	A13	A5		A4	
	INPUT	OUTPUT	INPUT	OUTPUT	LATCH
OOL Disable*	Connector/Pin	Connector/Pin	Connector/Pin	Connector/Pin	IC Pin U13/9
A13 CLK	A13A2J1/15	A5J6/2	A5J16/41	A4P2/41	U16/2
A13 DATA	A13A2J1/13	A5J6/4	A5J16/43	A4P2/43	U16/4
A13 OOL	A13A2J1/11	A5J6/6	A5J16/12	A4P2/12	U35/13

* OOL Disable: Circuitry Located on A4. Disables out of lock interrupts to the DCU.

Table 8P-43. A13 Special Functions

Function	Description
SHIFT SPCL 3 7 0 4 HZ	Turns Off CAL DATA
SHIFT SPCL 3 7 1 4 HZ	Turns On CAL DATA
SHIFT SPCL 3 6 2 0 4 HZ	Displays Output Section FREQ
SHIFT SPCL 4	Disables ALC
SHIFT SPCL 9	Allows 20 dbm of vernier.
SHIFT SPCL 1 2 2	Linear Amplitude Sweep
SHIFT SPCL 2 0 4	Re-enables ALC
SHIFT SPCL 2 0 9	Range Hold Off
SHIFT SPCL 2 2 2	Log Amplitude Sweep

Adjustments

DESCRIPTION OF A13 ADJUSTMENTS

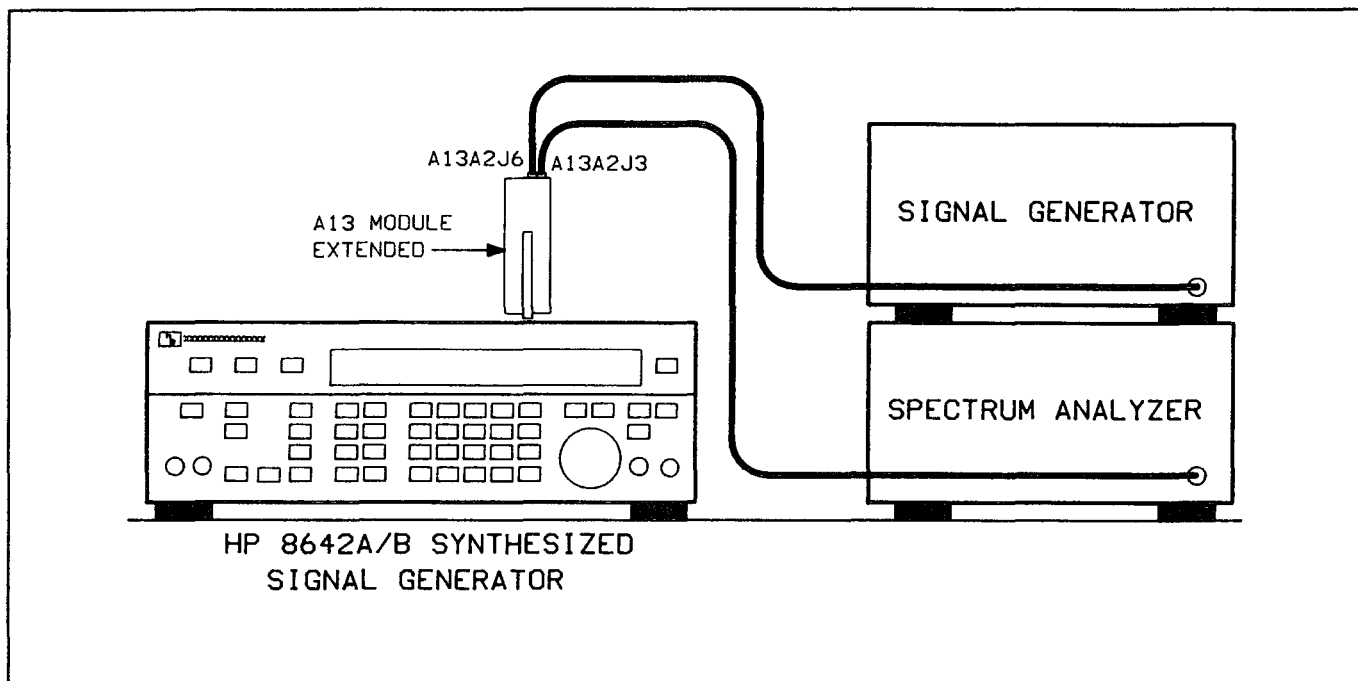
The A13 manual adjustment procedure adjusts the HF1 and HF2 low pass filters on the A13A1 Low Pass Filter Assembly for a passband ripple of ± 2 dB and a stopband rejection of at least -20 dB at one octave above the filters lowest used passband frequency. After the Manual Adjustment Procedure the A13 Auto-Adjust Procedure is ran, after which the A13A2 non-linearity compensation adjustment is adjusted for minimum AM distortion.

Overall Equipment List

Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
HP-IB Printer	HP 2225A
DVM	HP3456A
Spectrum Analyzer	HP 8566A/B
Semi-Rigid Adapter Cable	08642-2009

NOTE

Each adjustment procedure assumes the HP 8642 cabling is connected normally and all circuitry is functioning properly.

ADJUSTMENT 1: A13 MODULE*Figure 8P-1. Adjustment 1 Set-up***Required Equipment:**

Spectrum Analyzer	HP 8566A/B
Signal Generator No. 2	HP 8642B

Procedure**Low Pass Filter Adjustment****1. Setup:**

Set the HP 8642 POWER switch to STBY.

Extend the A13 Module on extender posts. (Refer to Instrument Disassembly Procedures if unfamiliar with this.)

Remove W32 from A13A2 J6.

Set Signal Generator No. 2 to sweep from 528.75 MHz to 1057.5 MHz, 0 dBm output, sweep time 10 seconds.

Connect Signal Generator No. 2 to A13A2 J6.

Remove W34 from A13A2 J3.

Connect the Spectrum Analyzer to A13A2 J3.

Set the Spectrum Analyzer to view frequencies from 525 MHz to 1100 MHz, reference level +10 dBm.

Set the HP 8642 POWER switch to ON.

NOTE

Do not remove the A13A1 cover to perform this adjustment. The adjustments must be made through the access holes provided in the A13A1 cover.

2. Adjust HF2 Low Pass Filter:

Set the HP 8642 frequency to 600 Mhz, amplitude to +5 dBm.

The Spectrum Analyzer should display a sweeping signal between 528.75 MHz and 1057.5 MHz, with the level at 528.75 MHz approximately -1 dBm.

Adjust A13A1 C1, C2 and C3 for a HF2 filter passband response of ± 2 dB between 528.75 MHz and 747.5 MHz and a stopband response of -20 dB, at 1057.5 MHz relative to the level at 528.75 MHz.

3. Adjust HF2 Low Pass Filter:

Set Signal Generator No. 2 to sweep from 747.5 MHz to 1500 MHz, -10 dBm output, sweep time 10 seconds.

Set the Spectrum Analyzer to view frequencies from 740 MHz to 1500 MHz, reference level +10 dBm.

Set the HP 8642 frequency to 900 Mhz, amplitude to +5 dBm.

The Spectrum Analyzer should display a sweeping signal between 747.5 MHz and 1500 MHz, with the level at 747.5 MHz approximately -1 dBm.

Adjust A13A1 C4 and C5 for a HF1 filter passband response of ± 2 dB between 747.5 MHz and 1057.5 MHz and a stopband response of -20 dB, at 1495 MHz relative to the level at 747.5 MHz.

A13 AUTO-ADJUSTMENTS

Description

The A13 Auto-Adjustment Procedure generates data that is used for three main functions of the output module. These are: 1) Rf level accuracy (ALC mode), 2) RF level accuracy (pulse/ALC off mode), and 3) AM accuracy.

The first step of the procedure will have you adjust R77 (detector compensation) full counter-clockwise. Once the auto-adjust portion of the procedure is completed, you will re-adjust R77 (detector compensation) for a symmetrical waveform. In the ALC mode, N1 is the difference between 20 dbm and the actual measurement. N2 is the gain correction factor and is generated by setting the amplitude to 5 dbm (using N1) measuring the error, and dividing by 15. Using a formula a lookup table is generated for every tenth db of power from 5 dbm to 20 dbm and stored in a ROM on the processor board.

Now that the vernier range is calibrated, the error due to frequency is calibrated out by measuring the level of 10 dbm at 17 frequency points from 4.13MHz to 1057.5 MHz. This is stored in an array called N3.

In the PULSE/ALC mode, DAC numbers are generated for power levels of 4 dbm and 23 dbm every 50 MHz with the end points of 4.13085 MHz and 1057.5 MHz. These Dac numbers are stored as ALC open cal data points.

The AM accuracy calibration points are generated as follows: NAM2 is the total voltage range of the output level DAC. The AM calibration data points are generated at the same frequencies as the N3 points and is the detector offset voltage required to achieve the AM depth set.

Required Equipment:

Measuring Receiver	HP8902A
Sensor Module	HP11722A
HP-IB Printer	HP2225A
DVM	HP3456A

NOTE

Read Section 5 before performing this procedure.

Procedure

1. Initialize Auto Adjust Routine:

Connect the Required Equipment to the HP 8642 via HP-IB. (Required equipment listed above. See Section 5 for more details.)

Key in: **INST PRESET**

Key in: **SHIFT SPCL 3 8 8 Hz 8 0 Hz.**

Key in: **4 Hz** when "ENTER ROUTINE NUMBER .G8000" appears.

Key in the the Day, Month, Year and Module Cal ID Number when prompted by the HP 8642 display. (See Section 5 for details.)

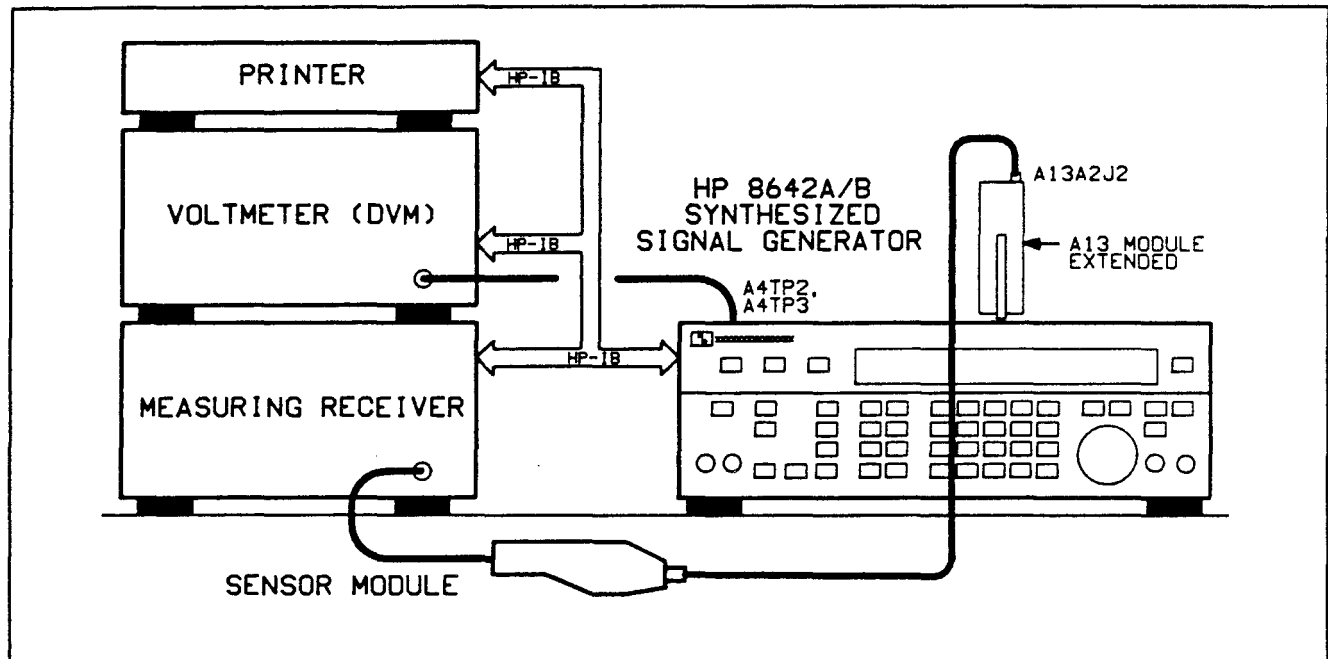


Figure 8P-2. Set-Up 1

2. When "WAITING FOR SET-UP 1 .V24" appears:

Ensure the Sensor Module is connected to the Measuring Receiver and that the Measuring Receiver's Power Meter is zeroed and calibrated.

Connect the HP 8642's voltmeter out test points: A4 TP2 VM OUT to the DVM HI input, and A4TP3 GND to the DVM LO input.

Set the DVM to measure volts DC.

Disconnect W34 from A13A2J3 and extend the A13 module.

Adjust A13R77 to its fully counter-clockwise position. (R77 is located on the right side of the A13 Module)

Press **[Hz]** to continue. (Run time \approx minute) 1 minute.

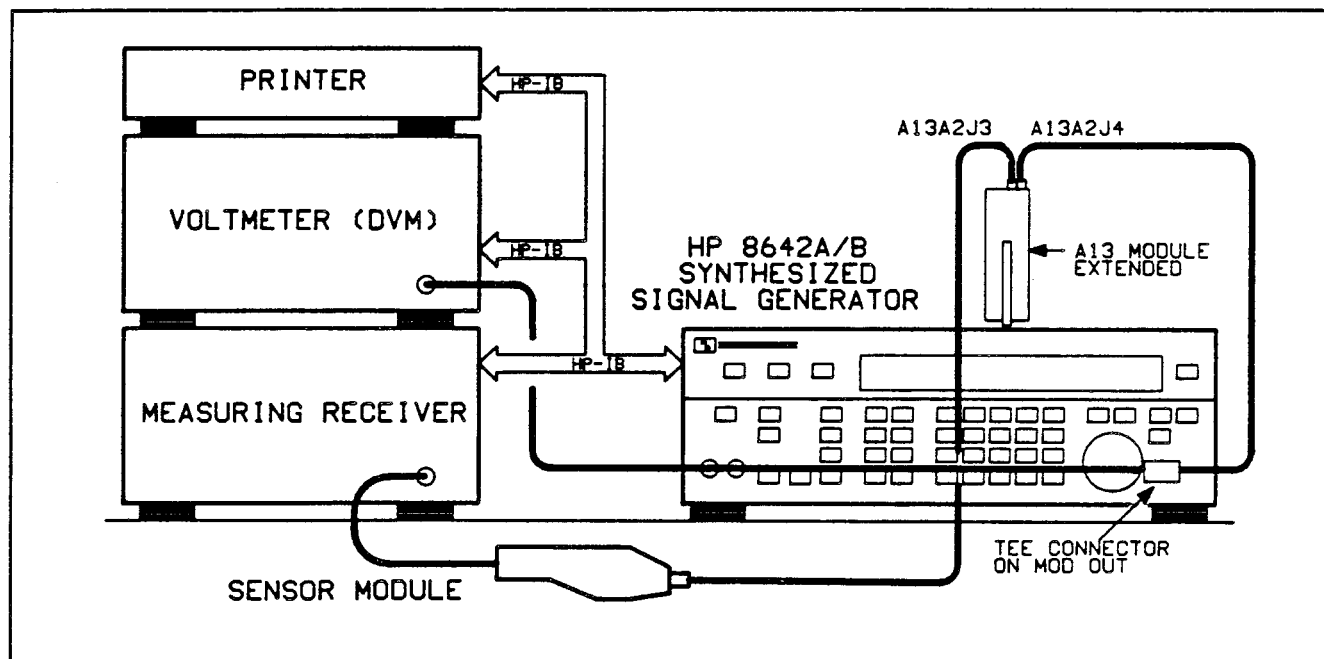


Figure 8P-3. Set-Up 2

3. When **"WAITING FOR SET-UP 2 .V25"** appears:

Connect a BNC tee to the mod output port on the HP 8642.

Connect a BNC cable from the tee to the DVM.

Set the DVM to volts AC.

Disconnect W22 (90) from the A13 module at A13A2J4.

Connect a BNC cable from the tee connector to A13A2J4.

Connect the HP 11722A Power Sensor to A13A2J3 using the semi-rigid cable supplied in the on site service kit. (HP 08642-20099)

Press **[Hz]** to continue. (Run time \approx 150 minutes)

4. When **"UNPROTECT CAL. MEMORY .G8005"** appears:
Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.
Press **[Hz]** to Continue.
5. When **"PROTECT CAL. MEMORY .G8006"** appears:
Switch A3 S2 toward the front of the instrument to protect the EEPROM's.
Press **[Hz]** to Continue.
6. When **"RECONNECT ALL CABLES .V29"** appears:
Disconnect all test cables from the instrument.
Reconnect any instrument cables which are still disconnected.
Press **[Hz]** to Continue.
7. Re-adjust A13A2 R77.

NOTE

Do not remove the A13A2 cover to perform this adjustment. The adjustment must be made through the access hole provided in the A13A2 cover for R77.

Press **[INST PRESET]** on the HP 8642.

Set the HP 8642 amplitude to +5 dBm.

Connect the Sensor Module to A12A2 J3.

Set the Measuring receiver to measure AM distortion at a 1 kHz rate.

On the HP 8642 press **[AM]** **[On]**, **[90]** **[%]**.

Adjust A13A2 R77 for minimum distortion on the Measuring Receiver. (Must be less than 4%.)

Re-install the A13 module into the instrument.

Reconnect all instrument cabling.

8. Run the instrument level diagnostics to verify operation:
Key in: **[SHIFT]** **[SPCL]** **[3]** **[3]** **[0]** **[Hz]**.
When **"WAITING FOR SETUP 1 .Z24"** appears, connect the MOD OUT to the AM/PULSE INPUT and FM/ΦM INPUT.
Press **[Hz]** to Continue.
9. When **"DIAG DONE HIT MSSGS .V1"** appears:
Press the MSSG key to view the message buffer. If **"NO MESSAGES .00"** is contained in the message buffer, the HP 8642 is functioning properly.

Scans by Artekmedia => 2009**10. Up Load Cal Data:**

Now that the functionality of the HP 8642 has been verified, use the following procedure to up load the new cal data.

Switch the HP 8642 to standby.

Remove the A20 Cal Module. (See Disassembly Procedures).

Plug the A20 Module on to A3 J3.

Switch the HP 8642 on.

Switch A20 S1 to the CHANGE position.

Key in: **SHIFT** **SPCL** **3** **7** **2** **4** **Hz**.

When "**TRANSFER VERIFIED .U613**" appears on the display, move A20 S1 up to its **PROTECTED** position.

Key in: **Hz** to end the routine.

Switch the HP 8642 to Standby.

Reconnect the A20 module to the rear panel (See Disassembly Procedures).

Re-install the top cover.

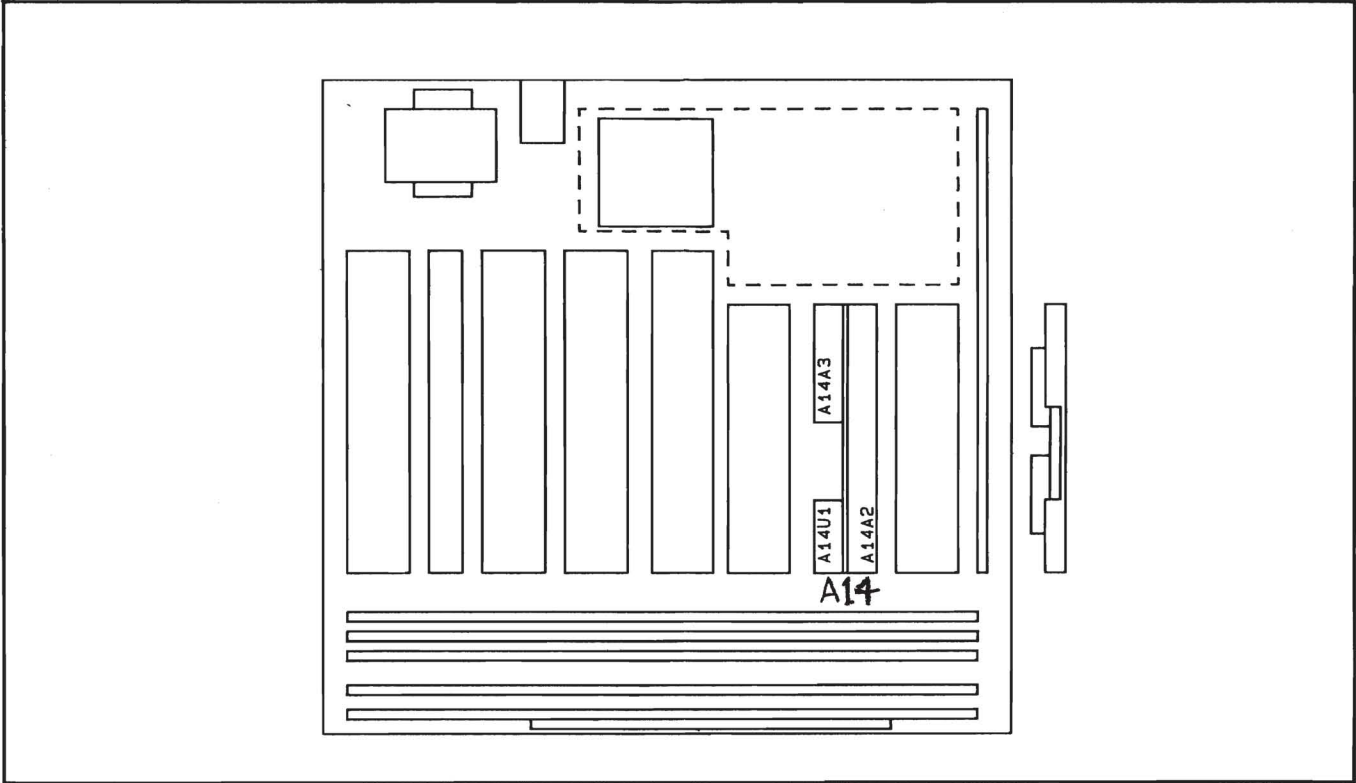
Table 8P-44. A13 Output Specifications

Electrical Characteristics	Conditions	Specifications
AM Accuracy	18 dBm at A13A2J3	$\pm 3.5\%$ of Setting +1%
AM Distortion @ 1kHz Rate	0-30% 30-70% 70-90%	<1% <2% <4%
Incidental PM (1kHz Rate 30% AM)		<.2 Radius
Residual AM	0.3 to 3.0 kHz Rate	<.01% AM RMS
Incidental AM	20 kHz Peak DEV 1kHz Rate > 400 kHz Carrier Freq @ $\leq +15$ dBm	<.2% Radius $\leq .3\%$
Pulse Modulation ON/OFF Ratio Rise Time/Fall Time Maximum Repetition Frequency Maximum Pulse Width Normal Input Threshold	@ ≤ 15 dBm 10% to 90% External DC	> 40 dB <3.5 μ 50 kHz 6 μ s 1.5 Vdc
Harmonics	@ ≤ 10 dBm @ ≤ 16 dBm	-30 dBc -20 dBc
Spurs	> 10 kHz From Carrier	≤ 100 dBc
Maximum Power OUT 4.13 to 50 MHz 50 to 200 MHz 200 to 500 MHz 500 to 1057.5 MHz	At ≥ 5 dBm Input At A13A2J6	≥ 21.2 dBm ≥ 22.5 dBm ≥ 21.5 dBm ≥ 20.5 dBm
Modulator Dynamic Range		≥ 40 dBm
Filter Insertion Loss HF1 HF2 HF3 HF4 HF5 HF6 HF7 HF8 LF1 LF2 LF3 LF4 LF5 LF6 LF7 LF8	747.800001 to 1057.5 MHz 528.750001 to 747.8 MHz 373.900001 to 528.75 MHz 264.400001 to 373.9 MHz 187.000001 to 264.4 MHz 132.200001 to 187 MHz 93.800001 to 132.2 MHz 66.100001 to 93.5 MHz 46.700001 to 66.1 MHz 33.050001 to 46.7 MHz 23.400001 to 33.05 MHz 16.500001 to 23.4 MHz 11.700001 to 16.5 MHz 8.260001 to 11.7 MHz 5.850001 to 8.26 MHz 4.130001 to 5.85 MHz	≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm ≈ 4 dBm

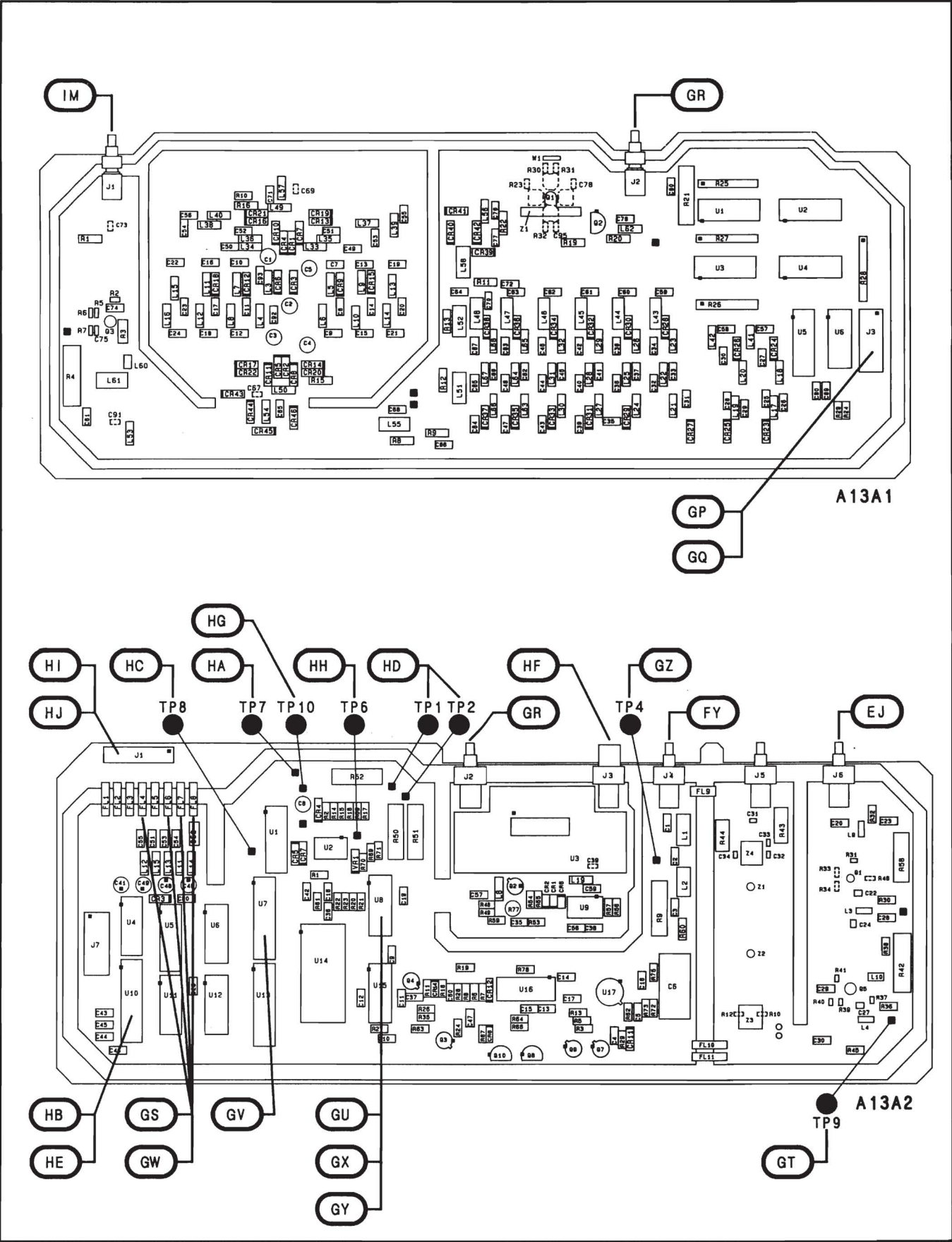
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**SCANS
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Assembly Locator



Module Test Point/Adjustment Locations



Simplified Block Diagram

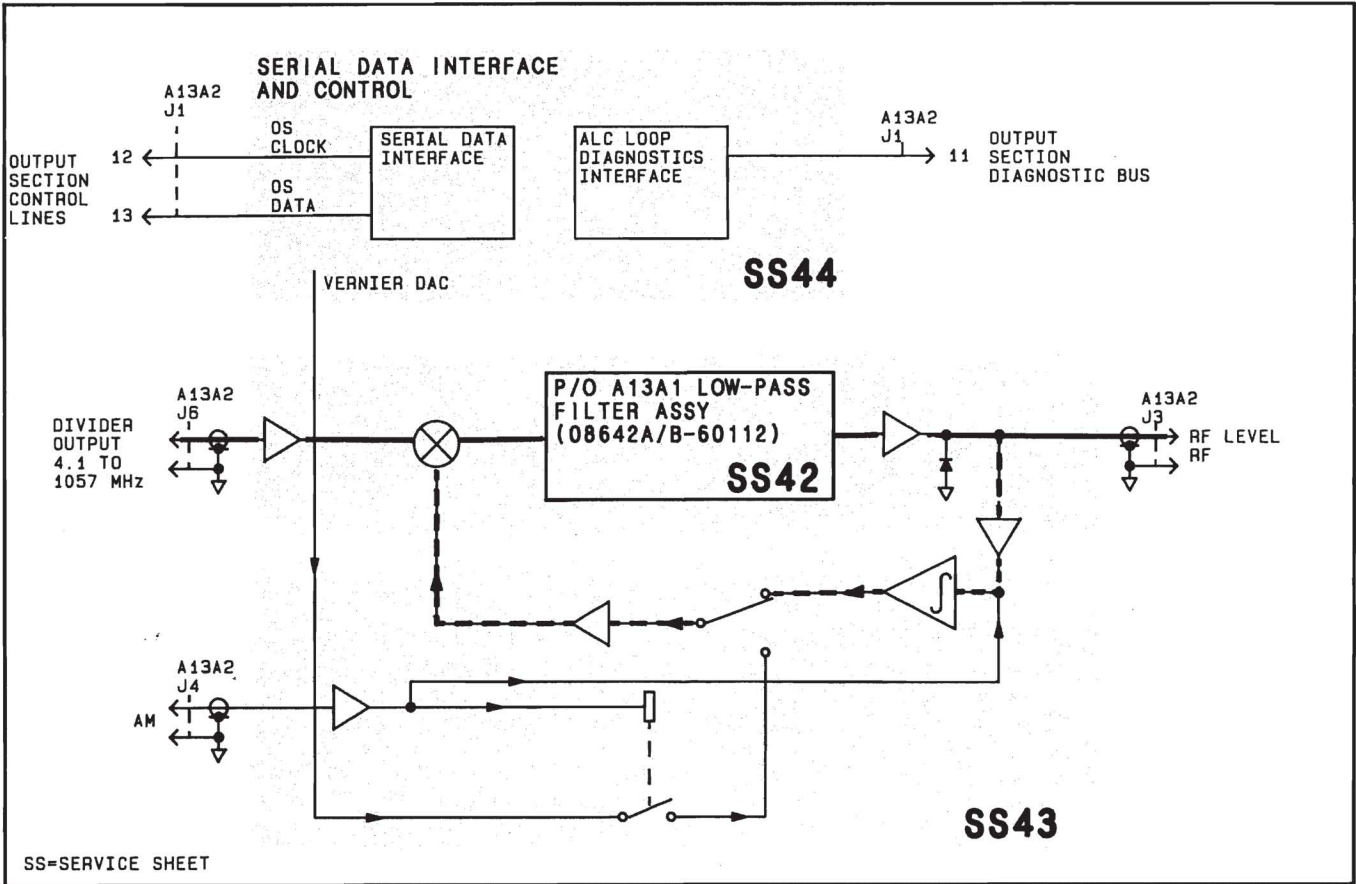


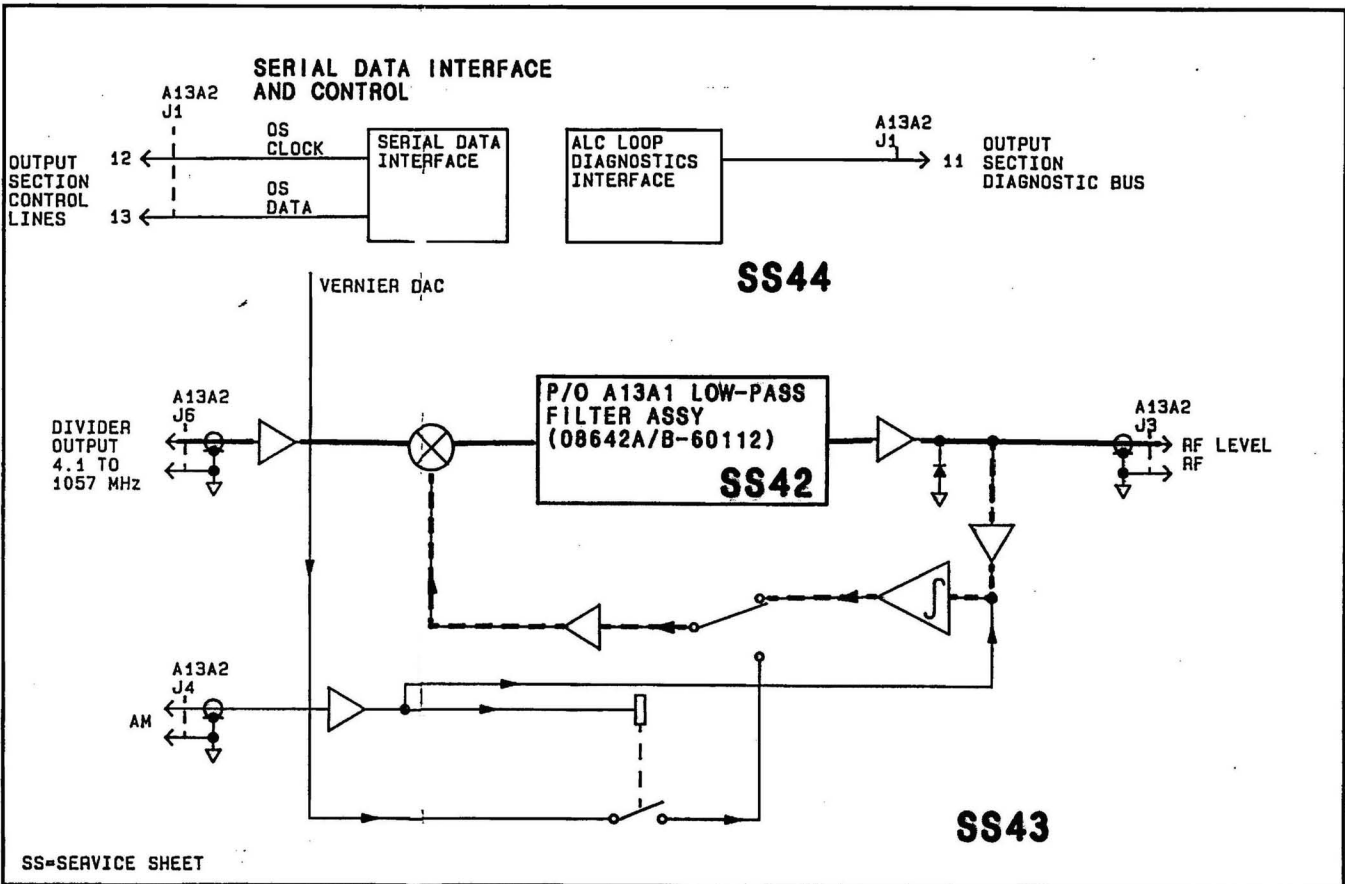
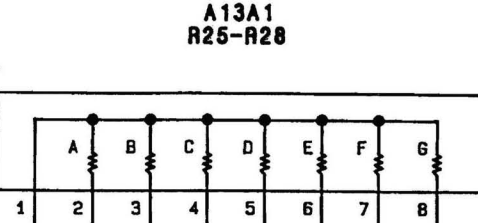
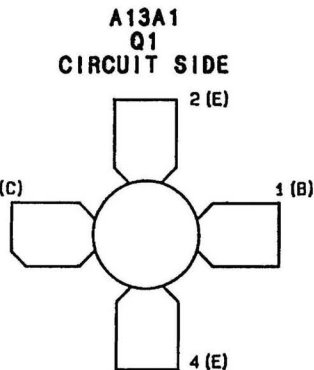
Figure 8P-100 BD14 General Information.

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**SCANS
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Notes:

- 1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- 2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
- 3. L69 is a printed circuit trace inductor.
- 4. Z1 is acting as a ground strap, connecting the stud of Q1 to ground.



Reference Block Diagram
Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	B,2	C39	C,3	C76	C,1	CR19	B,1	L7	A,2	L44	C,2	R9	B,3						
C2	B,2	C40	C,3	C77	C,1	CR20	B,3	L8	A,2	L45	C,2	R10	A,1						
C3	B,2	C41	C,3	C78	C,1	CR21	A,1	L9	B,2	L46	C,2	R11	C,2						
C4	B,2	C42	C,3	C79	C,1	CR22	A,3	L10	B,2	L47	C,2	R12	B,3						
C5	B,2	C43	C,3	C80	C,1	CR23	D,3	L11	A,2	L48	B,2	R13	B,2						
C6	B,2	C44	C,3	C81	D,2	CR24	D,2	L12	A,2	L49	B,1	R15	B,3						
C7	B,2	C45	C,3	C82	C,3	CR25	D,3	L13	B,2	L50	B,3	R16	A,1						
C8	B,2	C46	C,3	C83	C,2	CR26	D,2	L14	B,2	L51	B,3	R19	C,1						
C9	B,2	C47	C,3	C84	B,3	CR27	C,3	L15	A,2	L52	B,2	R20	C,1						
C10	A,2	C48	A,3	C85	B,3	CR28	C,3	L16	A,2	L53	A,3	R21	C,1						
C11	A,2	C49	B,1	C86	C,3	CR29	C,3	L17	D,3	L54	B,3	R22	C,1						
C12	A,2	C50	A,1	C87	B,2	CR30	C,2	L18	D,3	L55	B,3	R23	C,1						
C13	B,2	C51	B,1	C88	D,3	CR31	C,3	L19	D,3	L56	C,1	R24	D,3						
C14	B,2	C52	A,1	C89	D,3	CR32	C,2	L20	D,3	L57	B,1	R25	D,1						
C15	A,2	C53	A,1	C90	D,3	CR33	C,2	L21	A,1	L58	B,2	R26	B,2						
C16	A,2	C54	A,1	C91	A,3	CR34	C,2	L22	C,3	L59	B,2	R27	D,1						
C17	A,2	C55	B,1	C92	B,2	CR35	C,3	L23	C,2	L60	C,2	R28	D,2						
C18	A,2	C56	A,1	C93	B,2	CR36	C,2	L24	C,3	L61	A,3	R29	D,3						
C19	B,2	C57	D,2	C94	C,1	CR37	C,3	L25	C,3	L62	C,1	R29	D,3						
C20	B,2	C58	D,2	CR1	B,1	CR38	C,3	L26	C,3	L63	C,2	R30	C,1						
C21	B,2	C59	C,2	CR2	B,3	CR39	C,1	L27	C,3	L64	C,2	R31	C,1						
C22	A,2	C60	C,2	CR3	B,2	CR40	B,1	L28	C,3	L65	C,3	R32	C,1						
C23	A,2	C61	C,2	CR4	B,1	CR41	B,1	L29	C,2	L66	C,3	TP1	A,2						
C24	A,2	C62	C,2	CR5	B,3	CR42	B,1	L30	C,3	L67	C,3	TP2	C,1						
C25	D,3	C63	C,2	CR6	B,3	CR43	A,3	L31	C,3	L68	C,2	TP3	B,3						
C26	D,3	C64	B,2	CR7	B,1	CR44	A,3	L32	C,2	Q1	C,1								
C27	D,2	C65	B,3	CR8	B,3	CR45	B,3	L33	B,1	Q2	C,1	U1	D,1						
C28	D,3	C66	B,3	CR9	B,2	CR46	B,3	L34	A,1	Q3	A,2	U2	D,1						
C29	D,3	C67	A,3	CR10	B,1			L35	B,1			U3	D,2						
C30	D,2	C68	B,3	CR11	B,3	J1	A,1	L36	A,3	R1	A,1	U4	D,2						
C31	C,3	C69	B,1	CR12	A,2	J2	C,1	L37	B,1	R2	A,2	U5	D,2						
C32	C,3	C70	C,2	CR13	B,1	J3	D,2	L38	A,1	R3	A,2	U6	D,2						
C33	C,3	C71	B,1	CR14	B,3			L39	B,1	R4	A,3								
C34	C,2	C72	C,2	CR15	B,2	L3	B,2	L40	A,1	R5	A,2								
C35	C,3	C73	C,2	CR16	A,1	L4	B,2	L41	D,2	R6	A,2								
C36	C,3	C74	A,2	CR17	A,3	L5	B,2	L42	D,2	R7	A,2								
C37	A,2	C75	A,2	CR18	A,2	L6	B,2	L43	C,2	R8	B,3								
C38	C,2																		

A13 MODULE **BD 14**

SEE REVERSE SIDE

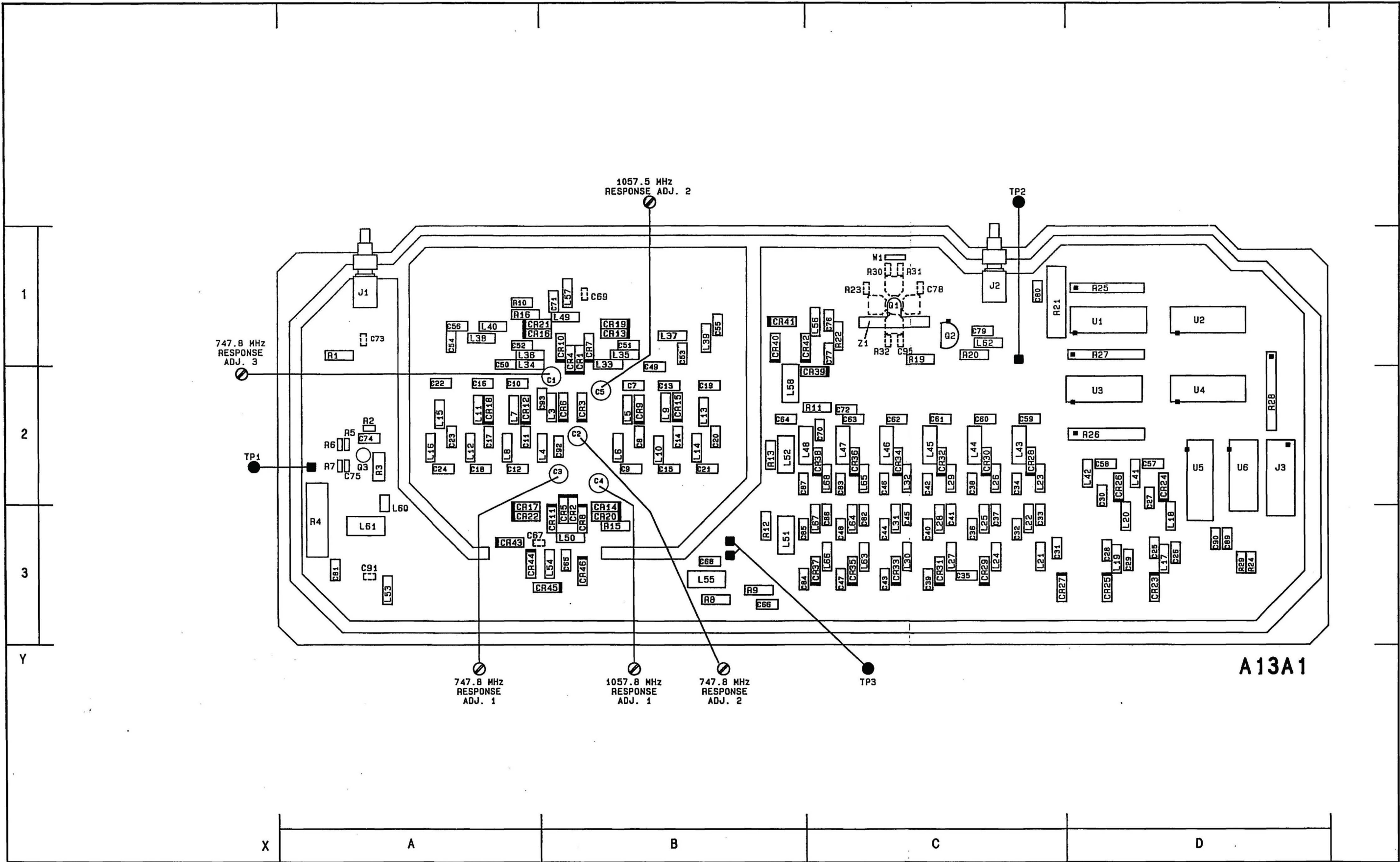


Figure 8P-102. SERVICE SHEET 42 INFORMATION

Component Locator

CHANGES

All Serial Prefixes

On the Component Locator:

- CR51, CR52 - Immediately above C19, add CR51. Immediately above C22, add CR52.

In Component Coordinates:

- CR51, CR52 - Add CR51 B,2. Add CR52 A,2.

On the schematic:

- To the left of **RF INPUT AMPLIFIER**, change "44" to "43" next to the bullet "IM".
- To the right of **RF OUTPUT AMPLIFIER**, change "44" to "43" next to the bullet "GR".
- CR51, CR52 - In **SWITCHED HIGH FREQUENCY FILTERS**, in the 132.2 MHz filter, add CR51 (same symbol as CR19) from the cathode of CR19 to ground. Orient CR51 with its cathode to ground. Directly below, in the 93.5 MHz filter, add CR52 from the cathode of CR21 to ground in the same orientation and same symbol as CR51.
- C29, C38 - In **SWITCHED LOW FREQUENCY FILTERS**, in the 46.7 MHz filter, change the value of C29 to 160p. In the 23.4 MHz filter, change C38 to C42 and assign it a value of 220p.
- C27, C35 - In **SWITCHED LOW FREQUENCY FILTERS**, in the 66.1 MHz filter, change the value of C27 to 68p Farads. In the the 23.4 MHz filter, change the value of C35 to 150p Farads.
- HF 5 - In **SWITCHED HIGH FREQUENCY FILTERS**, change HF 5 frequency from 246.4 to 264.4 MHz.
- To the left of **SWITCH DRIVE LOGIC**, change the service sheet number for **FILTER SELECT LINES**, "GP" from 43 to 44.
- In **SWITCHED LOW FREQUENCY FILTERS**, in the 16.5 MHz filter, change the reference designator for C38 to C42.

CHANGES

2511A to 2550A

On the Component Locator:

- Note changes on 8P-102.6

On the schematic:

- In the upper left portion of the schematic, change A13A1 part number to 08642-60212.
- R3, R5, R6, R7, C75 - In **RF INPUT AMPLIFIER**, change R3 value to 178. Change R5, R6, and R7 values to 42.2 ohms. Change C75 value to 3.3p.
- C26, C85, C86 - In the **SWITCHED LOW FREQUENCY FILTERS**, change C26 value to 120p. (C26 is in the 66.1 MHz filter). Change C85 and C86 values to 1100p. (C85 and C86 are in the 5.85MHz filter).
- Replace the appropriate portion of the schematic with the partial on 8P-102.5.
- Note: The 08642-60212 board ground comes from the 08642-60213 board by the outer conductor of the coax cables and the castings.

2512A to 2550A

On the schematic partial:

- C97 - On change page 8P-102.5, in **OUTPUT PATH SWITCH** add C97, 1p, from the anode of CR41 to ground. Change the caption below the schematic partial to read "CHANGES TO FIGURE 8P-103 (2512A to 2550A)"
- To the right of **RF OUTPUT AMPLIFIER**, change "44" to "43" next to the bullet labeled "GR".

On the schematic:

- C74 - In **RF INPUT AMPLIFIER**, change the value of C74 to 1000p.

CHANGES**2529A to 2550A**

On the Component Locator:

- Note changes on page 8P-102.7

In Component Coordinates:

- C100, C101, R39 - Add C100, C101, and R39. Assign grid locations of C,1 for all three.

On the schematic partial:

- C100, C101, R39 - On change page 8P-102.5, in RF OUTPUT AMPLIFIER, add a resistor R39 in series with the cathode of CR50 and ground. Assign it a value of 220 ohms. In parallel with R39, add a capacitor, C100. Assign it a value of 220p Farads. Also in parallel with R39, add another capacitor, C101. Assign it a value of 220p Farads. Change the caption below the schematic partial to read "CHANGES TO 8P-103 (2529A to 2550A).

2534A to 2550A

On the schematic partial:

- C96, L70, R34, R35 - On change page 8P-102.5, remove the series path between U5 pin 11 and the anode of CR49. This path includes all parts listed above and amplifier U5G becomes unused. Change the caption below the schematic partial to read "CHANGES TO 8P-102.3 (2534A to 2550A).

2535A to 2550A

On the schematic:

- C25-C28, C30 - In SWITCHED LOW FREQUENCY FILTERS, in the 66.1 MHz filter, change the values of the following components to these new values:
 C25 - 47p
 C26 - 100p
 C27 - 47p
 In the 46.7 MHz filter, change the values of the following components to these new values:
 C28 - 82p
 C30 - 82p
 C29 - 160p

CHANGES

2551A and above

On the Component Locator:

- Note new Component Locator on page 8P-102.10.

In the Component Coordinates:

- Note new Component Coordinates table on page 8P-102.10.

On the schematic:

- C96, C97, C98, C99, R34, R35, R38, L70 - Note new SS42 on page 8P-102.11.

2728A and above

On the Component Locator:

- C98, R38 - Delete C98 and R38.

In Component Coordinates:

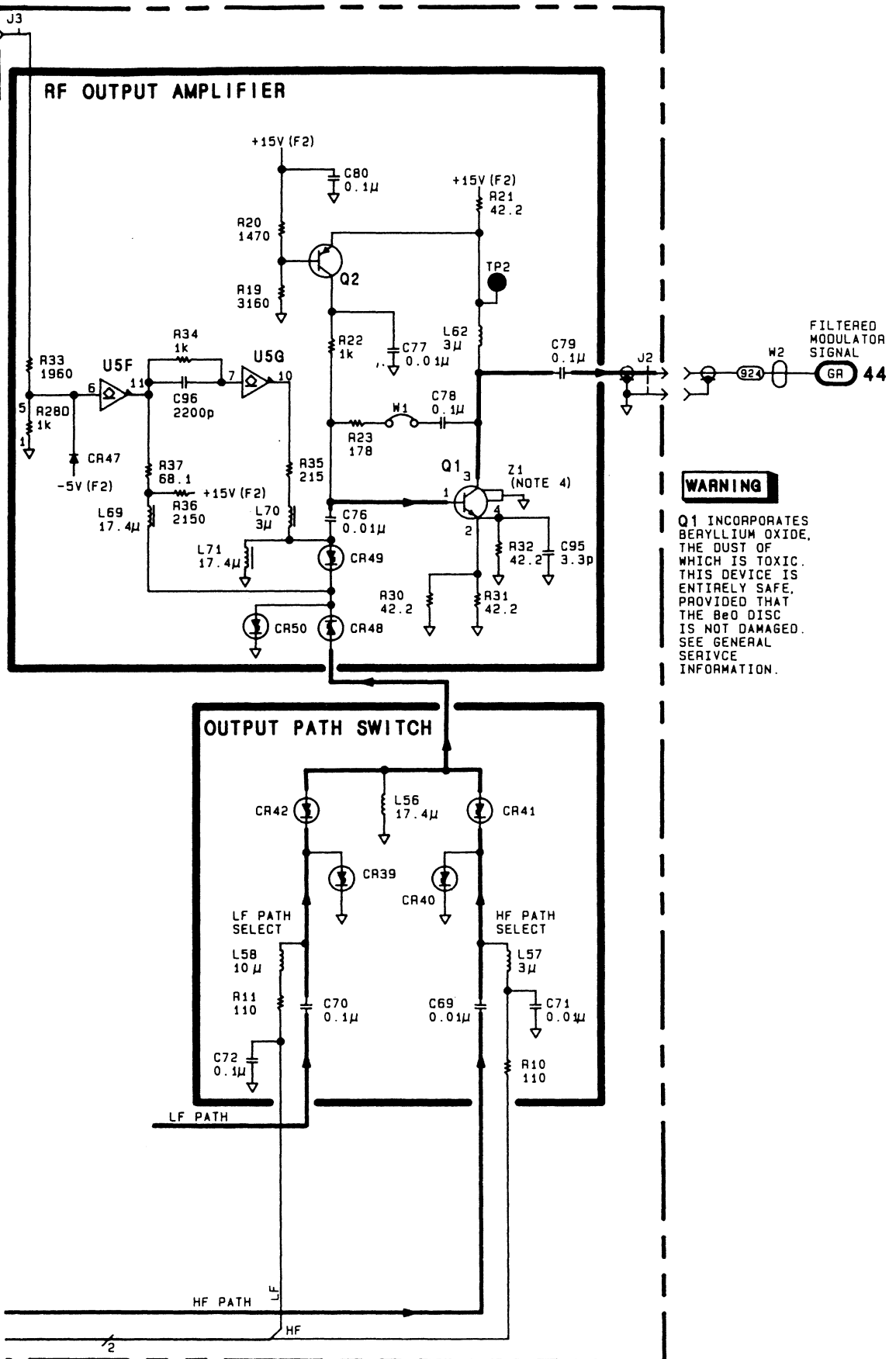
- C98, R38 - Delete C98 and R38.

On the schematic:

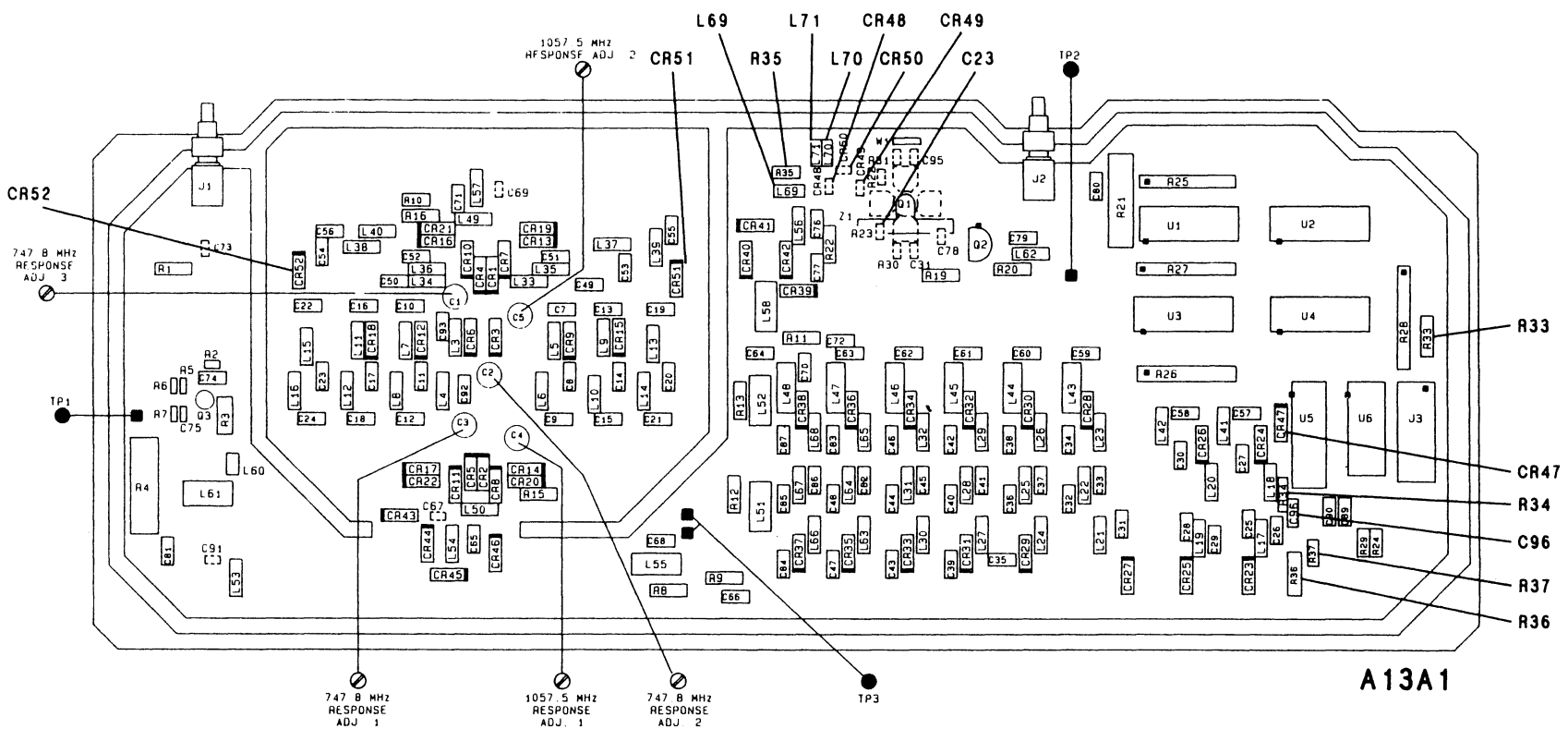
- C92, C93, L3, L4 - In **SWITCHED HIGH FREQUENCY FILTERS**, change C92 to 6.0p, C93 to 10p, L3 and L4 from 27nh to (jumper/wire).
- R38, C98 - In **RF OUTPUT AMPLIFIER**, delete R38 and C98 from the assembly.

PULSE MOD

43 (PM)

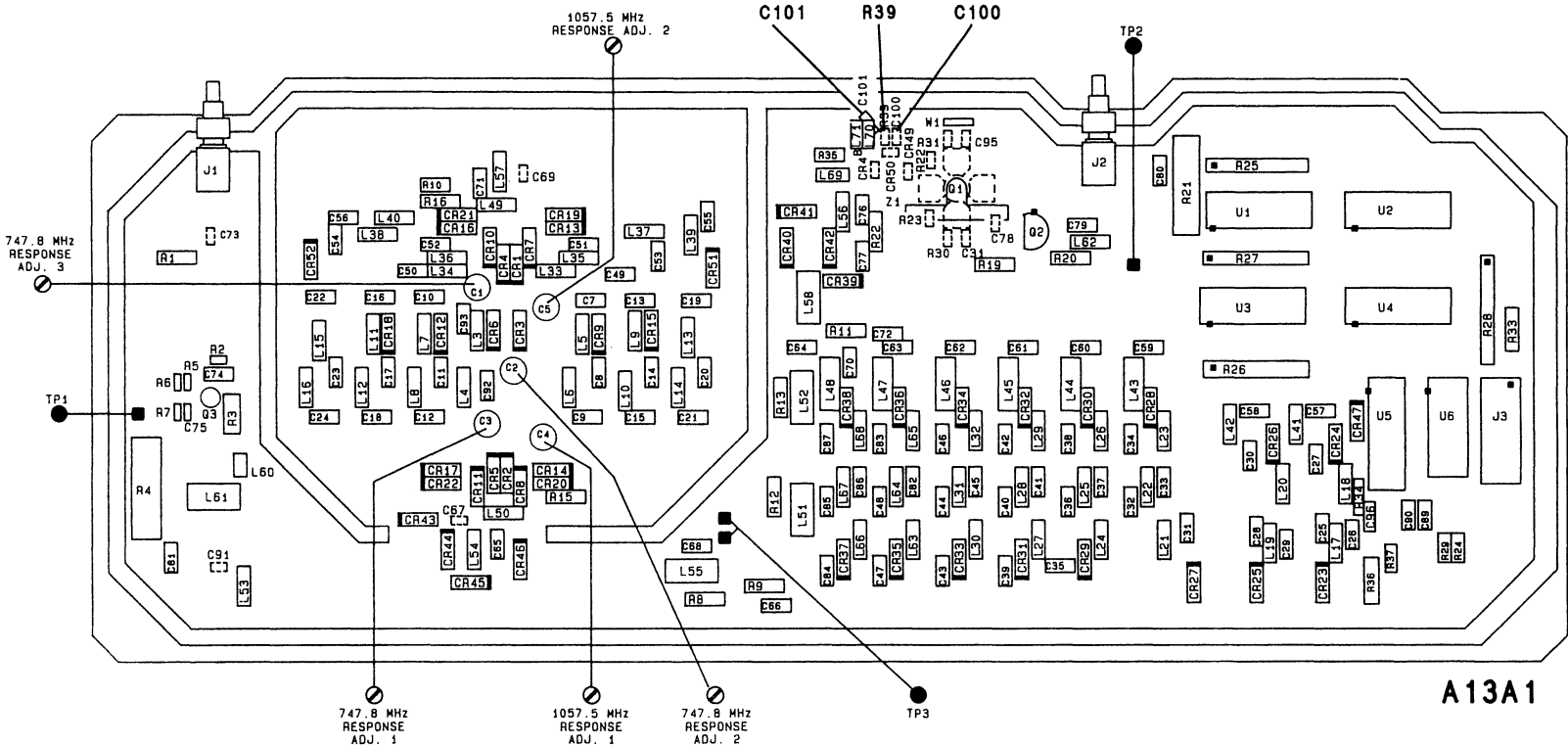


CHANGES TO FIGURE 8P-103 (2511A to 2550A)

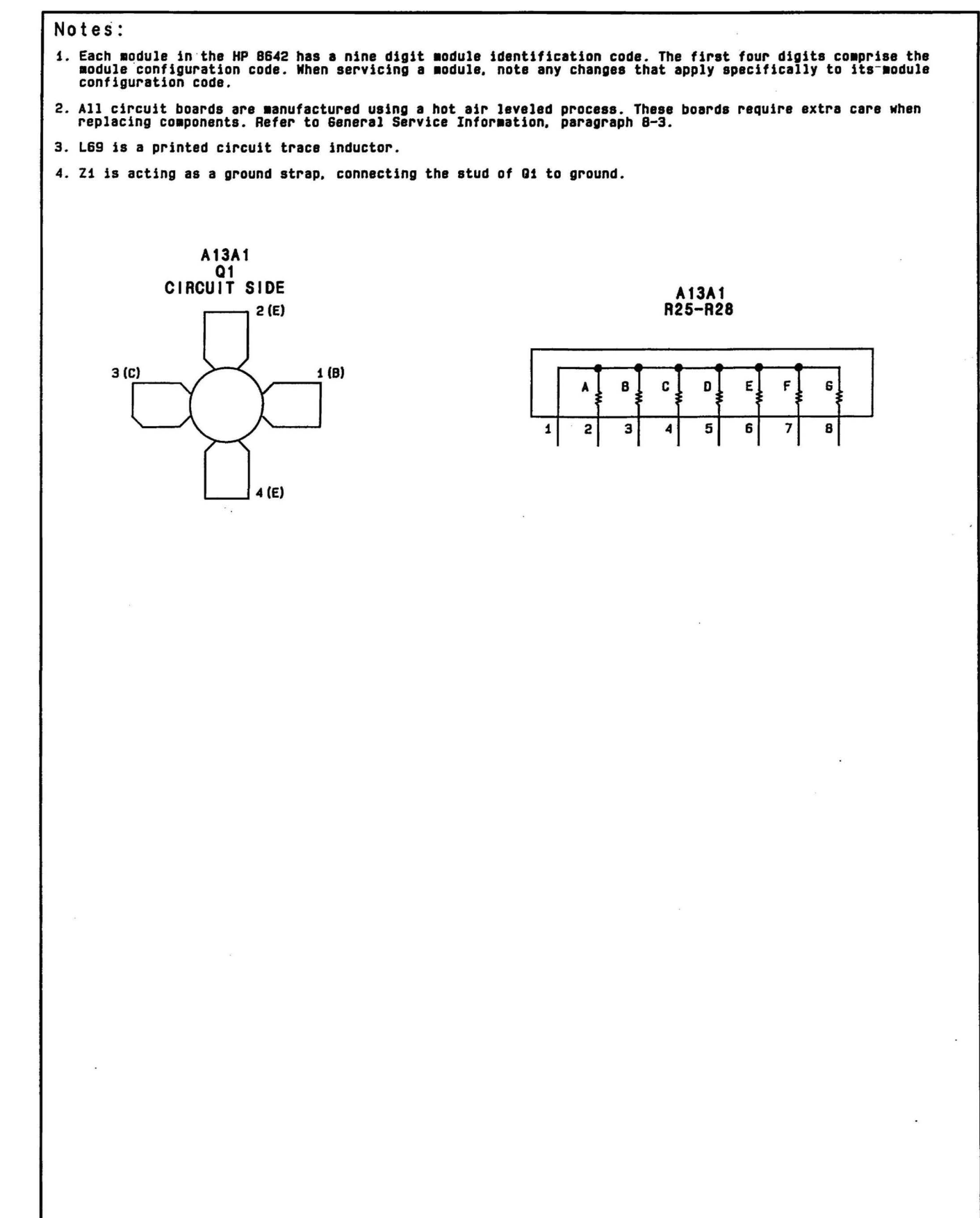


CHANGES TO FIGURE 8P-102 (2511A to 2550A)

SS42
8P-102.6

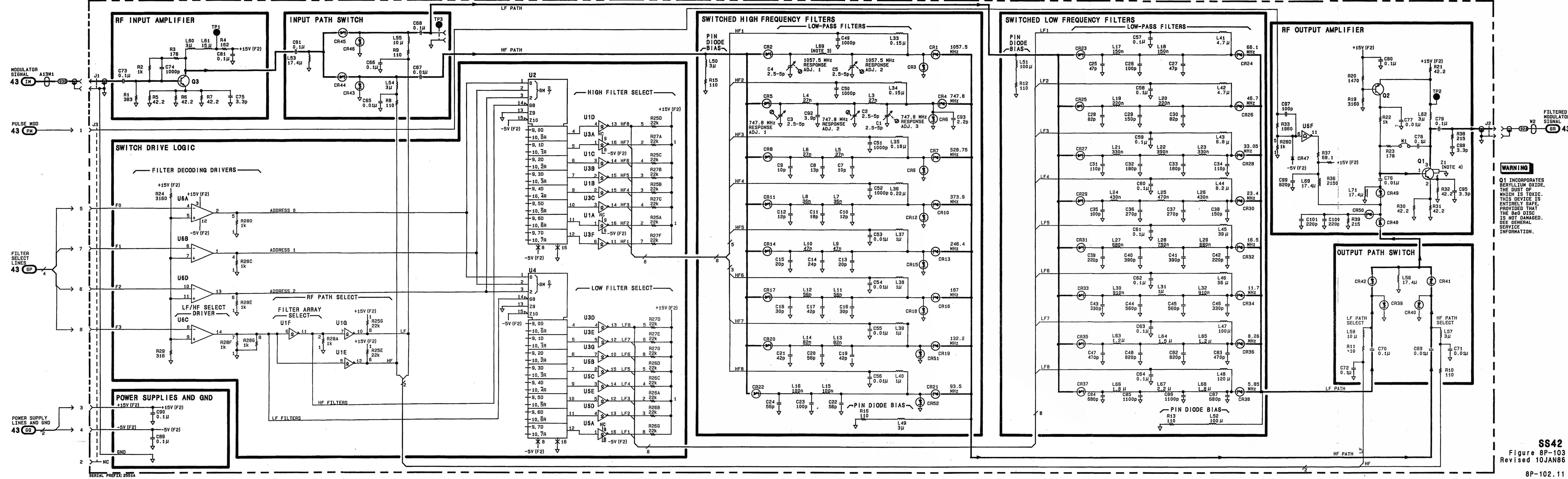


CHANGES TO FIGURE 8P-102 (2529A to 2550A)



Schematic General Information

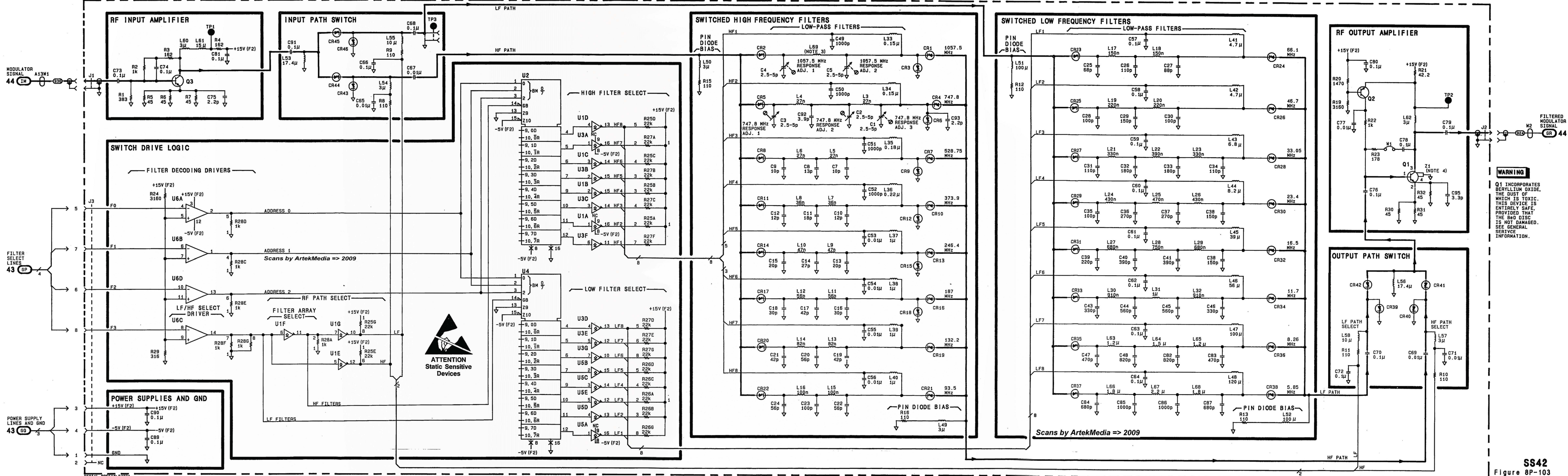
A13A1 LOW PASS FILTER ASSEMBLY (08642-60312)



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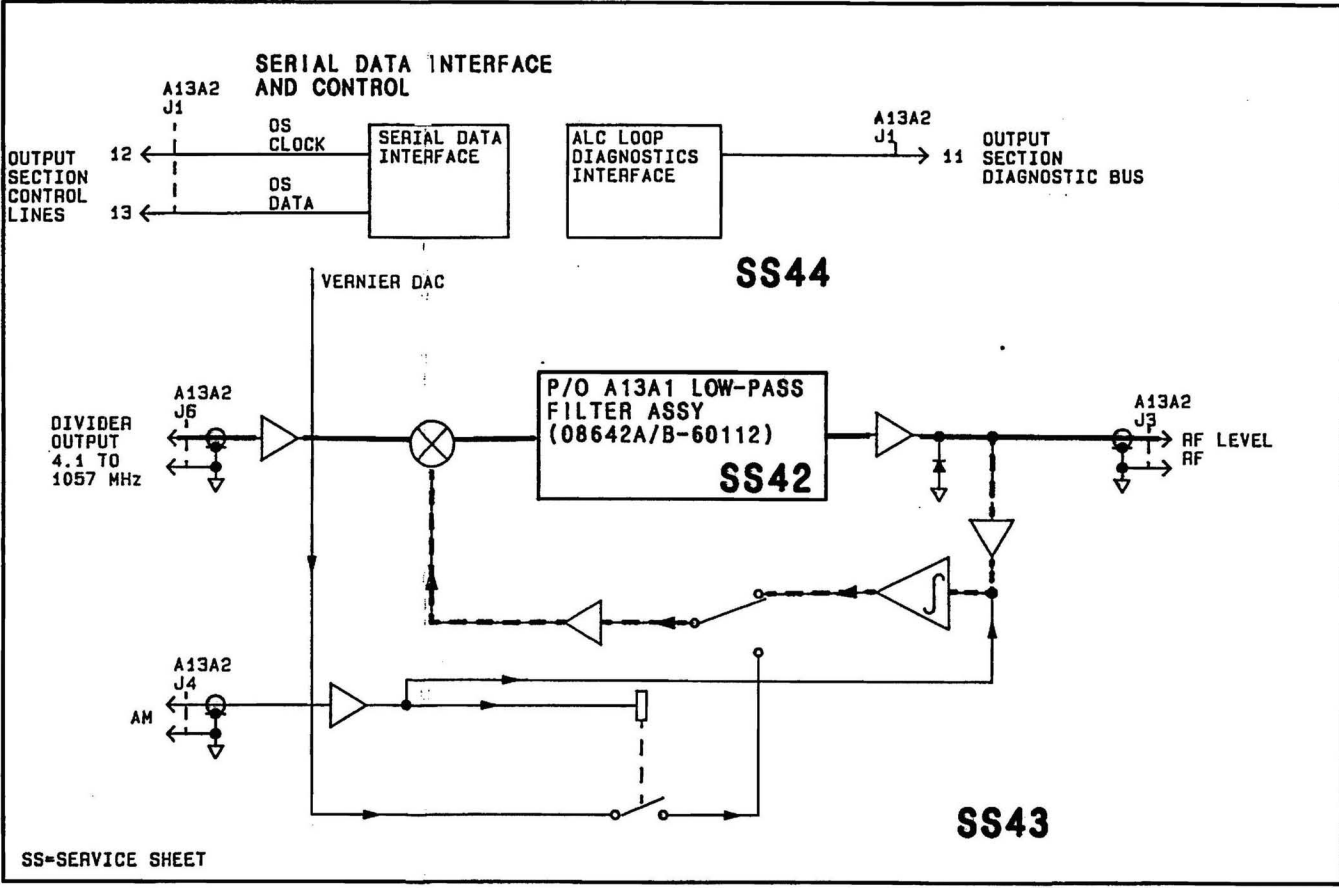
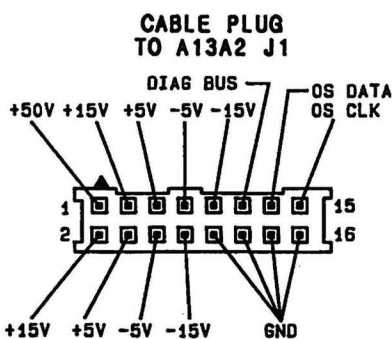
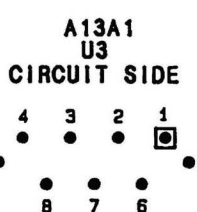
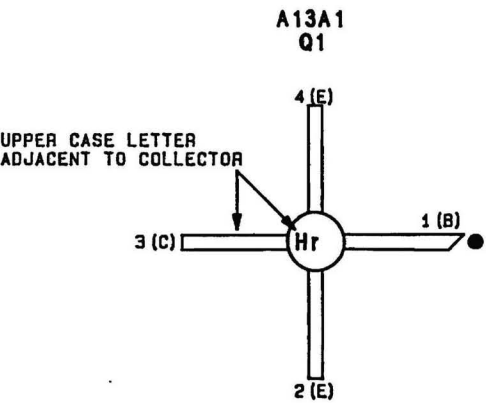
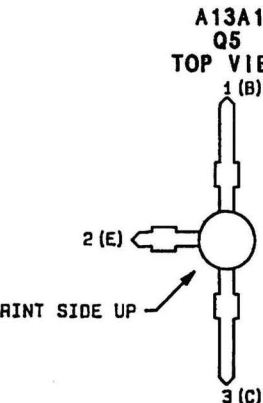
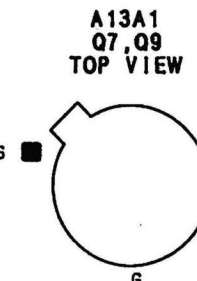
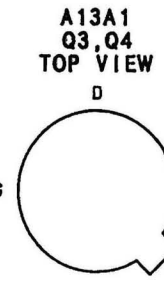
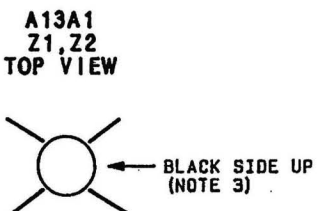
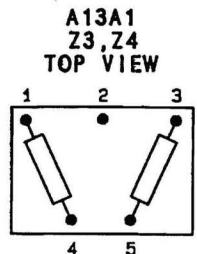
**SCANS
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A13A1 LOW PASS FILTER ASSEMBLY (08642-60112)



Notes:

- 1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- 2. FL9 outer body must be soldered to pad in notched area of shielding.
- 3. Z1, Z2 are diode rings as shown on schematic. Pin numbering is not shown because devices can be oriented any way and still operate properly.
- 4. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph B-3.

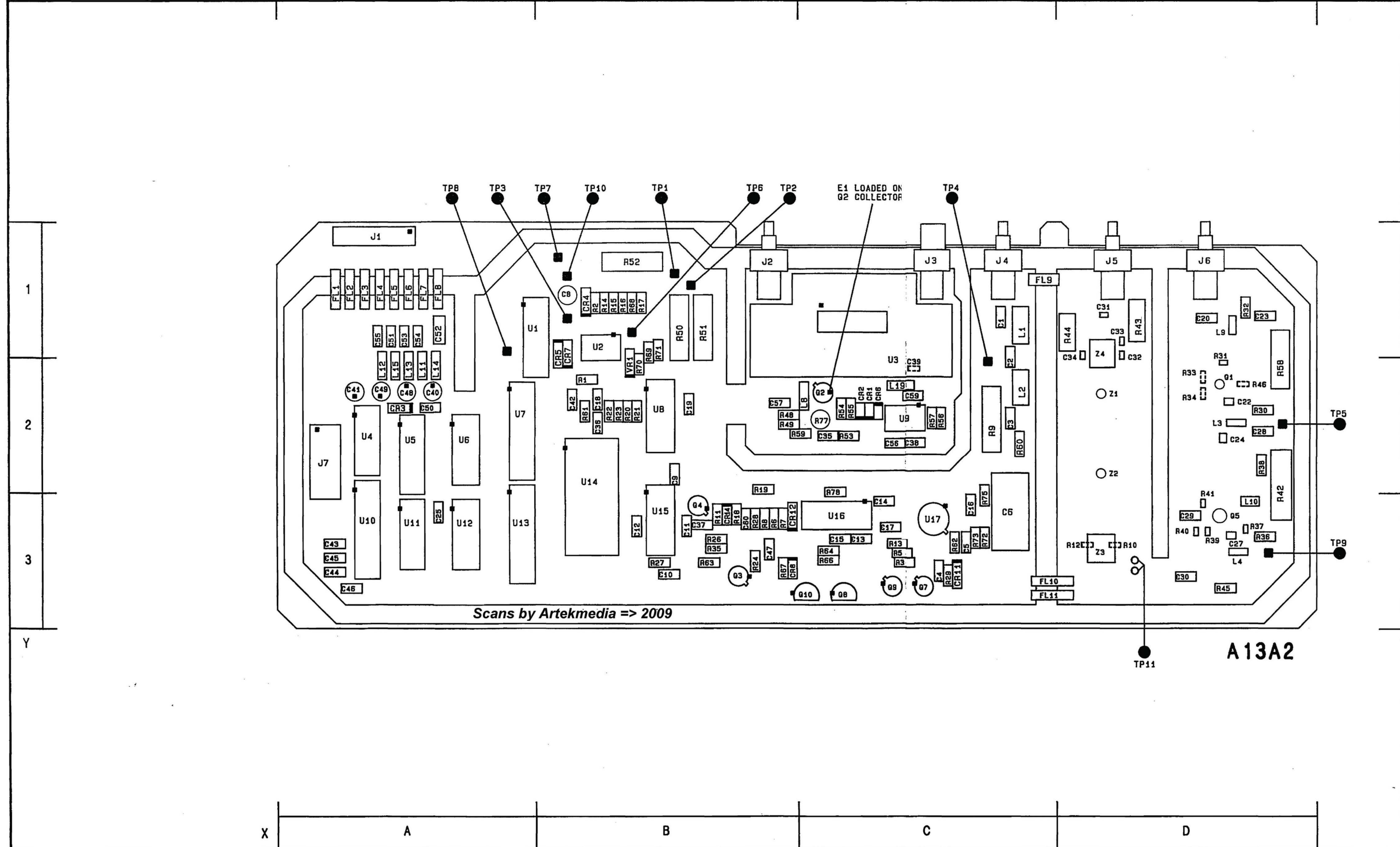


Reference Block Diagram

Component Coordinates

COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y
C1	C, 1	C53	A, 1	L1	C, 1	R20	B, 2	R62	B, 2	C, 3							
C2	C, 1	C54	A, 1	L2	C, 2	R21	B, 2	R63	B, 3	C, 3							
C3	C, 2	C55	A, 1	L3	C, 3	R22	B, 2	R64	B, 3	C, 3							
C4	C, 3	C56	C, 2	L4	D, 3	R23	B, 2	R65	B, 3	C, 3							
C5	C, 3	C57	B, 2	L8	C, 2	R24	B, 3	R67	B, 3	C, 3							
C6	C, 3	C59	C, 2	L9	D, 1	R28	B, 3	R68	B, 1	C, 3							
C11	B, 3	C60	B, 3	L10	D, 3	R29	C, 3	R70	B, 2	C, 3							
C12	B, 3			L11	A, 2	R30	D, 2	R71	B, 1	C, 3							
C13	C, 3	CR1	C, 2	L12	A, 2	R31	D, 2	R72	C, 3	C, 3							
C14	C, 3	CR2	C, 2	L13	A, 2	R32	D, 1	R73	C, 3	C, 3							
C15	C, 3	CR3	C, 2	L14	A, 2	R33	D, 2	R74	C, 3	C, 3							
C16	C, 3	CR6	C, 2	L15	A, 2	R34	D, 2	R77	C, 2	C, 3							
C17	C, 3	CR8	B, 3	L19	C, 2	R36	D, 3	R78	C, 2	C, 3							
C20	D, 1	CR11	C, 3			R37	D, 3										
C22	D, 2	CR12	B, 3	Q1	D, 2	R38	D, 2	TP1	B, 1								
C23	D, 1	CR14	B, 3	Q2	D, 2	R39	D, 3	TP2	B, 1								
C24	D, 2			Q3	B, 3	R40	D, 3	TP4	B, 1								
C27	D, 3	E1	C, 2	Q4	B, 3	R41	D, 3	TP5	D, 2								
C28	D, 2			Q5	D, 3	R42	D, 2	TP8	A, 1								
C29	D, 3	FL4	A, 1	Q7	C, 3	R43	D, 1	TP9	D, 3								
C30	D, 3	FL5	A, 1	Q8	D, 1	R44	D, 1	TP10	B, 1								
C31	D, 1	FL6	A, 1	Q9	C, 3	R45	D, 3	TP11	D, 3								
C32	D, 1	FL7	A, 1	Q10	C, 3	R46	D, 2										
C33	D, 1	FL8	A, 1			R48	B, 2	U3	C, 1								
C34	D, 1	FL9	C, 1	R1	B, 2	R49	B, 2	U8	B, 2								
C35	C, 2	FL10	C, 3	R3	C, 2	R50	B, 1	U9	B, 3								
C36	B, 2	FL11	C, 3	R5	C, 3	R51	B, 1	U15	B, 3								
C38	C, 2			R6	B, 3	R52	B, 1	U16	C, 3								
C39	C, 2	J1	A, 1	R7	B, 3	R53	C, 2	U17	C, 3								
C40	A, 2	J2	B, 1	R8	B, 3	R54	C, 2										
C41	A, 2	J3	C, 1	R9	B, 3	R55	C, 2										
C47	B, 3	J4	C, 1	R10	D, 3	R56	C, 2	VR1	B, 2								
C48	A, 2	J5	D, 1	R11	B, 3	R57	C, 2										
C49	A, 2	J6	D, 1	R12	D, 3	R58	D, 2	Z1	D, 2								
C50	A, 2			R13	C, 3	R59	B, 2	Z2	D, 2								
C51	A, 1			R14	B, 2	R60	B, 2	Z3	D, 3								
C52	A, 1			R19	B, 2	R61	B, 2	Z4	D, 1								

A13A1 LOW-PASS FILTER ASSEMBLY SS42
SEE REVERSE SIDE



Component Locator

Figure 8P-104. SERVICE SHEET 43 INFORMATION

Schematic General Information

CHANGES

All Serial Prefixes

On the schematic:

- R10,R12 - In the **AMPLITUDE MODULATOR**, change the value of R10 and R12 to 147 ohm's.
- R31,R37 - In the **MODULATION RF DRIVER**, change the value of R31 and R37 to 215 ohm's.
- R33,R34,R46 - In the **MODULATION RF DRIVER** change the value of R33, R34, and R46 to 46.4 ohm's.

2511A and above

On the Component Locator:

- R61 - Remove R61.

In Component Coordinates:

- R61 - Remove R61.

On the schematic:

- In the upper right portion of the schematic, change A13A2 part number to 08642-60213.
- Replace appropriate portion of the schematic with the partial on 8P-104.3.
- To the left of **ALC OFF**, change bullet GU from "AMP SWEEP CONTROL" to "ALC OFF SELECT".

2630A and above

On the Component Locator:

- CR6 - Delete CR6 in section C,2.

In the Component Coordinates:

- CR6 - Delete CR6, C,2.

On the schematic:

- CR6 - In the **RF AMPLIFIER AND PEAK DETECTOR** under **BUFFER AMPLIFIER**, delete CR6.

CHANGES

2642A and above

On the Component Locator:

- CR15 - In section B,2, add CR15 directly below CR19.

In Component Coordinates:

- CR15 - Add CR15, B,2.

On the schematic:

- In the upper right portion of the schematic, change A13A2 part number to 08642-60313.
- Replace appropriate portion of the schematic with the partial on 8P-104.5
- R39,R40,R41 - In the **MODULATION RF DRIVER** change the value of R39, R40 and R41 to 42.2 ohm's.

2709A and above

On the schematic:

- CR6, Q11, R79, R80, R81, - Use the schematic with the new schematic partial on page 8P-104.7.

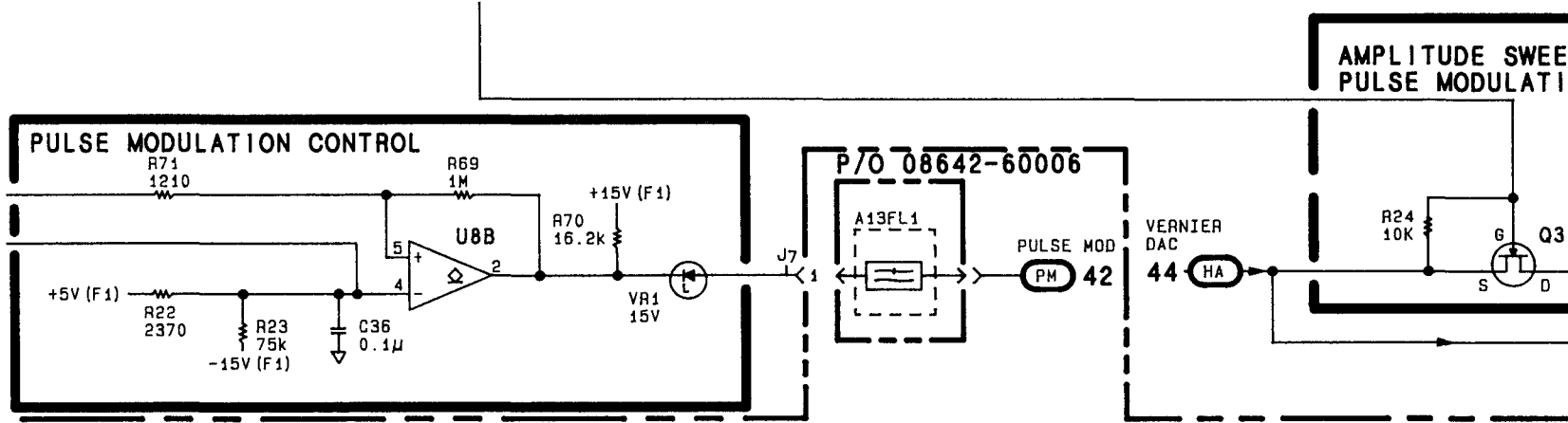
On the Component Locator:

- CR6, Q11, R79, R80, R81, - Use the component locator with the new component locator on page 8P-104.8.

2722A and above

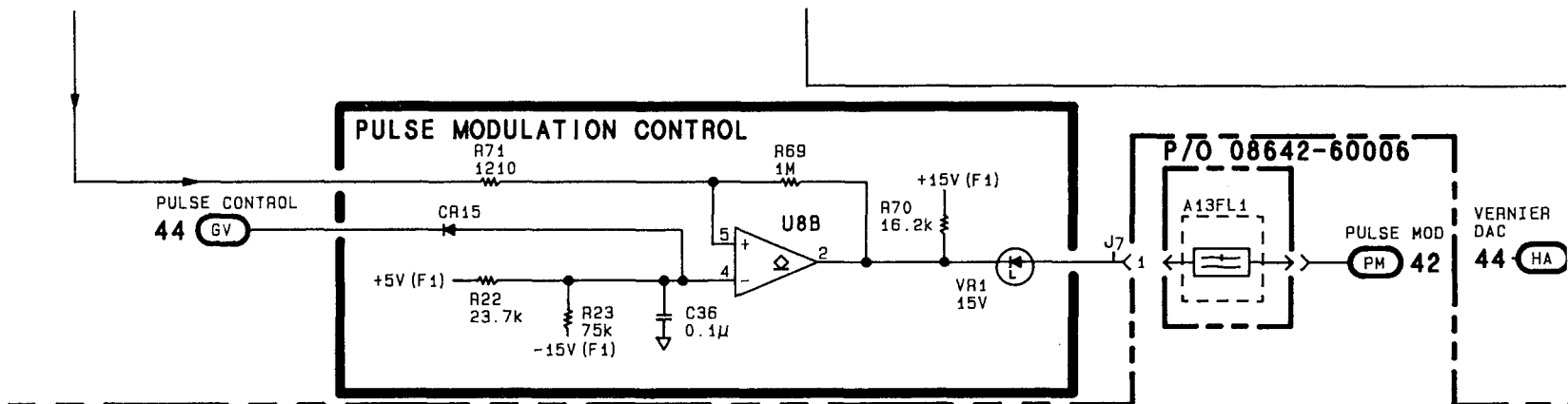
On the schematic:

- R52 - In **RF POWER AMPLIFIER AND PEAK DETECTOR**, change the value of R52 to 107 ohms.



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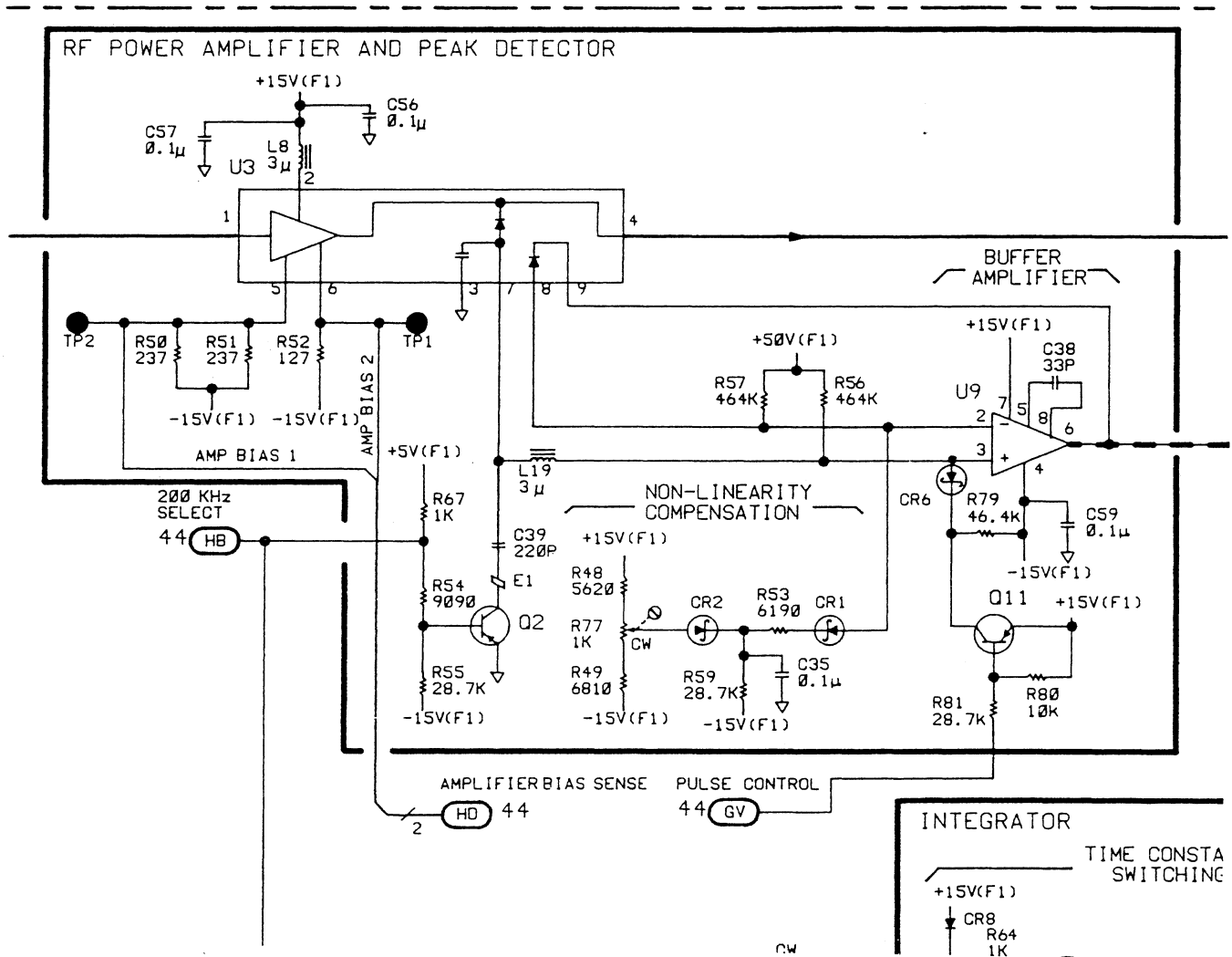


CHANGES TO FIGURE 8P-105 (2642A AND ABOVE)

SS43
8P-104.5

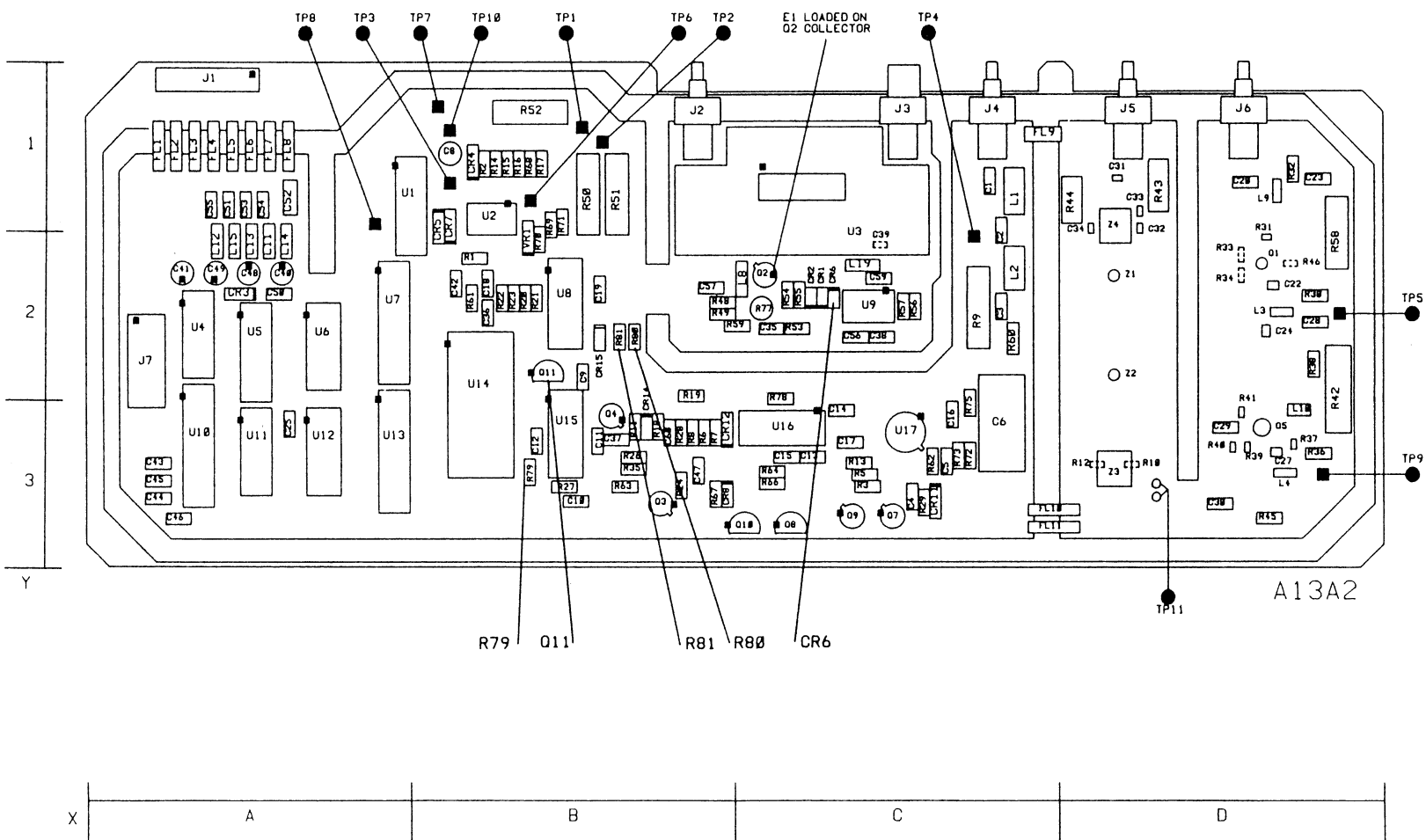
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CHANGES TO FIGURE 8P-105 (2709A AND ABOVE)

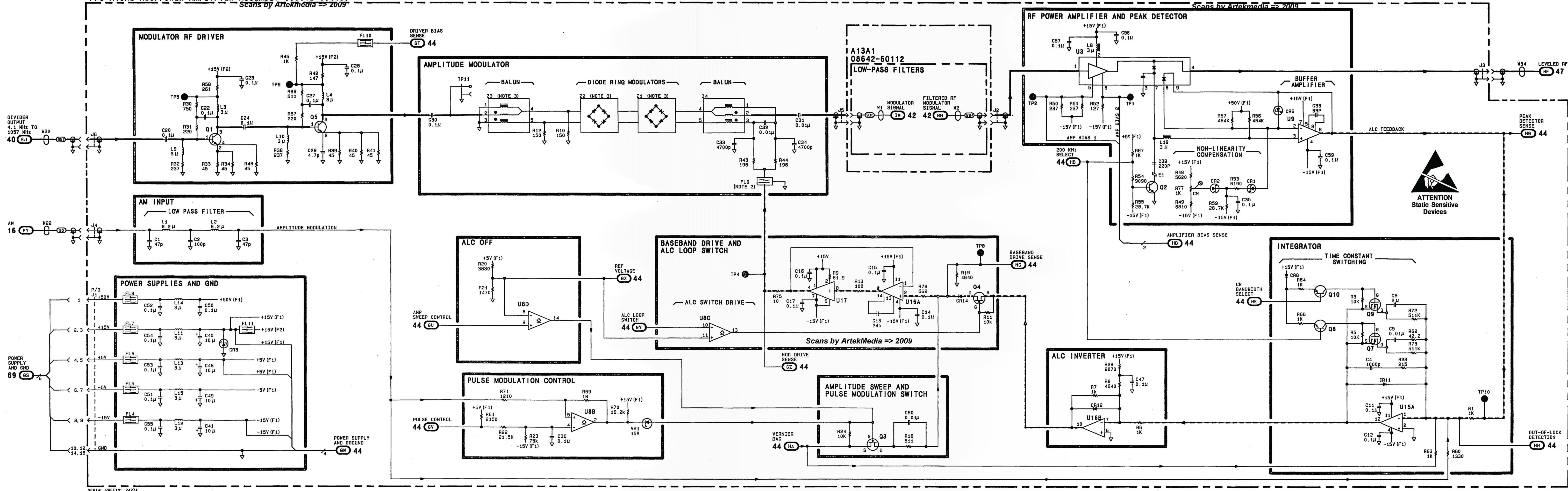
SS43
8P-104.7



SS43

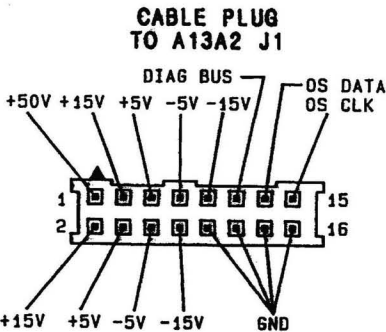
8P-104.8

CHANGES TO FIGURE TO 8P-103 (2709A AND ABOVE)

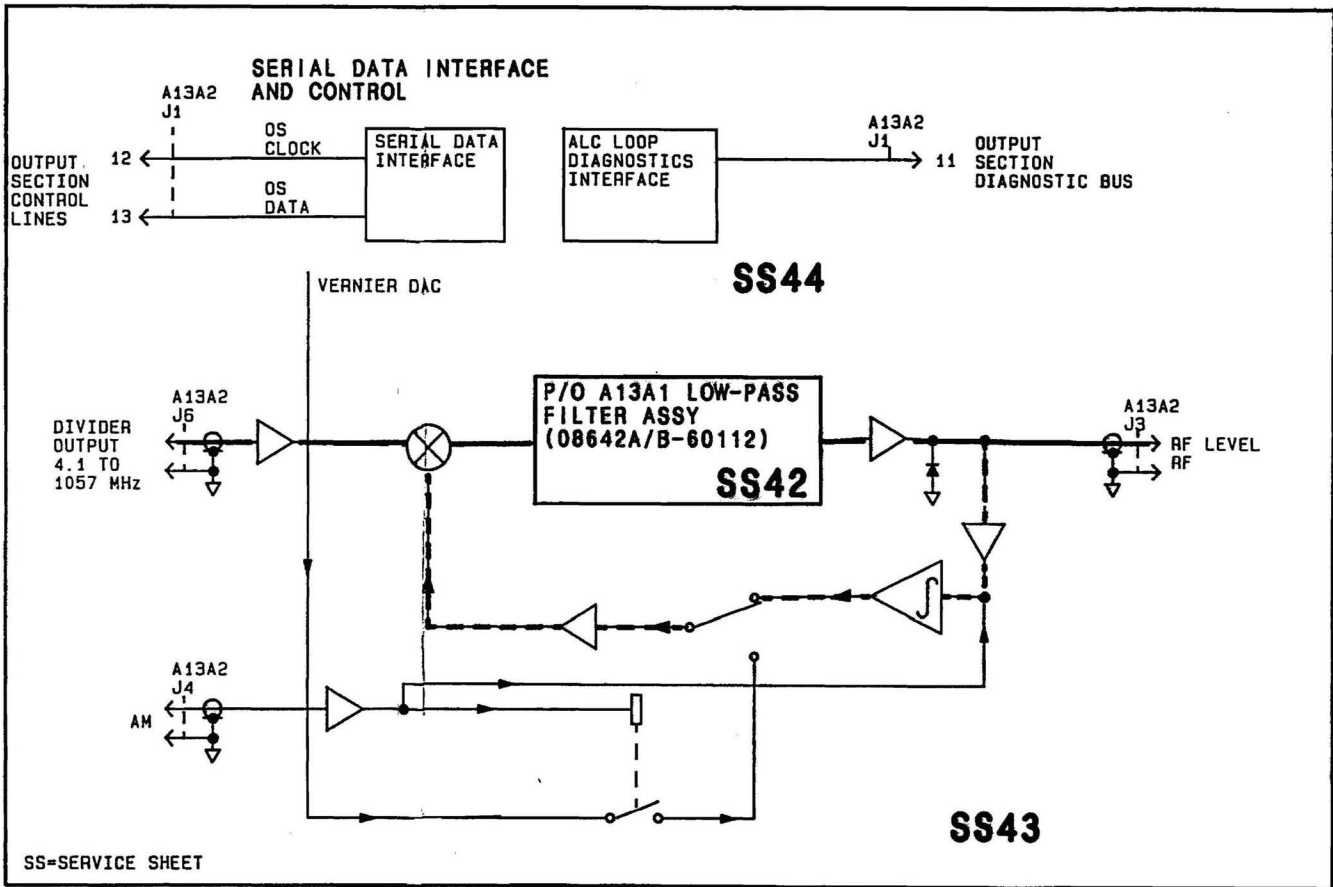


Notes: Scans by Artekmedia => 2009

- 1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- 2. FL1, FL2, FL3 outer bodies must be soldered to pads in notched area of shielding.
- 3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
- 4. A13FL1 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.



Schematic General Information



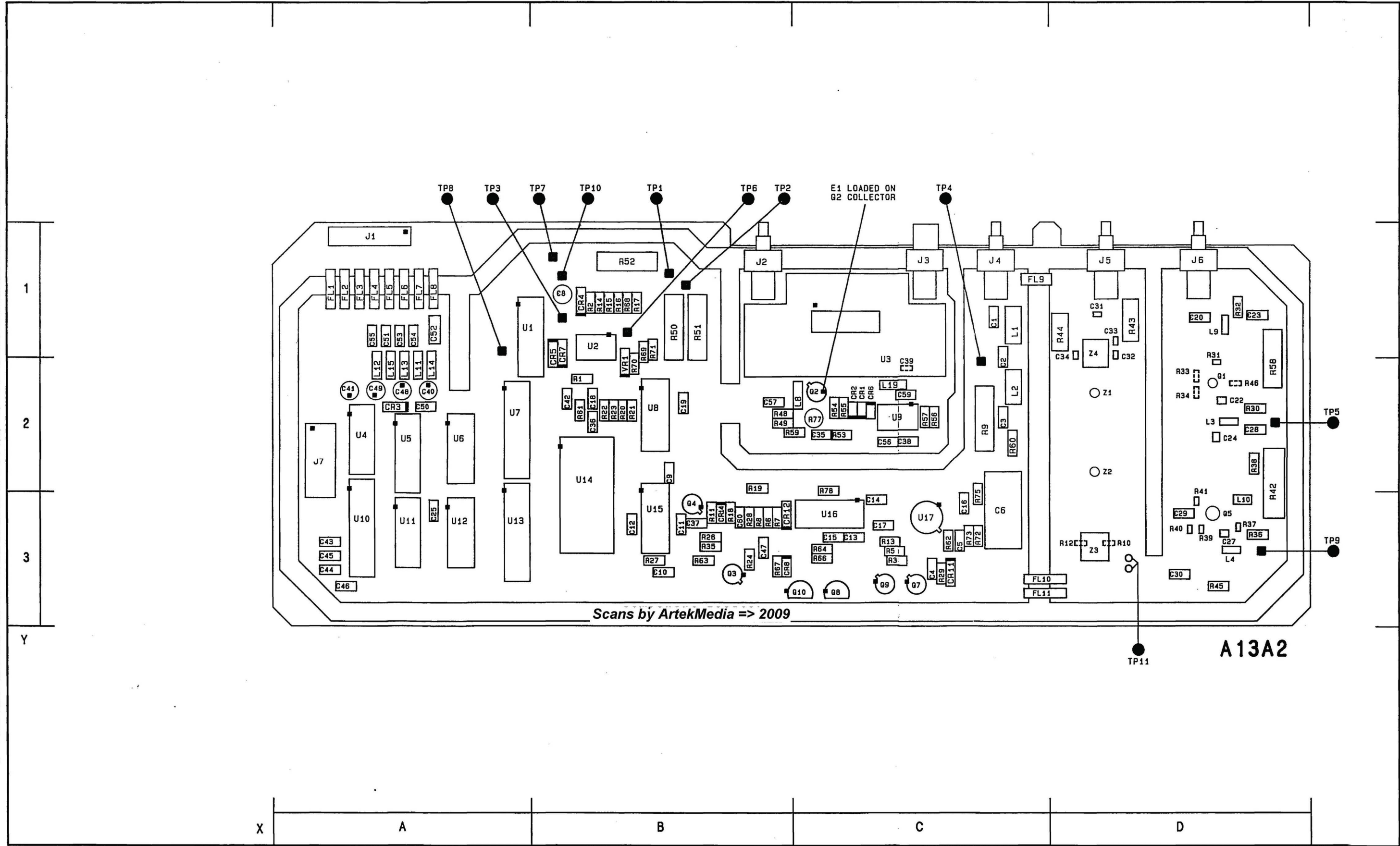
Reference Block Diagram

Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C8	B, 1	U1	A, 1														
C9	B, 2	U2	B, 1														
C10	B, 3	U4	A, 2														
C18	B, 2	U5	A, 2														
C19	B, 2	U6	A, 2														
C25	A, 3	U7	A, 2														
C37	B, 3	U8	B, 2														
C42	B, 2	U10	A, 3														
C43	A, 3	U11	A, 3														
C44	A, 3	U12	A, 3														
C45	A, 3	U13	A, 3														
C46	A, 3	U14	B, 2														
		U15	B, 3														
CR4	B, 1																
CR5	B, 1																
CR7	B, 1																
FL1	A, 1																
FL2	A, 1																
FL3	A, 1																
J1	A, 1																
J7	A, 2																
R2	B, 1																
R14	B, 1																
R15	B, 1																
R16	B, 1																
R17	B, 1																
R26	B, 3																
R27	B, 3																
R35	B, 3																
R68	B, 1																
TP3	B, 1																
TP6	B, 1																
TP7	B, 1																

P/O A13A2 ALC/POWER AMPLIFIER ASSEMBLY SS43

SEE REVERSE SIDE



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A13A2

Figure 8P-106. SERVICE SHEET 44 INFORMATION

Component Locator

CHANGES

All Serial Prefixes

On the schematic:

- To the left of **OUT-OF-LOCK WINDOW COMPARATOR**, add "43" next to the bullet "HH" and delete "A13A2".
- J7 - On the right side of the schematic, under P/O J7, change the following pin numbers:
 - 3 to 8
 - 4 to 6
 - 1 to 7
 - 8 to 5
 - 6 to 3
 - 7 to 4
 - 5 to 1

2511A and above

On the schematic:

- In the upper left portion of the schematic, change A13A2 part number to 08642-60213.
- Replace the appropriate portion of the schematic with the partial on 8P-106.3.
- J7, A13FL1 - On the right side of the schematic, delete the line labeled GND, J7 pin 1, and the feed through filter connected to J7 pin 1. Be sure J7 pin numbering changes were made first! (See All Serial Prefixes).
- To the right of **SERIAL DATA INTERFACE**, change bullet GU from "AMP SWEEP CONTROL" to "ALC OFF SELECT".

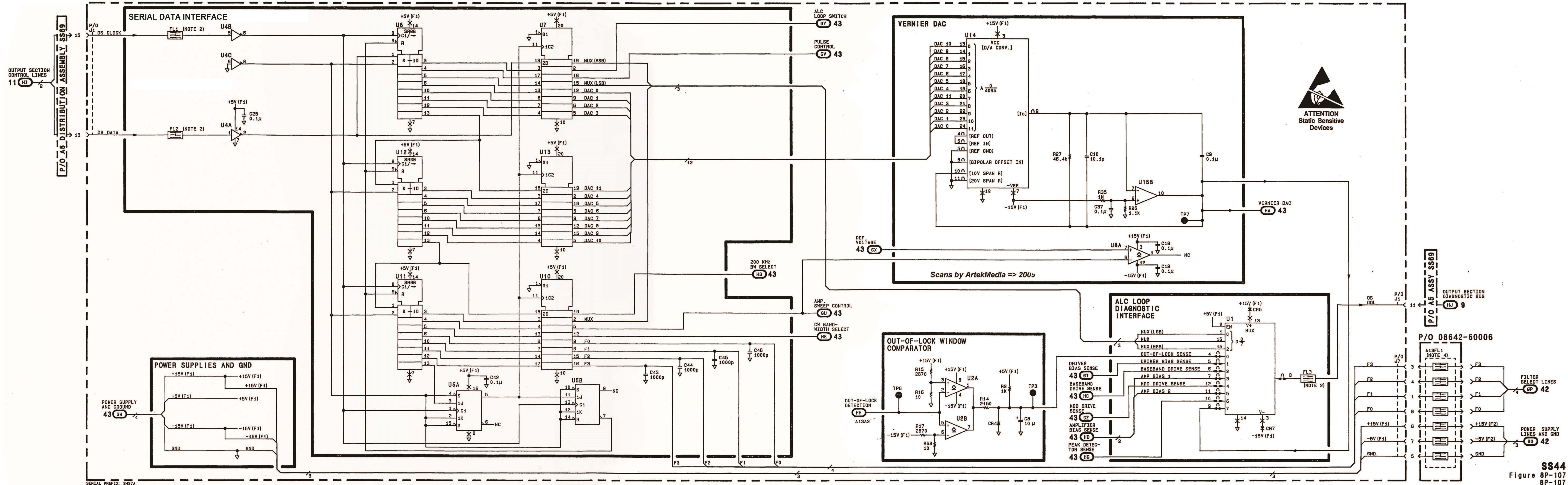
2709A and above

On the Component Locator:

- Use the new component locator on page 8P-106.4.

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A14 Module

Troubleshooting and Adjustments Contents

Troubleshooting

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Oscillator Assembly Specifications Table	8Q-34
Heterodyne Assembly Specifications Table	8Q-34

Troubleshooting

A14 TROUBLESHOOTING INFORMATION

Before Proceeding With Module Troubleshooting

- You should have confidence that A14 is the faulty module based on the results of Module Level Diagnostics (MLD).
- Open the manual to the foldout on page 8Q-100. There are 3 diagrams of the A14 module. One of the diagrams is titled Simplified Block Diagram. It is intended to be used to understand the operation of A14. (There is a brief discussion of the circuit operation on page 8Q-3).
- Open the next foldout on page 8Q-101 (BD15). There, you will see a more detailed Block Diagram of the A14 Heterodyne Module. **This Block Diagram is meant to be used during Checks 1, 2 and 3.** Notice there are two assemblies shown, A14A2 and A14A3. These assemblies are shown on three Service Sheets, SS45, SS46 and SS47.
- The objective of Troubleshooting Checks is to isolate the malfunction to an area of circuitry represented on one Service Sheet. The Checks are intended to be done in the order they are numbered.
- Once the malfunction is isolated, refer to the Component Level Repair Directory. There, you will find information useful for locating faulty components.
- Specification failures (for example, phase noise, spurs, etc.) might not be found by Troubleshooting Checks. Manual Adjustment Procedures can be done, and the HP 8642 then re-tested to see if the specific failure condition still exists. At this point, if repair is necessary, Module Performance Checks may be helpful to pinpoint a failure condition in the module.

Overall Equipment List

Signal Generator No. 2	HP 8642A/B
Oscilloscope	HP 1980B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
Measuring Receiver	HP 8902A
HP 8642 Bench Service Kit	HP 11802A
Sensor Module	HP 11722A

Essentials of A14 Module Operation

Refer to the Simplified Block Diagram opposite the foldout on BD15. The A14 Heterodyne Module down converts the A13 output module's output into two low frequency bands for heterodyne operation or switches it directly to the A16 Attenuator Module (HP 8642A) or A19 Attenuator/Doubler Module (HP 8642B).

The two heterodyne bands are: Band 1 0.10–4.13 MHz, and HET 0.10–132.18 MHz. Band 1 is used normally by the HP 8642 for 0.10 to 4.13 MHz frequencies. HET Band is only used when requested by the user by entering **[SHIFT] [SPCL] [8]** or when fm deviation amounts greater than allowed by the dividers for frequencies between 4.13 and 132.18 MHz is requested. (HP 8642 then selects **[SHIFT] [SPCL] [8]** automatically.)

The two heterodyne bands are derived by mixing the A13 module's output with one of two fixed frequencies. For Band 1 the fixed frequency is the 45 MHz timebase signal from the A6 Module for HET Band it is an 832.5 MHz signal which is phase locked to the 45 MHz timebase signal. The difference frequency in both cases is lowpass filtered, amplified, and routed to the A16 (HP 8642A) or A19 (HP 8642B) modules.

The 832.5 MHz phase Locked Loop is shown on Service Sheets 45 and 46. The heterodyne circuitry is shown on Service Sheet 47.

See the A14 Module block diagram (BD15, page 8Q-101) for further understanding of the A14 Module's internal operation.

CHECK 1: A14U1 HETERODYNE SWITCH (SS47)**NOTE**

Use the Module Test Point/Adjustment Locations diagram on the fold-out opposite BD15 to locate test points on A14A3. Test point designators (XX) will be used when applicable. Points not located on the Module Test Point/Adjustment Locations diagram can be found using the Component Locator diagrams opposite SS47.

Essentials of A14U1 Operation

A14U1 is a double pull double throw coaxial switch. A14U1 either bypasses the A14 module and transfers the output from the A13 module to the attenuator or switches the output from the A13 module into the A14 module for down conversion and transfers the down converted signal to the attenuator.

Description of Check 1

Check 1 verifies proper A14U1 operation by verifying the switch drive voltages and RF frequency transfer.

Required Equipment:

Signal Generator No. 2	HP 8642A/B
Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
DVM	HP 3456A

Test A14U1**1. Setup:**

Set the HP 8642 POWER switch to STBY.

Remove the two top rear feet from the HP 8642 and remove the instrument top cover (center captive screw).

Extend the A14 module on extender posts (Refer to DISASSEMBLY PROCEDURES in the Service Manual or MECHANICAL PROCEDURES in the On Site Service Manual).

Remove the A14A2 cover.

Set Signal Generator No. 2 to 862.5 MHz, 0 dBm output.

Connect a 1 meter coaxial cable to the RF output on Signal Generator No. 2.

Connect the Sensor Module to the end of the 1 meter cable connected to Signal Generator No. 2. Ensure that the Sensor Module is connected to the Measuring Receiver and that the Measuring Receiver power meter is zeroed and calibrated.

Set the HP 8642 POWER switch to ON.

2. Test A14U1 Operation:

Set the Measuring Receiver to measure RF Power. When the reading is displayed set the Measuring Receiver for a ratio reading (press the Ratio key) and logarithmic units. The Measuring should now be displaying 0.00 dB.

Disconnect the Sensor Module from the 1 meter cable.

Connect the Sensor Module to A14U1 J3.

Connect Signal Generator No. 2 to A14U1 J2 through the 1 meter cable.

On the HP 8642 press **INST PRESET**.

The Measuring Receiver should display between 0.00 dB and -1.22 dB.

Connect the DVM to A14A3 J5 pin 1 and then pin 2. Both J5 pins should measure approximately 20.0 Vdc. (See SS45 Component locator for A14A3 J5 location.)

On the HP 8642 key in **SHIFT** **SPCL** **8**.

Connect the DVM to A14A3 J5 pin 1 and then pin 2. Both J5 pins should measure approximately 0.0 Vdc.

Connect the Sensor Module to A14U1 J1.

The Measuring Receiver should display between -10.00 dB and -10.45 dB.

Connect Signal Generator No. 2 to A14U1 J4 through the 1 meter cable.

Connect the Sensor Module to A14U1 J3.

The Measuring Receiver should display between 0.00 dB and -1.22 dB.

CHECK 2: A14 PHASE DETECTOR/INTEGRATOR CIRCUITRY (SS45)

NOTE

*Use the Module Test Point/Adjustment Locations diagram on the fold-out opposite BD15 to locate test points on A14A2. Test point designators (**XX**) will be used when applicable. Points not located on the Module Test Point/Adjustment Locations diagram can be found using the Component Locator diagrams opposite SS45.*

Essentials of SS45 Circuit Operation

Service Sheet 45 shows the **45 MHz INPUT AND DIVIDE BY 2, PHASE DETECTOR, 45 MHz CONTROL, INTEGRATOR, HET DIAGNOSTICS, POWER SUPPLY** and **GND** circuitry.

The **45 MHz INPUT AND DIVIDE BY 2** circuitry, translates the 45 MHz timebase signal to a TTL signal and then divides it by two resulting in a 22.5 MHz TTL signal.

The **PHASE DETECTOR** circuitry produces a 22.5 MHz comb signal in the **PULSE TRAIN GENERATOR**, which is used to drive the **SAMPLING MIXER**. The other input to the **SAMPLING MIXER** is the output from the 832.5 MHz SAWR Oscillator from SS46. The output from the **SAMPLING MIXER** is an error signal generated by the difference in phase between the **SAWR** Oscillator and the 22.5 MHz harmonic of the same frequency.

The **INTEGRATOR** circuitry integrates the error signal and outputs a voltage of the same sign and proportional to the phase difference between the **SAWR** oscillator and the 22.5 MHz harmonic. The **INTEGRATOR** has two bandwidths, 700 Hz when the loop is locked and approximately 10 KHz when the loop is unlocked.

The **HET DIAGNOSTICS** sense two points for an out of lock condition;

1. If there is a difference in phase between the two phase detector inputs, a beat note will be at U3 Pin 6.
2. If the SAWR PLL FEEDBACK signal (output from the **SAWR FEEDBACK AMPLIFIERS**, SS46) is not present, this condition will be sensed by peak detector CR8, C17 and U6A.

If one of these conditions exists, U7 (one shot multivibrator) will hold the out of lock line low through U8 for 10 ms. The out of lock line also changes the bandwidth of the **INTEGRATOR** by switching analog switch U5 on to bypass R19 in the **INTEGRATOR** feedback. The out of lock line will stay low until the out of lock condition is resolved.

The **POWER SUPPLY** and **GND** circuitry filters and de-couples the power supplies for the A14 **HETERODYNE ASSEMBLY**.

Description of Check 2

The first test of Check 2 verifies that the power supply voltages on the A14A2 circuit board are correct.

Then, the operation of the Phase Detector, Integrator, and related circuitry is tested using signal substitution to simulate a difference in frequencies being sampled at the phase detector.

The next test is the HET Diagnostics. This test also uses signal substitution to simulate out of lock conditions. An Oscilloscope is used to observe the integrator and diagnostic lines during out of lock conditions.

The last test is for the **45 MHz CONTROL** circuitry. This test verifies that the 45 MHz signal can be switched off and on.

Required Equipment:

Signal Generator No. 2	HP 8642A/B
Oscilloscope	HP 1980B
Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
DVM	HP 3456A

Test the Power Supplies

3. Setup:

Extend the A14 module on extender posts (Refer to DISASSEMBLY PROCEDURES in the Service Manual or MECHANICAL PROCEDURES in the On Site Service Manual).

Remove the A14A2 cover.

CAUTION

To remove the A14A2 cover, first remove the A14A2 Q13 heatsink. This is a round threaded heatsink which screws onto the A14A2 Q13 heatsink stud. It is located just below A14A2 J4. Then remove the screws securing the A13A2 cover. After removing the cover, screw the Q13 heatsink back on to Q13.

4. Measure Voltage Levels:

Check power supply lines at the points given in Table 8Q-1 with the DVM. (Locations can be found on the A14A2 Component Locator opposite SS45).

Table 8Q-1. A14 Power Supply Lines

Component	Nominal Voltage
FL7	≈ +15V
FL6	≈ +5V
FL5	≈ -15V

Test the Phase Detector, Integrator, and Related Circuitry

5. Setup:

Ensure that the Sensor Module is connected to the Measuring Receiver and that the Measuring Receivers power meter is zeroed and calibrated.

Switch the HP 8642 to STANDBY.

Set Signal Generator No. 2 to 45 MHz and 8.0 dBm output.

Lock the timebases of Signal Generator No. 2 and HP 8642 together.

Connect Signal Generator No. 2 to A14A2 J1 (HN) .

Remove W1 from between A14A2 TP3 pins A and B then connect it between pins B and C.

Connect the Oscilloscope to A14A2 TP3 pin A (SAWR TUNE VOLTAGE).

Remove cable A14 W1 from A14A2 J4.

Connect the Sensor Module to A14A2 J4 through a short piece of coaxial cable.

Switch the HP 8642 to ON.

6. Verify Integrator Waveforms (Phase Detector and Integrator Outputs):

On the HP 8642 key in **[SHIFT] [SPCL] [8], [10] [MHz]**, (sets the HP 8642 to prefer Het Mode and turns on the 832.5 MHz SAWR Oscillator (SS46)).

NOTE

If the Measuring Receiver does not measure a signal of approximately 832.5 MHz and an amplitude of approximately +17 to +21 dBm then there is a failure on SS46 go to Check 3.

Set the Measuring Receiver to measure frequency. Record the frequency reading here f1 _____ MHz (record all digits of Measuring Receiver display).

Set Signal Generator No. 2 to $(f1/18.5) + 0.005405$ MHz.

Adjust the Oscilloscope (DC coupled) so that the display appears similar to Figure 8Q-1. This sweep-to-lock signal should be between +15 and +22 Volts peak to peak with a 5 mS to 10 mS time period.

Adjust the Oscilloscope (DC coupled) so that the display appears similar to Figure 8Q-2. This is a 100 kHz beat note signal superimposed on the sweep-to-lock signal. The beat note amplitude should be approximately +.5 to +2 Volts peak to peak.

Set Signal Generator No. 2 to $(f1/18.5) + 0.135135$ MHz.

Adjust the scope so that the display is similar to Figure 8Q-3. The signal should be between +15Vpp and 21 Vpp Volts peak to peak with approximately a 15 mS time period.

Move the Oscilloscope probe to A14A2 FL2.

On the HP 8642 key in **[SHIFT] [SPCL] [3] [249] [Hz]** (This connects A14A2 U8 pin 7 to pin 8).

The signal should be similar to Figure 8Q-3.

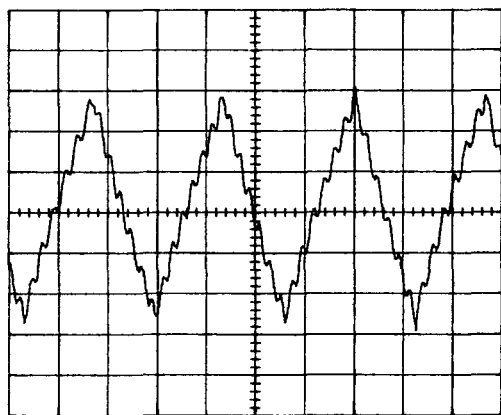


Figure 8Q-1. 3.0V/DIV 3.0 ms/DIV

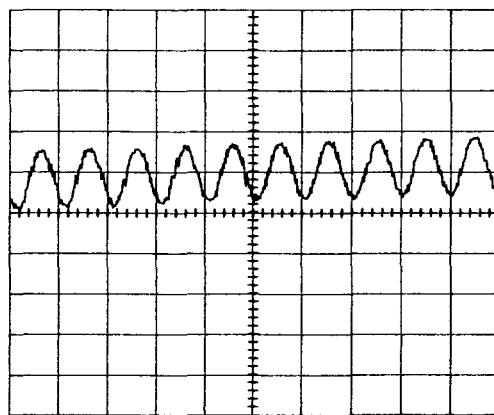


Figure 8Q-2. 1.0V/DIV mS/DIV

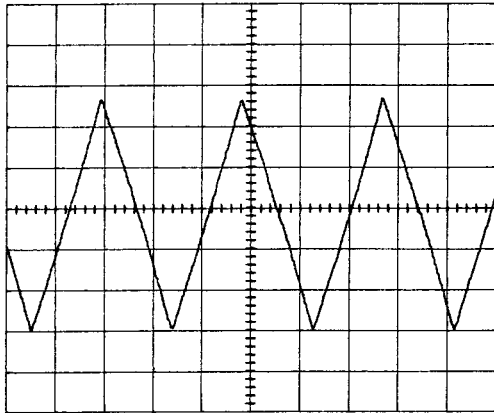


Figure 8Q-3. 3.0/DIV 3.0 mS/DIV

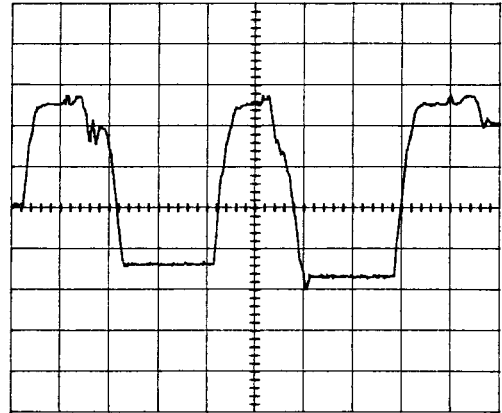


Figure 8Q-4. 9.0V/DIV 6 mS/DIV

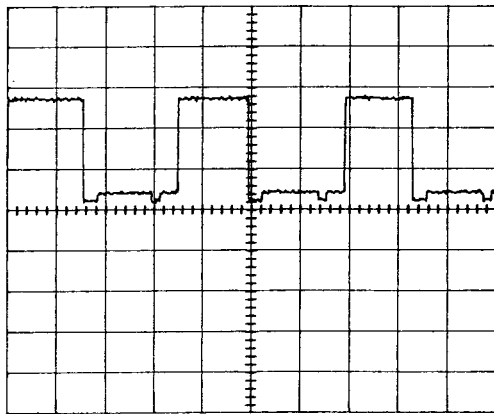


Figure 8Q-5. 2.0/DIV 6 mS/DIV

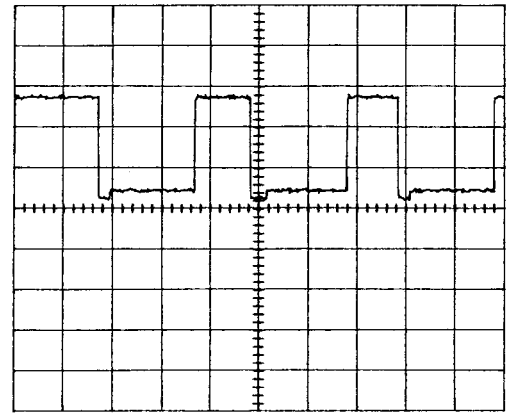


Figure 8Q-6. 2.0V/DIV 6 mS/DIV

Test Out-Of-Lock Detector Circuitry**7. Setup:**

Connect the Oscilloscope to A14A2 TP2.

Set the Oscilloscope for DC coupling, 9V/DIV, 6 mS/DIV.

Set Signal Generator No. 2 to f1/18.5 MHz.

On the HP 8642 key in **[SHIFT] [SPCL] [8], [10] [MHz]**, (sets the HP 8642 to prefer Het Mode and turns on the 832.5 MHz SAWR Oscillator (SS46)).

8. Verify Waveforms:

Fine tune Signal Generator No. 2 to obtain a 24 mS period beat note signal similar to Figure 8Q-4 on the Oscilloscope display.

Connect the Oscilloscope to A14A2 TP4.

Adjust the Oscilloscope and fine tune Signal Generator No. 2 if necessary, for a display similar to Figure 8Q-5. Figure 8Q-5 is not exact due to the variances in 832.5 MHz Oscillator free running characteristics. This waveform will not be stable the important characteristic of the waveform at TP4 is that it has TTL transitions from 0V to +5V in a squarewave like manner. This checks the beat note detector circuitry, U6B, U6C, and U6D.

On the HP 8642 key in **[SHIFT] [SPCL] [208]**. This turns off the 832.5 MHz SAWR Oscillator (SS46), causing U6A (peak detector consisting of CR8, C17, R14 and L26) to detect no SAWR PLL FEEDBACK. (The measuring receiver should now be displaying 45 MHz indicating that the 832.5 MHz oscillator is off.)

The Oscilloscope should now display a 0 Vdc measurement.

On the HP 8642 key in **[SHIFT] [SPCL] [8], [SHIFT] [SPCL] [3], [246] [Hz]** (This connects A14A2 U8 pin 4 to pin 8).

Connect the Oscilloscope to A14A2 FL2. Adjust the Oscilloscope for a display similar to Figure 8Q-6. This is the out-of-lock signal from U7 pin 5. (If the waveform is not correct fine tune Signal Generator No. 2 to obtain a signal similar to Figure 8Q-6.) This waveform will not be stable, the important characteristic of the waveform is that it has TTL transitions from 0 Vdc to +5 Vdc in a squarewave like manner.

Test HET Diagnostics Interface Circuitry**9. Setup:**

Ensure that the test setup has not changed from the above steps.

10. Verify Voltages:

Four points can be multiplexed through A14A2 U8 to the instrument voltmeter. They are connected to U8 pins 4, 5, 6, and 7. U8 pins 7 and 4 have already been checked. This check, checks the other two.

On the HP 8642 key in **[SHIFT] [SPCL] [3] [247] [Hz]** (This connects A14A2 U8 pin 5 to pin 8. This is the Impulse Generator Bias sense point).

The Oscilloscope and the HP 8642 display should read +8.0 Vdc \pm 1.0 Vdc.

On the HP 8642 key in **[SHIFT] [SPCL] [3] [248] [Hz]** (This connects A14A2 U8 pin 6 to pin 8. This is the SAWR PLL FEEDBACK peak detector sense point.)

The Oscilloscope and the HP 8642 display should read +3.5 Vdc \pm 0.5 Vdc.

Test 45 MHz Control Circuitry

11. Setup:

Connect the Oscilloscope to the junction at A14A2 R12 and R13.

Ensure that the setup from the above steps has not changed.

12. Verify 45 MHz Control:

The Oscilloscope should be displaying a 0 Vdc signal.

On the HP 8642 key in **INST PRESET**, (switches the 45 MHz signal on).

The Oscilloscope should be displaying a 45 MHz signal between approximately 0.3 Vpp and 1.0 Vpp.

Restore Module

13. Do not perform the following module restoration steps if continuing with **CHECK 3**.
14. Move W1 from TP3 pins B and C to pins A and B.
15. Remove test equipment from the A14 Module.
16. Reconnect A14 cables.
17. Re-install the A14A2 cover.

CAUTION

When re-installing the A14A2 cover, remove the heatsink from Q13. Then screw the cover on. Then screw the Q13 heatsink back on. ONLY TIGHTEN THE Q13 HEATSINK FINGER TIGHT.

CHECK 3: A14A2 SAWR OSCILLATOR CIRCUITRY (SS46)

Essentials of SS46 Circuit Operation

Service Sheet 46 shows the **45 MHz OR 832.5 MHz BAND SELECT, SAWR OSCILLATOR, SAWR BUFFER AMPLIFIER, SAWR OUTPUT AMPLIFIERS, SAWR FEEDBACK AMPLIFIERS, 45 MHz CONTROL, TUNE LINE FILTER, and POWER SUPPLY GND.** circuitry for the A14 HETERODYNE ASSEMBLY.

The **45 MHz OR 832.5 MHz BAND SELECT** circuitry filters the **HET REF BAND SELECT** (HK) line. This line either turns on the **SAWR OSCILLATOR** through **SAWR OSCILLATOR CONTROL** transistor Q3 or switches the **45 MHz SIGNAL** (JV) through the **45 MHz CONTROL PIN DIODE SWITCH** to the **HET REFERENCE POWER AMPLIFIERS**.

The **SAWR OSCILLATOR** (Q4) is a common emitter oscillator with the **SAWR** device (Y1) as the high Q tank for the feedback. The varactors (CR11, CR12) allow the oscillator to be pulled in frequency by +130 ppm and -80 ppm. (ppm = parts per million).

The **SAWR BUFFER AMPLIFIER** and **SAWR OUTPUT AMPLIFIERS** buffer and amplify the SAWR Oscillator output or the 45 MHz signal.

The **SAWR FEEDBACK AMPLIFIERS** provide the **SAWR PLL FEEDBACK** (JU) signal to the sampling phase detector on SS45.

The **45 MHz CONTROL** switches the **45 MHz SIGNAL** (JV) to the **HET REFERENCE POWER AMPLIFIERS** when the HP 8642 is in the normal heterodyne band from 0.1 MHz to 4.13 MHz.

Description of Check 3

This check selects the SAWR Oscillator and the 45 MHz Signal individually and checks for proper output frequency, output level, and SAWR PLL FEEDBACK level. The Measuring Receiver is used to verify levels and frequency, and a DVM is used to verify the input select line states. Then, the pull range of the SAWR Oscillator is tested by varying the SAWR TUNE LINE (HR) while observing the output frequency on a Spectrum Analyzer. If the SAWR oscillator does not have sufficient pull range to pass this test, the SAWR device (Y1) should be checked.

If any test fails during CHECK 3, refer to the Component Level Repair Directory.

Required Equipment:

Oscilloscope	HP 1980B
Signal Generator No. 2	HP 8642A/B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
HP 8642 Bench Service Kit	HP 11802A
RF Probe	1250-1589

Test the 45 MHz OR 832.5 MHz BAND SELECT line input and SAWR Oscillator Output (SS46)

1. Setup:

Ensure that the Sensor Module is connected to the Measuring Receiver and that the Measuring Receiver is zeroed and calibrated.

Switch the HP 8642 to STANDBY.

Remove W1 from between A14A2 TP3 pins A and B then connect it between pins B and C (SS45).

Remove cable A14 W1 from A14A2 J4.

Connect the Sensor Module to A14A2 J4 through a short piece of coaxial cable.

Set Signal Generator No. 2 to 45 MHz and 8.0 dBm output.

Lock the timebases of Signal Generator No. 2, the Measuring Receiver and HP 8642 together.

Connect Signal Generator No. 2 to A14A2 J1 **HN** (SS45)

Switch the HP 8642 to ON.

2. Measure HET REF Band Select **HK** Levels:

Connect the DVM to L7. Set the DVM to measure DC Volts.

On the HP 8642 key in **SHIFT** **SPCL** **8**, **10** **MHz**.

The DVM should measure $-14 \text{ Vdc} \pm 1 \text{ Vdc}$.

On the HP 8642 key in **INST PRESET**.

The DVM should measure $+14 \text{ Vdc} \pm 1 \text{ Vdc}$.

Measure 45 MHz Signal **JV , HET Reference RF Output **HM** , and SAWR PLL Feedback **JU****

3. Setup:

Connect the Oscilloscope to A14A2 L36.

On the HP 8642 key in **INST PRESET**.

4. Measure 45 MHz SIGNAL **JV** from SS45:

The Oscilloscope should display a 45 MHz signal between approximately 0.25 Vpp and 0.6 Vpp.

5. Measure HET Reference RF Output **HM** :

Set the Measuring Receiver to measure frequency.

The Measuring Receiver should measure 45 MHz.

Set the Measuring Receiver to measure RF Power.

The Measuring Receiver should measure between 17 dBm and 21 dBm.

On the HP 8642 key in **SHIFT** **SPCL** **8**, **10** **MHz**.

Set the Measuring Receiver to measure frequency.

The Measuring Receiver should measure $832.5 \text{ MHz} \pm 100 \text{ KHz}$.

Set the Measuring Receiver to measure RF Power.

The Measuring Receiver should measure between 17 dBm and 21 dBm.

6. Measure SAWR PLL Feedback **JU** :

Remove the Sensor Module from A14A2 J4.

Measure the 832.5 MHz signal on the collector of A14A2 Q1 using RF probe HP P/N 1250-1598 connected to the Sensor Module through a piece of coaxial cable. Place the center pin of the RF Probe on Q1's collector and the outside pin (gnd) on the ground plane just above Q1's collector.

Set the Measuring Receiver to measure frequency.

The Measuring Receiver should measure $832.5 \text{ MHz} \pm 100 \text{ KHz}$.

Set the Measuring Receiver to measure RF Power.

The Measuring Receiver should measure $10 \text{ dBm} \pm 2 \text{ dBm}$.

Test the Voltage Controlled SAWR Oscillators Pull Range**7. Setup:**

Switch the HP 8642 to Standby.

Move W1 from TP3 pins B and C to pins A and B.

Re-install the A14A2 cover.

CAUTION

When re-installing the A14A2 cover, remove the heatsink from Q13. Then screw the cover on. Then screw the Q13 heatsink back on. ONLY TIGHTEN THE Q13 HEATSINK FINGER TIGHT. Over tightening the heatsink will cause lead breakage on Q13.

Set Signal Generator No. 2 to sweep up and down between the frequencies of 44.9964 MHz and 45.00585 MHz, sweep time 5 seconds.

Set Signal Generator No. 2 to ≈ 8 dBm.

Disconnect the sensor module from A14A2 J4.

Connect the Spectrum Analyzer to A14A2 J4 (HM) .

Connect the timebases of the HP 8642, Spectrum Analyzer and Signal Generator No. 2 together.

Switch the HP 8642 on.

Ensure that Signal Generator No. 2 is sweeping (HP 8642 will have SWPNG annunciator lit).

8. Measure Power Levels and Observe Frequency Stability:

On the HP 8642 key in **[SHIFT] [SPCL] [8], [10] [MHz]**, verify that the output displayed on the Spectrum Analyzer is between +17 and +21 dBm, and is a stable 832.5 MHz frequency, sweeping up in frequency to 832.608225 MHz (+ 130 ppm) and down to 832.433400 MHz (−80 ppm).

Restore Module

9. Remove test equipment from the A14 Module.

10. Reconnect A14 cables.

CHECK 4: A14A3 HETERODYNE CIRCUITRY (SS47)

Essentials of SS47 Circuit Operation

Service Sheet 47 shows the **60 MHz LOW-PASS FILTER, MIXER, 216 MHz LOW-PASS FILTER, 1ST HET AMP, 6.8 MHz/216 MHz FILTER, 2ND HET AMP, HET POWER AMP, FILTER SWITCH INTERFACE**, and **A14 U1** circuitry for the A14 **HETERODYNE ASSEMBLY**.

The **60 MHz LOW-PASS FILTER (SWITCHED)** circuitry contains a 16 dB PI attenuator for impedance matching between the A13 module output and the A14 module input. The 60 MHz LOW-PASS FILTER is only used when the HP 8642 is operating in Band 1 (0.1 to 4.13 MHz). The normal frequencies applied to the 60 MHz LOW-PASS FILTER are 45.1 MHz to 49.13 MHz. When the HP 8642 is operating in preferred HET mode (**SHIFT** **SPCL** **8**) the input signal bypasses the 60 MHz LOW-PASS FILTER through A14A3 CR9, R52 and CR11. The normal frequencies for preferred HET band are 832.6 MHz to 964.68 MHz.

The **MIXER** mixes the HET REFERENCE RF OUTPUT (**HM**) with the input from the **60 MHz LOW-PASS FILTER (S)**. When the HP 8642 is in Band 1 the HET REFERENCE RF OUTPUT is 45 MHz at approximately +18 dBm, and in preferred HET band 832.5 MHz at approximately +18 dBm.

The **216 MHz LOW-PASS FILTER (DIPLEXED)** low pass filters the output from the **MIXER** and presents a constant 50Ω load to the **MIXER** output through the diplexer made by A14A3 C61 and R46.

The **1ST HET AMP** amplifies the HET IF with a gain of approximately 10 dB.

The **6.8 MHz/216 MHz LOW-PASS FILTER** further low pass filters the HET IF. The 6.8 MHz low pass filter is selected when the HP 8642 is in Band 1. The 216 MHz low pass filter is selected when in preferred HET band.

The **2ND HET AMP** further amplifies the HET IF with a gain of approximately +12 dB.

The **HET POWER AMP** provides the final A14 Heterodyne Module output to the A16 Attenuator Module (HP 8642A only) or A19 Attenuator/Doubler Module (HP 8642B only). The **HET POWER AMP** has a gain of approximately +13 dB.

The **FILTER SWITCH INTERFACE** translates the TTL BAND SELECT (**JW**) signal from a TTL level signal to a +/− 15 Vdc signal for driving the pin diode switches on SS47 for filter switching. It also provides the HET REF BAND SELECT (**HK**) to SS46 for selecting either the 832.5 MHz SAWR Oscillator or the 45 MHz timebase signals which are amplified and supply the HET REFERENCE RF OUTPUT (**HM**) for the LO drive signal to the **MIXER**.

Description of Check 4

Check 4 first tests the **FILTER SWITCH INTERFACE** using the DVM. Then the **60 MHz LOW-PASS FILTER (SWITCHED), MIXER, 216 MHz LOW-PASS FILTER (DIPLEXED)** and **1ST HET AMP** are checked using Signal Generator No. 2 as a sweep source and the Spectrum Analyzer to measure the circuit response. Finally the **6.8 MHz/216 MHz LOW-PASS FILTER, 2ND HET AMP, AND HET POWER AMP** are checked using Signal Generator No. 2 and the Spectrum Analyzer.

If any test fails during CHECK 4, refer to the Component Level Repair Directory.

Required Equipment:

Signal Generator No. 2	HP 8642A/B
DVM	HP 3456A
Spectrum Analyzer	HP 8566A/B
HP 8642 Bench Service Kit	HP 11802A
RF Probe	1250-1589

NOTE

*Check 4 assumes that Checks 1, 2 and 3 have passed and that the **HET REFERENCE RF OUTPUT** at A14A3 J2 is good.*

Test the Filter Switch Interface

1. Setup:

Set the HP 8642 POWER switch to STBY.

Remove the A14A3 cover.

CAUTION

To remove the A14A3 cover, first remove the A14A3 Q6 heatsink, this is a round threaded heatsink which screws onto the A14A3 Q6 heatsink stud. It is located directly below A14A3 J1. Then remove the screws securing the A14A3 cover. After removing the cover, screw the Q6 heatsink back onto Q6. Q6 will be very hot in this configuration. Do not run the instrument any longer than needed like this.

Set the HP 8642 POWER switch to ON.

2. Measure Voltages:

Key in the HP 8642 front panel key sequences from Table 8Q-2 and verify that the A14A3 U1 voltages are correct at the pin numbers listed.

Table 8Q-2. FILTER SWITCH INTERFACE VOLTAGES

HP 8642 Front Panel Key Sequence	A14A3 U1 Pin Numbers			
	3	4	12	11
INST PRESET SHIFT SPCL 8	+14 Vdc*	-14 Vdc	+14 Vdc	-14 Vdc
INST PRESET 1 MHz	-14 Vdc	+14 Vdc	-14 Vdc	+14 Vdc
* All Voltages are ± 1 Vdc				

Test 60 MHz Low-Pass Filter, Mixer, 216 MHz Low-Pass Filter and 1ST HET AMP

3. Setup:

Remove A14 W34 from A14A3 J3.

Set Signal Generator No. 2 to sweep from 832.6 MHz to 964 MHz, +5 dBm output.

Connect Signal Generator No. 2 to A14A3 J3.

Ensure that A14 W1 is connected between A14A2 J4 and A14A3 J2.

Connect the Spectrum Analyzer to A14A3 TP2 pins B and C using RF Probe HP P/N 1250-1598. Center conductor of probe goes to pin B.

Set the Spectrum Analyzer to view frequencies from 100 kHz to 140 MHz.

Disconnect A14 W3 (914) from A14A3 J1.

Connect a 50 Ω load to A14A3 J1.

4. Test the 60 MHz Low-Pass Filter bypass:

On the HP 8642 key in **SHIFT** **SPCL** **8**, **10** **MHz**

The Spectrum Analyzer should display a sweeping signal between 100 kHz and 132.5 MHz, with a level between -9 dBm and -5 dBm.

Ensure that cable W29 is connected to A14A2 J1.

5. Test the 60 MHz Low-Pass Filter:

Stop the frequency sweep on Signal Generator No. 2.

On the HP 8642 key in **INST PRESET**, **1** **MHz**.

Set Signal Generator No. 2 to the frequencies listed in Table 8Q-3. Verify that the RF levels are correct for each **IF FREQUENCY** using the Spectrum Analyzer.

Table 8Q-3. 60 MHz LOW-PASS FILTER RESPONSE

Signal Generator Frequency	IF Frequency	IF Level		
		Lower Limit	Actual	Upper Limit
20 MHz	25 MHz	-9 dBm	_____	-5 dBm
80 MHz	35 MHz	-12 dBm	_____	-8 dBm
100 MHz	55 MHz	-15 dBm	_____	-12 dBm
150 MHz	105 MHz	-29 dBm	_____	-25 dBm

6. Test the 216 MHz Low-Pass Filter (Diplexed):

On the HP 8642 key in **SHIFT** **SPCL** **8**, **10** **MHz**.

Set Signal Generator No. 2 to 682.5 MHz.

Set the Spectrum Analyzer to view signals between 125 MHz and 400 MHz.

Set Signal Generator No. 2 to the frequencies in Table 8Q-4 and verify the **IF FREQUENCIES** and Levels listed for each Signal Generator No. 1 frequency.

Table 8Q-4. 216 MHz LOW-PASS FILTER (DIPLEXED) RESPONSE

Signal Generator Frequency	IF Frequency	IF Level		
		Lower Limit	Actual	Upper Limit
682.5 MHz	150 MHz	-12 dBm	_____	-5 dBm
607.5 MHz	225 MHz	-15 dBm	_____	-8 dBm
557.5 MHz	275 MHz	-25 dBm	_____	-15 dBm
532.5 MHz	300 MHz	-35 dBm	_____	-25 dBm
482.5 MHz	350 MHz	-45 dBm	_____	-35 dBm

7. Test the 6.8 MHz/216 MHz Low-Pass Filter:

Set Signal Generator No. 2 to 682.5 MHz.

Connect the Spectrum Analyzer to A14A3 TP3 pins A and C using RF Probe HP P/N 1250-1598. Center conductor on probe to pin A.

Set the Spectrum Analyzer to view signals between 125 MHz and 400 MHz.

Set Signal Generator No. 2 to the frequencies in Table 8Q-5 and verify the **IF FREQUENCIES** and Levels listed for each Signal Generator No. 1 frequency.

Table 8Q-5. 216 MHz LOW-PASS FILTER RESPONSE

Signal Generator Frequency	IF Frequency	IF Level		
		Lower Limit	Actual	Upper Limit
682.5 MHz	150 MHz	-12 dBm	_____	-7 dBm
607.5 MHz	225 MHz	-20 dBm	_____	-15 dBm
557.5 MHz	275 MHz	-45 dBm	_____	-35 dBm
532.5 MHz	300 MHz	-60 dBm	_____	-45 dBm
482.5 MHz	350 MHz	-90 dBm	_____	-70 dBm

8. Test the 6.8 MHz Low-Pass Filter:

On the HP 8642 key in **INST PRESET**, **1** **MHz**

Set Signal Generator No. 2 to the frequencies listed in Table 8Q-6. Verify that the **IF FREQUENCIES** and Levels are correct for each Signal Generator frequency using the Spectrum Analyzer.

Table 8Q-6. 6.8 MHz LOW-PASS FILTER RESPONSE

Signal Generator Frequency	IF Frequency	IF Level		
		Lower Limit	Actual	Upper Limit
49 MHz	4 MHz	-12 dBm	_____	-7 dBm
51.8 MHz	6.8 MHz	-15 dBm	_____	-12 dBm
55 MHz	10 MHz	-35 dBm	_____	-22 dBm
60 MHz	15 MHz	-60 dBm	_____	-47 dBm

9. Test the 2ND HET AMP and HET POWER AMP:

Remove the 50 Ω load from A14A3 J1.

Connect the Spectrum Analyzer to A14A3 J1.

Set Signal Generator No. 2 to 45.1 MHz (this generates a 100 kHz output signal).

Set the Spectrum Analyzer to measure the 100 kHz signal.

The Spectrum Analyzer should measure a 100 kHz signal with an amplitude between 14 dBm to 16 dBm.

On the HP 8642 key in **SHIFT** **SPCL** **8**, **10** **MHz**

Set Signal Generator No. 2 to 964.5 MHz (this generates a 132.5 MHz output signal).

Set the Spectrum Analyzer to measure the 132.5 MHz signal.

The Spectrum Analyzer should measure a 132.5 MHz signal with an amplitude between 14 dBm to 16 dBm.

Restore Module

10. Remove test equipment from the A14 Module.
11. Reconnect A14 cables.
12. Re-install the A14A3 cover.

CAUTION

When re-installing the A14A3 cover, remove the heatsink from A14A3 Q6. Then re-install the cover and screw it in place. Then screw the Q6 heatsink in place. ONLY TIGHTEN THE Q13 HEATSINK FINGER TIGHT.

COMPONENT LEVEL REPAIR DIRECTORY

The following tables contain information to aid in component level repairs. These tables are designed to be used after the module troubleshooting procedures have verified a failure in circuitry represented on one of the module service sheet schematics. In general the tables supply one of the following types of information:

- * Special function codes relevant to the module.
- * Transistor emitter, base and collector voltages.
- * Frequency and power levels at different circuit points.
- * Module control line and power supply interconnections in the module and instrument.

NOTE

*Start with the tables that are labeled with a Service Sheet number (Example: **Table 8Q-8 SS45 Power Supply Lines**). Other tables are more general and are to be used at your discretion. It is suggested that you familiarize yourself with the contents of these tables so you can determine if they will be effective in solving your particular troubleshooting need.*

Table 8Q-7	SS45 Power Supply Lines	8Q-21
Table 8Q-8	SS45 Out Of Lock Detector Status	8Q-21
Table 8Q-9	SS45 HET Diagnostics	8Q-21
Table 8Q-10	SS45 Setting Control Lines	8Q-22
Table 8Q-11	SS45 Control Line Interconnections	8Q-22
Table 8Q-12	SS45 Power Supply Lines Interconnections	8Q-22
Table 8Q-13	SS46 Power Supply Lines	8Q-23
Table 8Q-14	SS46 Oscillator Frequency and Pull Range	8Q-23
Table 8Q-15	SS46 DC Voltages	8Q-23
Table 8Q-16	SS46 832.5 MHz Power Levels	8Q-23
Table 8Q-17	SS46 45 MHz Power Levels	8Q-24
Table 8Q-18	SS47 DC Voltages	8Q-24
Table 8Q-19	SS47 RF Power Levels	8Q-24
Table 8Q-20	SS47 Typical Filter Response	8Q-24
Table 8Q-21	SS47 Het Switch Control Line Interconnections	8Q-25
Table 8Q-22	Heterodyne Bands and Frequencies	8Q-25
Table 8Q-23	Special Functions	8Q-25

SERVICE SHEET 45**Table 8Q-7. SS45 Power Supply Lines**

Component	Nominal Voltage
J3 Pin 6	+15 Vdc (F1)
A14A2 L23	+15 Vdc (F2)
J3 Pin 5	+5 Vdc (F1)
A14A2 L27	+5 Vdc (F2)
J3 Pin 4	-15 Vdc (F1)
J3 Pin 7	GND

Table 8Q-8. SS45 Out-Of-Lock Detector Status

Inputs		Output
Voltage @ TP1	Voltage at U6 Pin 9	Voltage @ TP4
-.7 to .7 Vdc <-.7 or >.7 Vdc	<1.4 Vdc	TTL Low (Unlocked) TTL High (Locked) TTL Low (Unlocked)

Table 8Q-9. SS45 HET Diagnostics

Enter Service Mode	Function	Line Label	Explanation
SHIFT	4 6 HZ	HET Out-Of-Lock (U8 Pin 4)	+5 Vdc Locked 0 Vdc Unlocked
SPCL	4 7 HZ	Step Recovery Diode Bias (U8 Pin 5)	
3 2	4 8 HZ	SAWR Detector Diode (U8 Pin 6)	$\leq 1.4V = \text{No SAWR}$
	4 9 HZ	SAWR Tune Line Voltage (U8 Pin 7)	

Table 8Q-10. SS45 Setting Control Lines

Enter Service Mode	Function	Line Label	
SHIFT	6 0 0 Read Line State	9 HZ	HET MUX A
SPCL	6 0 1 Sets Line to 1	1 1 HZ	HET MUX B
3	6 0 2 Sets Line to 0	1 5 HZ	OOL Disable*
	6 1 5 continuous Toggle	2 6 HZ	HET Band+
		1 1 9 HZ	HET OOL**
		7 1 HZ	HET Switch Cont.++
* (1) = Disable (0) = Enable + (1) = Band 1 .1 to 4.13 MHz (0) = HET .1 to 132.18 MHz ** This Line can only be read (1) = Lock (0) = Out of Lock + (1) = Either HET Band (0) = Thru Path *** Refer to Table 8Q-12 Control Line Interconnections for Pin Numbers			

Table 8Q-11. SS45 Control Line Interconnections

Line Label	A14	A5		A4	
	Input Connector/Pin	Output Connector/Pin	Input Connector/Pin	Output Connector/Pin	Latch IC/Pin
HET MUX A	A14A2J2/12	A5J7/14	A5J17/45	A4P1/45	U12/5
HET MUX B	A14A2J2/13	A5J7/15	A5J16/3	A4P2/3	U12/12
OOL DISABLE*					U12/9
HET Band	A14A2J2/15	A5J7/12	A5J15/1	A4P3/1	U19/9
HET OOL	A14A2J2/11	A5J7/16	A5J16/11	A4P2/11	U33/18
* NOTE: OOL Disable is located on A4					

Table 8Q-12. SS45 Power Supply Lines Interconnections

Supply	A17	A5		A14
	Output	Input	Output	Input
+15 Vdc	J2 Pins 9-18	J12 Pins 9-18	J7 Pins 25,24	A14A2J2 Pins 2,3
+5 Vdc	J2 Pins 35-50	J12 Pins 35-50	J7 Pins 22,23	A14A2J2 Pins 4,5
-15 Vdc	J2 Pins 19-22	J12 Pins 19-22	J7 Pins 18,19	A14A2J2 Pins 8,9
GND		Chassis GND	J7 Pins 11,13,17,20,21,26	A14A2J2 Pins 1,6,7,10,14,16

SERVICE SHEET 46**Table 8Q-13. SS46 Power Supply Lines**

Component	Nominal Voltage
A14A2 L5	+15 Vdc
A14A2 L6	+15 Vdc
A14A2 L8	+15 Vdc
A14A2 L11	+15 Vdc
A14A2 L12	+15 Vdc
A14A2 L13	+15 Vdc
A14A2 L14	+15 Vdc
A14A2 L19	+15 Vdc

Table 8Q-14. SS46 Oscillator Frequency and Pull Range

Lower Pull FREQ	Center FREQ	Upper Pull FREQ
832.433 MHz	832.5 MHz	832.608 MHz

Table 8Q-15. SS46 DC Voltages

Transistor	Base Voltage	Collector Voltage
Q1,Q2,Q6 Thru Q10	.6 to .9 Vdc	4 to 6 Vdc
Q12,Q13	.9 to 1.2 Vdc	5.5 to 7.5 Vdc
Q3 HET 1	13.8 to 14.3 Vdc	14.5 to 15 Vdc
HET 2	≈15 Vdc	≈15 Vdc
Q4 HET 1	.6 to .9 Vdc	4 to 6 Vdc
HET 2	≈0 Vdc	≈0 Vdc
Q5 HET 1	≈-.2 Vdc	≈12 Vdc
HET 2	.6 to .9 Vdc	4 to 6 Vdc

Table 8Q-16. SS46 HET 1 832.5 Power Levels *

Stage	Input	Output
SAWR Oscillator		≈ 5 dBm
SAWR Buffer Amplifier	≈ 5 dBm	≈ 5 dBm
SAWR Output Amplifiers		
Q7	≈-10 dBm	≈0 dBm
Q8	≈0 dBm	≈0 dBm
Q9	≈-12 dBm	≈4 dBm
Q10	≈4 dBm	≈4 dBm
Q12	≈4 dBm	≈10 dBm
Q13	≈10 dBm	17 to 20 dBm
SAWR Feedback Amplifiers		
Q2	≈0 dBm	≈4 dBm
Q1	≈4 dBm	≈8 dBm

* NOTE: All Frequencies Are At 832.5 MHz

Table 8Q-17. SS46 45 MHz Power Levels *

Stage	Input	Output
45 MHz Control	≈ -5 dBm	≈ 0 dBm
SAWR Output Amplifiers		
Q12	≈ 0 dBm	≈ 10 dBm
Q13	≈ 10 dBm	18 to 21 dBm
* NOTE: All Frequencies Are At 45 MHz		

SERVICE SHEET 47**Table 8Q-18. SS47 DC Voltages**

Transistor	Base	Collector
Q1,Q3,Q5	13.0 to 13.5 Vdc	13.5 to 14 Vdc
Q2	.7 to 1.2 Vdc	6 to 7 Vdc
Q4	.7 to 1.2 Vdc	6.2 to 7.2 Vdc
Q6	1.2 to 1.7 Vdc	13.2 to 13.7 Vdc

Table 8Q-19. SS47 RF Power Levels

Stage	Input	Output
60 MHz Low-Pass Filter	4.5 to 5.5 dBm	-11.5 to -10.5 dBm
Mixer (RF)	-11.5 to -10.5 dBm	
(LO)	17 to 21 dBm	-19 to -16 dBm
1ST HET Amplifiers	-19 to -16 dBm	-9 to -5 dBm
2ND HET Amplifiers	-11 to -7 dBm	1 to 5 dBm
HET Power Amplifiers	1 to 5 dBm	14 to 16 dBm
* NOTE: Power levels are with an +5 dBm Input signal at A14A3J3 and the Output (A14A3J1) terminated with a 50 Ω load. HP Part 1250-0839		

Table 8Q-20. SS47 Typical Filter Response

Filter	Input Level	FREQ	Response
60 MHz Low-Pass	≈ -10 to 10 dBm	80 MHz	≈ -3 dBc
		100 MHz	≈ -7 dBc
		150 MHz	≈ -20 dBc
216 MHz Low-Pass (Duplexed)	≈ -35 to -16 dBm	225 MHz	≈ -3 dBc
		275 MHz	≈ -10 dBc
		300 MHz	≈ -20 dBc
		350 MHz	≈ -30 dBc
6.8/216 MHz Low-Pass (6.8 MHz)	≈ -25 to -5 dBm	6.8 MHz	≈ -3 dBc
		10 MHz	≈ -15 dBc
		15 MHz	≈ -40 dBc
(216 MHz)	≈ -25 to -5 dBm	216 MHz	≈ -3 dBc
		250 MHz	≈ -15 dBc
		300 MHz	≈ -40 dBc

Table 8Q-21. SS47 Het Switch Control Line Interconnections

HET Switch Control	A14	A5		A17	
	Input Connector/Pin	Output Connector/Pin	Input Connector/Pin	Output Connector/Pin	Input Connector/Pin
	A14A3J6/1-6	A5J7/1-6	A5J13/5-7,10-12	A17J3/5-7,10-12	A17J3/4

HET Switch Control (Cont.)	A5		A4	
	Output Connector/Pin	Input Connector/Pin	Output Connector/Pin	IC/Pin
	A5J13/4	A5J16/23	A4P2/23	19/19

Table 8Q-22. Heterodyne Bands and Frequencies

Band	HET REF Band Select	Frequency Range	HET OSC FREQ	A13 Frequency	Selected Filter
Band 1 HET Band	+15 Vdc -15 Vdc	.1 to 4.1309 MHz .1 to 132.1874 MHz	45 MHz 832.5 MHz	45.1 to 49.1 MHz 832.6 to 964.6875 MHz	6.8 MHz 216 MHz

Table 8Q-23. Special Functions

Select Function	Description
SHIFT SPCL 8	HET Band On (<132.187501)
SHIFT SPCL 2 0 8	Re-enables Divide Bands (<132.187501)
SHIFT SPCL 3 7 0 8 HZ	Turns Off Heterodyne Cal Data
SHIFT SPCL 3 7 1 8 HZ	Turns On Heterodyne Cal Data
SHIFT SPCL 3 6 2 0 4 HZ	Displays A13 Output Modules Frequency

Adjustments

DESCRIPTION OF A14 ADJUSTMENTS

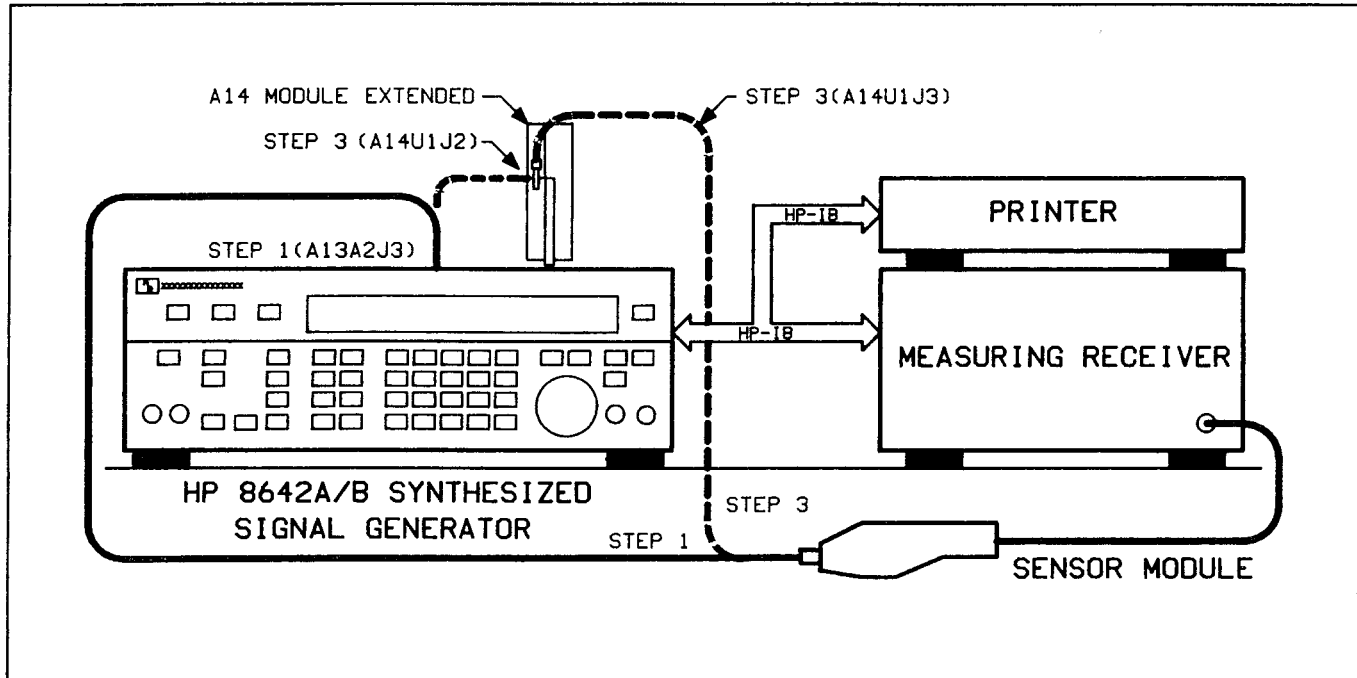
The A14 manual adjustment procedure adjusts the insertion loss through the 216 MHz Low Pass Filter for an overall A14 Module conversion loss of ± 1 dB in heterodyne mode. Conversion loss must be kept within ± 1 dB before the Auto-Adjustment routine can be performed. There are two manual adjustment procedures; A14 Module Conversion Loss Adjustment, and (optional) Factory Select Resistor Procedure.

Overall Equipment List

Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
HP-IB Printer	HP 2225A
Semi-Rigid Adapter Cable	08642-2009

NOTE

Each adjustment procedure assumes the HP 8642 cabling is connected normally and all circuitry is functioning properly.

ADJUSTMENT 1: A14 MODULE*Figure 8Q-1. Set-up 1***Required Equipment:**

Measuring Receiver	HP 8902A
Sensor Module	HP 11722A
HP-IB Printer	HP 2225A

NOTE

If the A14 Module Conversion Loss Adjustment fails, perform the Factory Select Resistor Procedure then re-perform the A14 Module Conversion Loss Adjustment. If the A14 Module Conversion Loss Adjustment still fails then there is a failure in A14 Module.

1. Setup:

Set the HP 8642 **POWER** switch to **STDBY**.

Extend the A14 Module.

Connect the Sensor Module to A13A2 J3. Ensure that the Sensor Module cal factors are entered into the Measuring Receiver and that the Measuring Receiver Power Meter is zeroed and calibrated.

Set the HP 8642 **POWER** switch to **ON**.

2. Measure the A13 Module Output Levels:

On the HP 8642 key in **SHIFT** **SPCL** **8**, **0.1** **MHz**.

Set the Measuring Receiver to measure RF Power and to display the measurement in dBm.

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Set the HP 8642 to the frequencies listed in Table 8Q-25 and record the Measuring Receiver RF Power reading for each frequency in Table 8Q-25 in the column labeled A13 Output Level. For each HP 8642 frequency key the **A13 Output Frequency** listed into the Measuring Receiver. This ensures that the Measuring Receiver uses the correct calibration factor for the Sensor Module.

Table 8Q-24. A14 Module Conversion Loss

HP 8642 Frequency	A13 Output Frequency	A13 Output Level	A14 Output Level	A14 Conversion Loss
0.1 MHz	832.6 MHz	A._____ dBm	A1._____ dBm	A-A1._____ dBm
0.2 MHz	823.7 MHz	B._____ dBm	B1._____ dBm	B-B1._____ dBm
0.5 MHz	833.0 MHz	C._____ dBm	C1._____ dBm	C-C1._____ dBm
1.0 MHz	833.5 MHz	D._____ dBm	D1._____ dBm	D-D1._____ dBm
2.0 MHz	834.5 MHz	E._____ dBm	E1._____ dBm	E-E1._____ dBm
5.0 MHz	837.5 MHz	F._____ dBm	F1._____ dBm	F-F1._____ dBm
10.0 MHz	842.5 MHz	G._____ dBm	G1._____ dBm	G-G1._____ dBm
20.0 MHz	852.5 MHz	H._____ dBm	H1._____ dBm	H-H1._____ dBm
50.0 MHz	882.5 MHz	I._____ dBm	I1._____ dBm	I-I1._____ dBm
100.0 MHz	932.5 MHz	N._____ dBm	N1._____ dBm	N-N1._____ dBm
132.18 MHz	964.5 MHz	Q._____ dBm	Q1._____ dBm	Q-Q1._____ dBm

3. Measure the A14 Module Conversion Loss:

Remove the Sensor Module from A13A2 J3.

Connect a short piece of coaxial cable between A13A2 J3 and A14U1 J2.

Connect the Sensor Module to A14U1 J3 through a short piece of coaxial cable.

Set the HP 8642 to the frequencies listed in Table 8Q-24 and record the Measuring Receiver RF Power reading for each frequency in Table 8Q-24 in the column labeled A14 Output Level. Key each **HP 8642 frequency** into the Measuring Receiver. This ensures that the Measuring Receiver uses the correct calibration factor for the Sensor Module.

Subtract the A14 Output Levels in Table 8Q-24 from the A13 Output Levels in Table 8Q-24 and record the results in the column labeled A14 Conversion Loss.

4. Adjust A14A3 R48:

If the conversion loss for the A14 Module is within ± 1 dB at all the points measured in Table 8Q-24 then A14A3 R48 does not need to be adjusted. Go to the A14 Auto-Adjustments and perform them.

If the conversion loss for the A14 Module is greater than ± 1 dB at any point measured in Table 8Q-24 then set the HP 8642 to the frequency which has the greatest conversion loss and adjust A14A3 R48 to bring the Measuring Receiver reading to within ± 1 dB of the A13 Output Level measured for that HP 8642 frequency. (Be sure to key the HP 8642 frequency into the Measuring Receiver to enable the correct Sensor calibration factor.)

Repeat steps 1 through 3.

If adjusting A14A3 R48 does not bring the A14 conversion loss within ± 1 dB then perform the Factory Select Resistor Adjustment. After selecting the Factory Select Resistor value perform steps 1 through 3.

FACTORY SELECT RESISTOR PROCEDURE

1. Setup:

Connect the Sensor Module to A13A2 J3.

On the HP 8642 key in **INST PRESET** **SHIFT** **SPCL** **8**, **30** **MHz**, **AMPTD** **-10** **dBm**

Set the Measuring Receiver to RF Power and key in 862.5 MHz.

When the RF Power reading on the Measuring Receiver is displayed, set the Measuring Receiver for a ratio reading in logarithmic units. The display should now show 0.00 dB.

2. Measure A14 conversion loss and determine A14A3 R52 value:

Set A14A3 R48 completely clockwise for maximum gain.

Remove the Sensor Module from A13A2 J3.

Connect a short piece of coaxial cable between A13A2 J2 and A14U1 J2.

Connect the Sensor Module to A14U1 J3 through a short piece of coaxial cable.

Key in 30 MHz on the Measuring Receiver. The Measuring Receiver should display between +0.6 dB to +1.2 dB. If not determine the resistance value needed for A14A3 R52 with the following formula.

A14A3 R52 resistance value = Current Value + (+/- Gain Change dB Needed/ 0.08)

Set the HP 8642 **POWER** switch to **STBY**.

Remove the Sensor Module from A14U1 J3.

Remove the A14 module from it's extender posts. Lay it on it's right side, inside of the HP 8642.

Remove the A14A3 cover.

Change A14A3 R52 to the standard value nearest the calculated value. (see Table 8Q-25 for R52 standard values) A14A3 R52 is a chip resistor located at the top of the A14A3 board between J2 and J3. Use the Component Locator on page 8Q-106 to determine it's exact location.

Table 8Q-25. A14A3 R52 Standard Values

Standard Value	HP Part Number
0.0Ω	0699-1503
5.0Ω	Two 10Ω in parallel
10.0Ω	0699-1344
14.7Ω	0699-1348
21.5Ω	0699-1352

Restore Module

3. Re-install the A14A3 cover and all cables removed when installing the new A14A3 R52.

CAUTION

When re-installing the A14A3 cover, remove the heatsink from A14A3 Q6. Then re-install the cover and screw it in place. Then screw the Q6 heatsink in place. ONLY TIGHTEN THE Q13 HEATSINK FINGER TIGHT.

4. Extend the A14 module.
5. Set the HP 8642 **POWER** switch to **ON**.
6. Repeat steps 1 and 2. If the A14 module conversion gain is now between +0.6 and +1.2 dB, then return the A14 Module Conversion Loss Adjustment and re-adjust A14A3 R48. If the A14 module conversion is still not correct then perform the Factory Select Resistor Procedure again until a correct resistor value is found.

A14 AUTO-ADJUSTMENTS

Description

The A14 Auto-Adjustment Procedure generates data that represents the difference of RF input and output Levels. The data is generated for the three different signal paths (Thru Path, Band 1, and HET Band) across the entire frequency range of each path.

Required Equipment:

Measuring Receiver	HP8902A
Sensor Module	HP11722A
HP-IB Printer	HP2225A
Semi-rigid Adapter Cable	08642-20099

1. Initialize Auto Adjust Routine:

Connect the Required Equipment to the HP 8642 via HP-IB.

Key in: **INST PRESET**.

Key in: **SHIFT SPCL 3 8 8 Hz 8 0 Hz**.

2. When "ENTER ROUTINE NUMBER .G8000" appears:

Key in: **8 Hz**.

Key in the the Day, Month, Year and Module Cal ID Number when prompted by the HP 8642 display. (See Section 5 for details.)

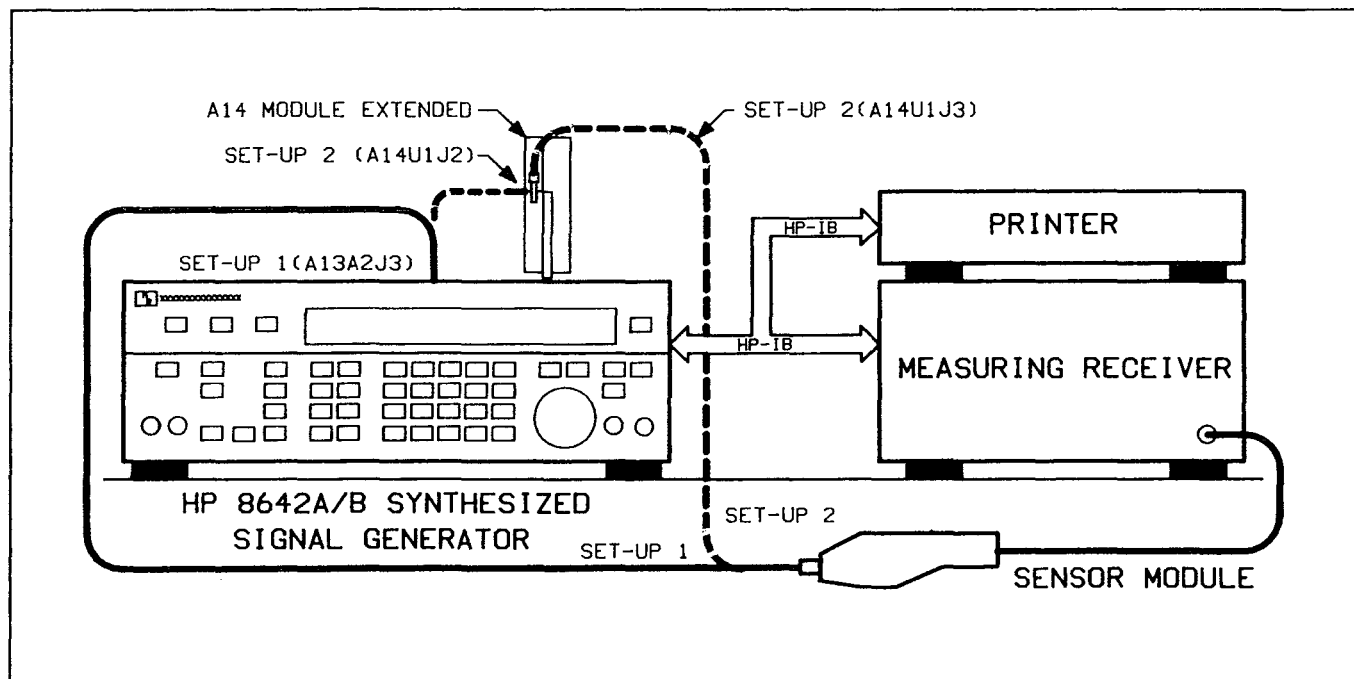


Figure 8Q-2. Set-up 1 and Set-up 2

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3. When **"WAITING FOR SET-UP 1 .V24"** appears:
Disconnect cable W34 from A14U1 J2 and A13A2 J3.
Turn the cable around and connect cable W34 to A13A2 J3, then connect the Sensor Module to the other end of W34 using a 90 degree adapter.
Press **[Hz]** to continue.
4. When **"WAITING FOR SET-UP 2 .V25"** appears:
Reconnect cable W34 to the A14 and A13 modules.
If the device under test is an HP 8642A; Disconnect W35 from A16AT1 J1.
If the device under test is an HP 8642B; Disconnect cable W36 from A19K1 J2 and A14U1 J3.
Connect the Sensor Module to A14U1 J3 using the Semi-Rigid Adapter Cable.
Press **[Hz]** to continue.
5. When **"UNPROTECT CAL. MEMORY .G8005"** appears:
Switch A3 S2 toward the rear of the instrument to unprotect the EEPROM's.
Press **[Hz]** to Continue.
6. When **"PROTECT CAL. MEMORY .G8006"** appears:
Switch A3 S2 toward the front of the instrument to protect the EEPROM's.
Press **[Hz]** to Continue.
7. When **"RECONNECT ALL CABLES .V29"** appears:
Disconnect all test cables from the instrument.
Reconnect any instrument cables which are still disconnected.
Press **[Hz]** to Continue.
8. Run the instrument level diagnostics to verify operation:
Key in: **[SHIFT] [SPCL] [3] [3] [0] [Hz]**.
When **"WAITING FOR SETUP 1 .Z24"** appears, connect the MOD OUT to the AM/PULSE INPUT and FM/ΦM INPUT.
Press **[Hz]** to Continue.
9. When **"DIAG DONE HIT MSSGS .V1"** appears:
Press the MSSG key to view the message buffer. If **"NO MESSAGES .00"** is contained in the message buffer, the HP 8642 is functioning properly.

10. Up Load Cal Data:

Now that the functionality of the HP 8642 has been verified, used the following procedure to up load the new cal data.

Switch the HP 8642 to standby.

Remove the A20 Cal Module. (See Disassembly Procedures).

Plug the A20 Module on to A3 J3.

Switch the HP 8642 on.

Switch A20 S1 to the CHANGE position.

Key in: **SHIFT** **SPCL** **3** **7** **2** **8** **Hz**.

When “**TRANSFER VERIFIED .U613**” appears on the display, move A20 S1 up to its PROTECTED position.

Key in: **Hz** to end the routine.

Switch the HP 8642 to Standby.

Reconnect the A20 module to the rear panel (See Disassembly Procedures).

Re-install the top cover.

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A14 CRITICAL SPECIFICATIONS**Table 8Q-26. A14 Output Specifications**

Output Power Level	3.65 to 4.35 dBm
Spurs	< - 100 dBc
Harmonics 2 nd	< - 10 dBc
SAWR Oscillator Pull Range	- 80 ppm to + 130 ppm
Time Base Return Power	< - 60 dBc

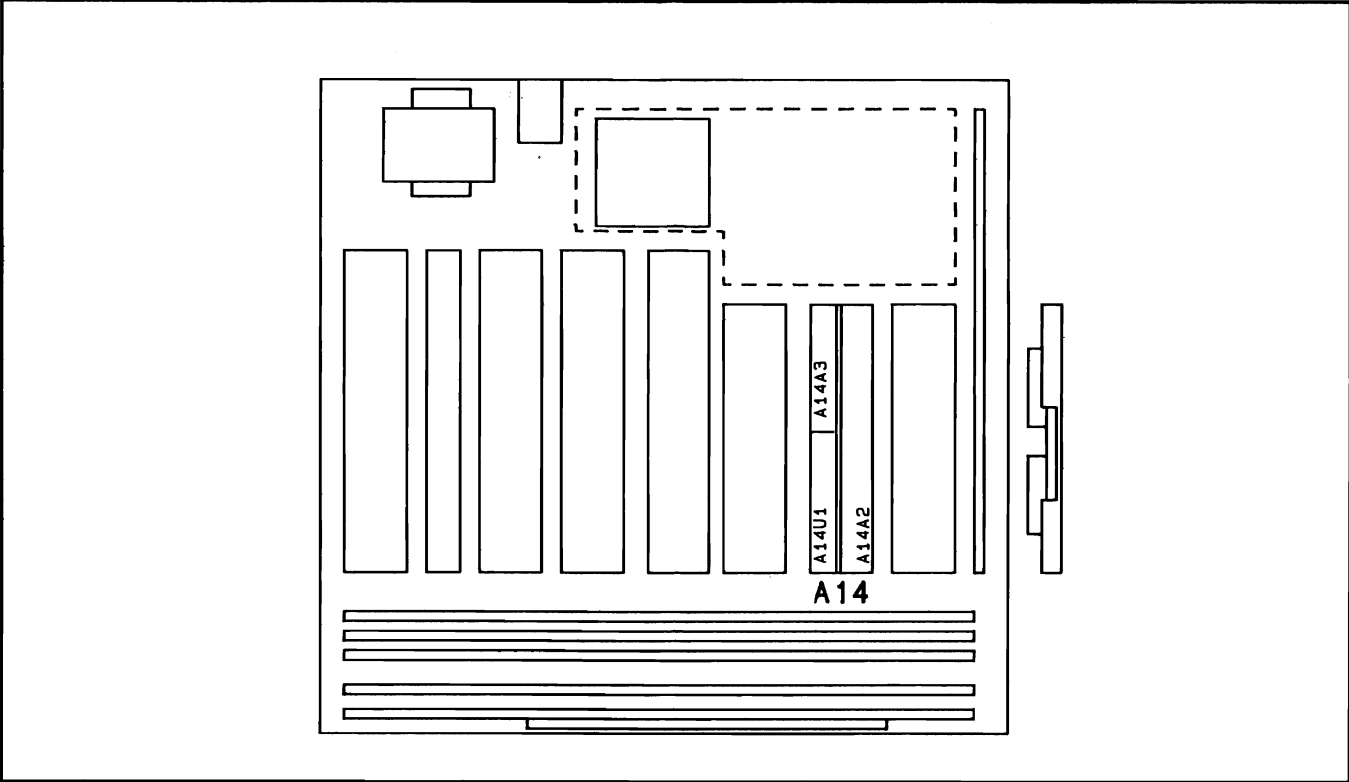
Table 8Q-27. A14A2 Oscillator Assembly Specifications*

Measurement	Results
Harmonics HET Band Band 1	f2 < -12 dBc f2 < -10 dBc f3 < -8 dBc f4 < -15 dBc f5 < -8 dBc f6 < -15 dBc
Spurs HET Bands	< -90 dBc
* Measured at A14A2J4	

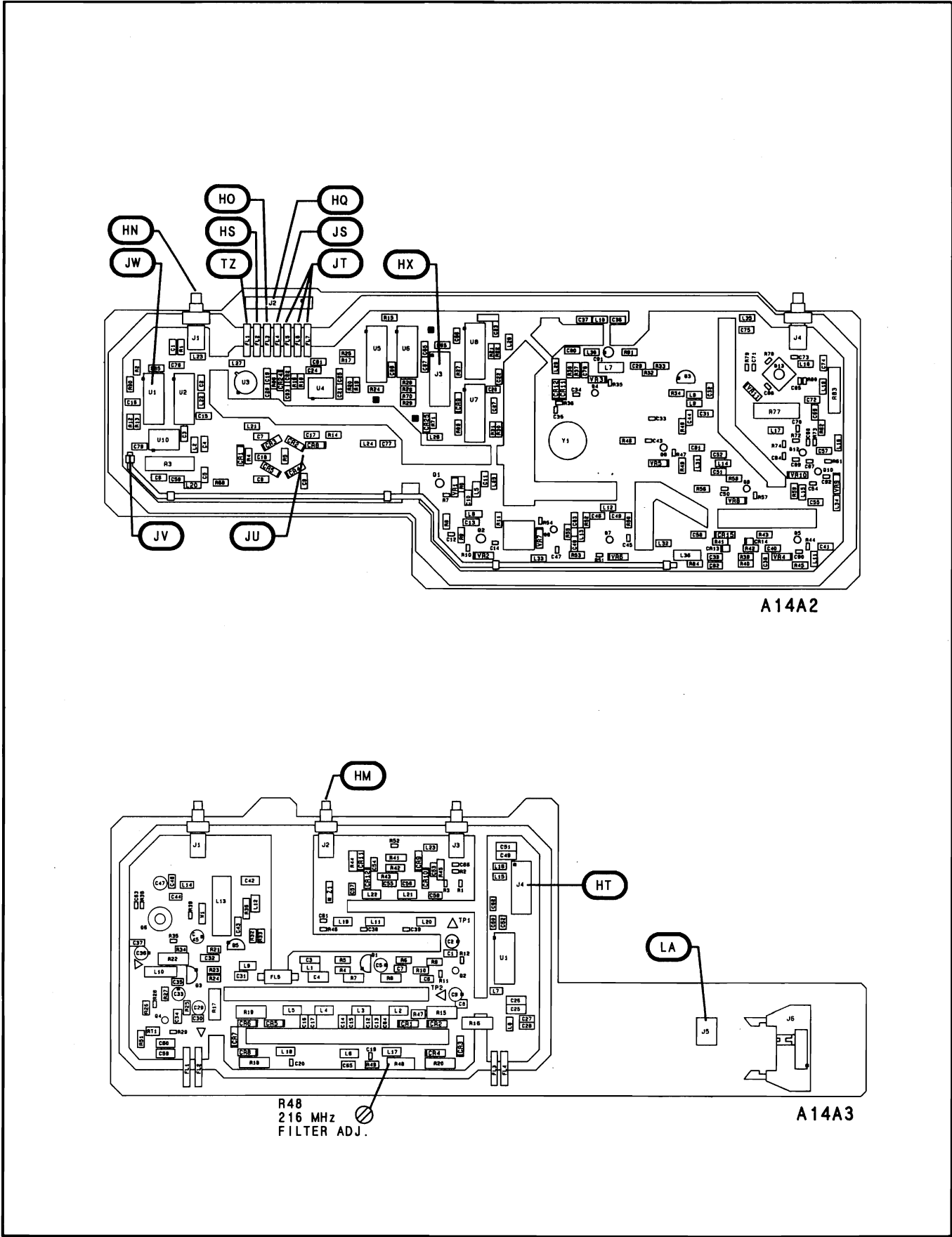
Table 8Q-28. A14A3 Heterodyne Assembly Specifications*

Measurement	Results
Harmonics HET Band @ +10 dBm @ +17 dBm Band 1 @ +10 dBm @ +10 dBm	< -35 dBc < -25 dBc < -35 dBc < -25 dBc
Spurs HET Band Band 1 AM Specs	< -105 dBc < -75 dBc
Accuracy HET Band Band 1 Distortion HET Band Band 1 Residual AM HET Band Band 1	≤ 1% ≤ 1% ≤ 2% THD ≤ 2% THD ≤ .02% ≤ .02%
* Measured at A14A3J1	

Assembly Locator



Module Test Point/Adjustment Locations



Simplified Block Diagram

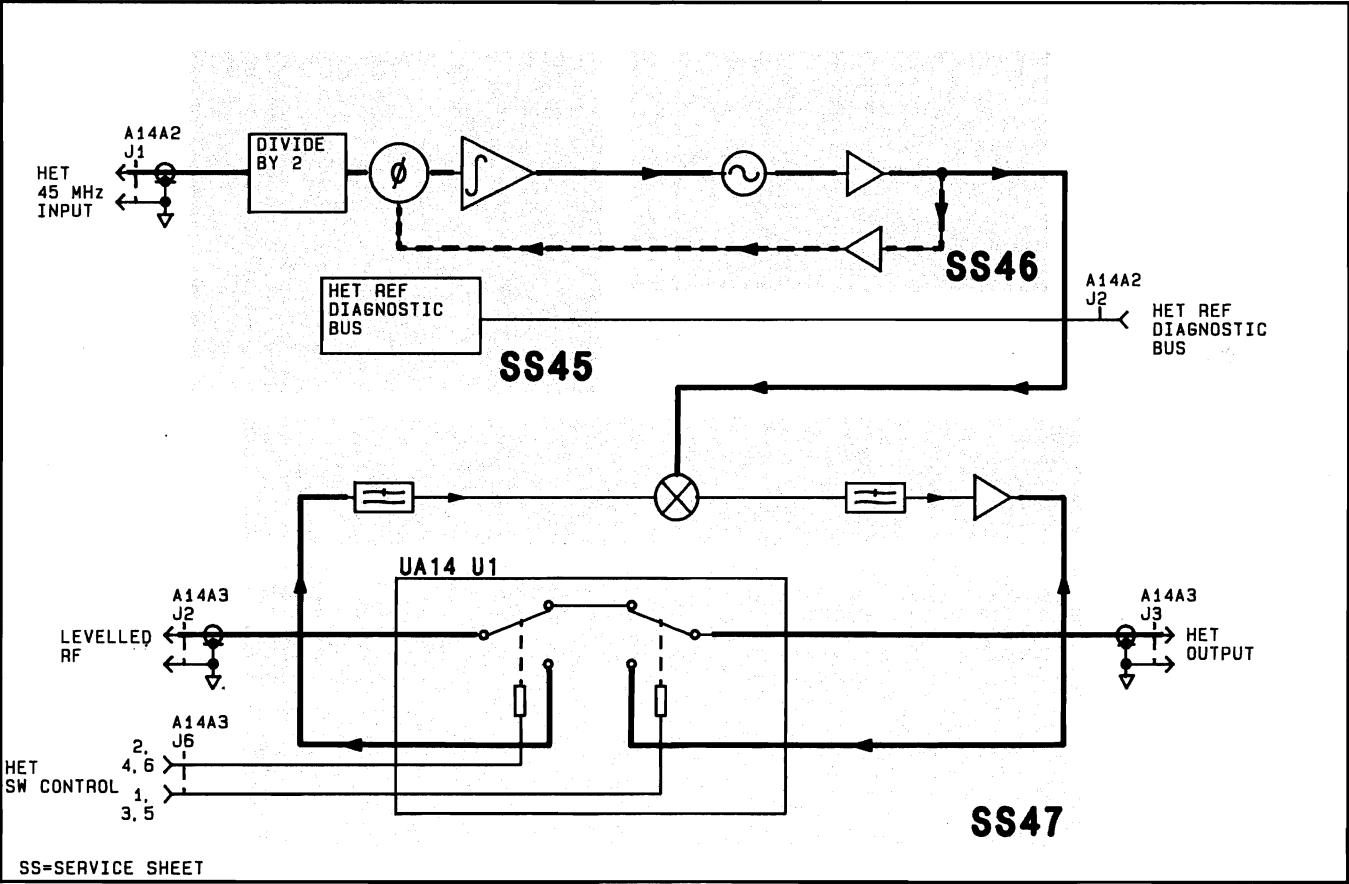


Figure 8Q-100 BD15 General Information.

CHANGES**2509A and above**

On the block diagram:

- A14A2 - In the upper left portion of the block diagram, change the A14A2 assembly number to 08642-60215.

2526A and above

On the block diagram:

- A14A2 - In the upper left portion of the block diagram, change the A14A2 assembly number to 08642-60315.

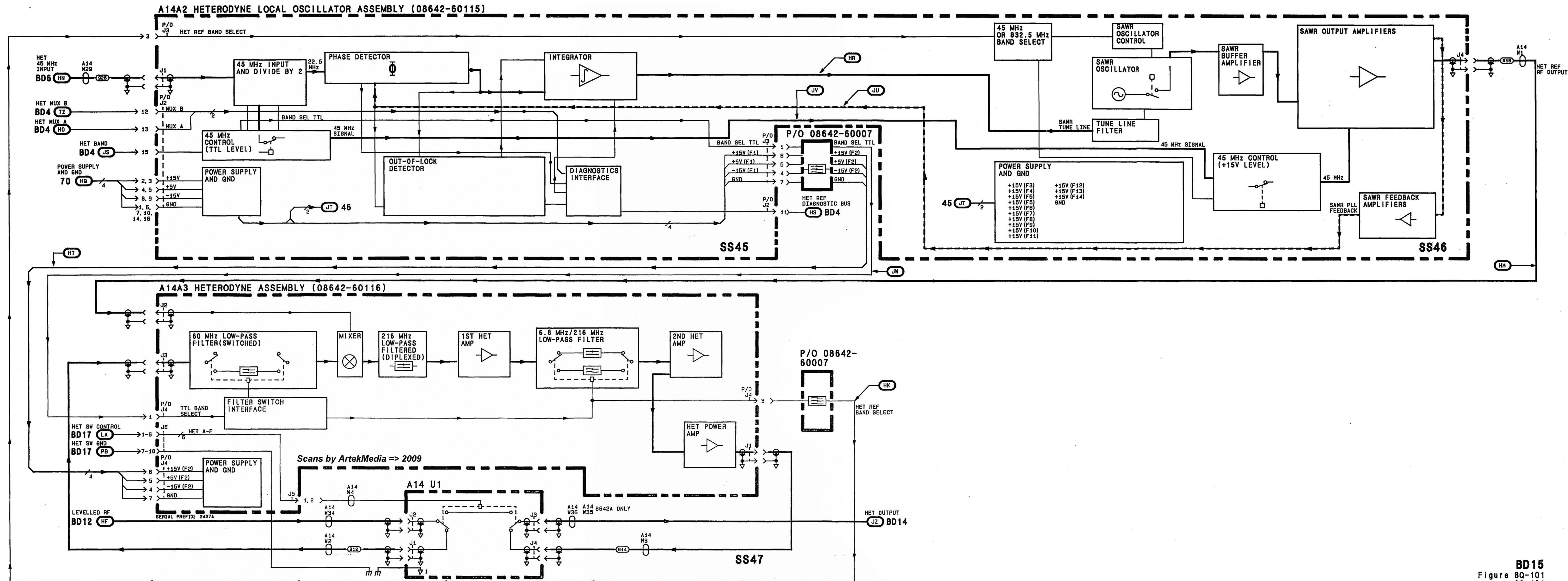


Figure **BD 15**
8Q-101
8Q-101

A14 MODULE **BD 15**

Schematic General Information

CHANGES

All Serial Prefixes

On the schematic:

- U6 - In **OUT-OF-LOCK DETECTOR**, change U6D pin 4 to the inverting input and pin 5 to the non-inverting input.

2514A and above

On the Component Locator:

- R92 - Add R92 between C15 and L21.

In Component Coordinates:

- R92 - Add R92, A,2.

On the schematic:

- R92 - In **PHASE DETECTOR**, add a resistor from U3 pin 3 to ground. Designate it R92 and assign a value of 1M ohms.

2526A and above

On the Component Locator:

- Note changes shown on 8Q-102.3

On the schematic:

- In the upper left portion of the schematic, change the A14A2 part number to 08642-60315.
- R3 - Replace the appropriate portion of the schematic with the partial on page 8Q-102.2

2714A and above

On the schematic:

- R24 - In **INTEGRATOR**, change the value of R24 to 28.7K.

CHANGES**All Serial Prefixes**

On the schematic:

- U6 - In **OUT-OF-LOCK DETECTOR**, change U6D pin 4 to the inverting input and pin 5 to the non-inverting input.

2514A and above

On the Component Locator:

- R92 - Add R92 between C15 and L21.

In Component Coordinates:

- R92 - Add R92, A,2.

On the schematic:

- R92 - In **PHASE DETECTOR**, add a resistor from U3 pin 3 to ground. Designate it R92 and assign a value of 1M ohms.

2526A and above

On the Component Locator:

- Note changes shown on 8Q-102.3

On the schematic:

- In the upper left portion of the schematic, change the A14A2 part number to 08642-60315.
- R3 - Replace the appropriate portion of the schematic with the partial on page 8Q-102.2

2714A and above

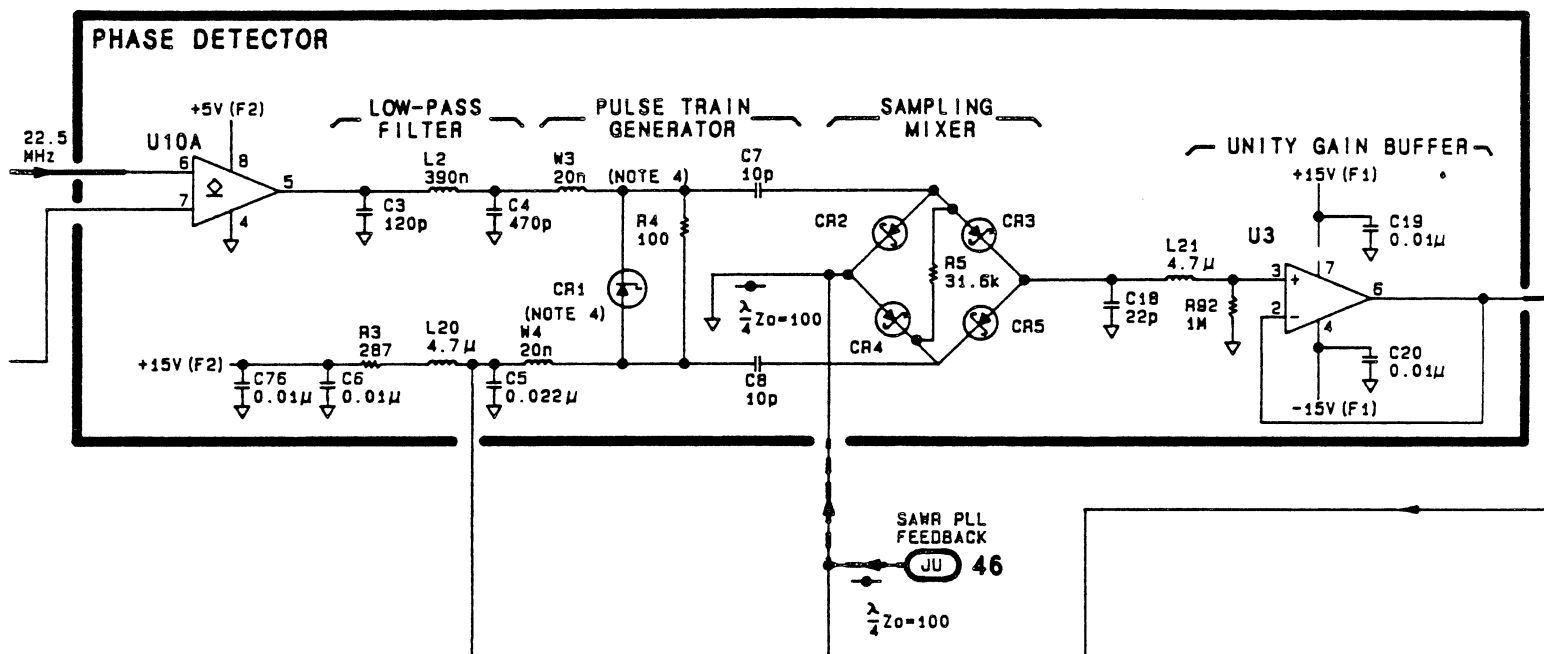
On the schematic:

- R24 - In **INTEGRATOR**, change the value of R24 to 28.7K.

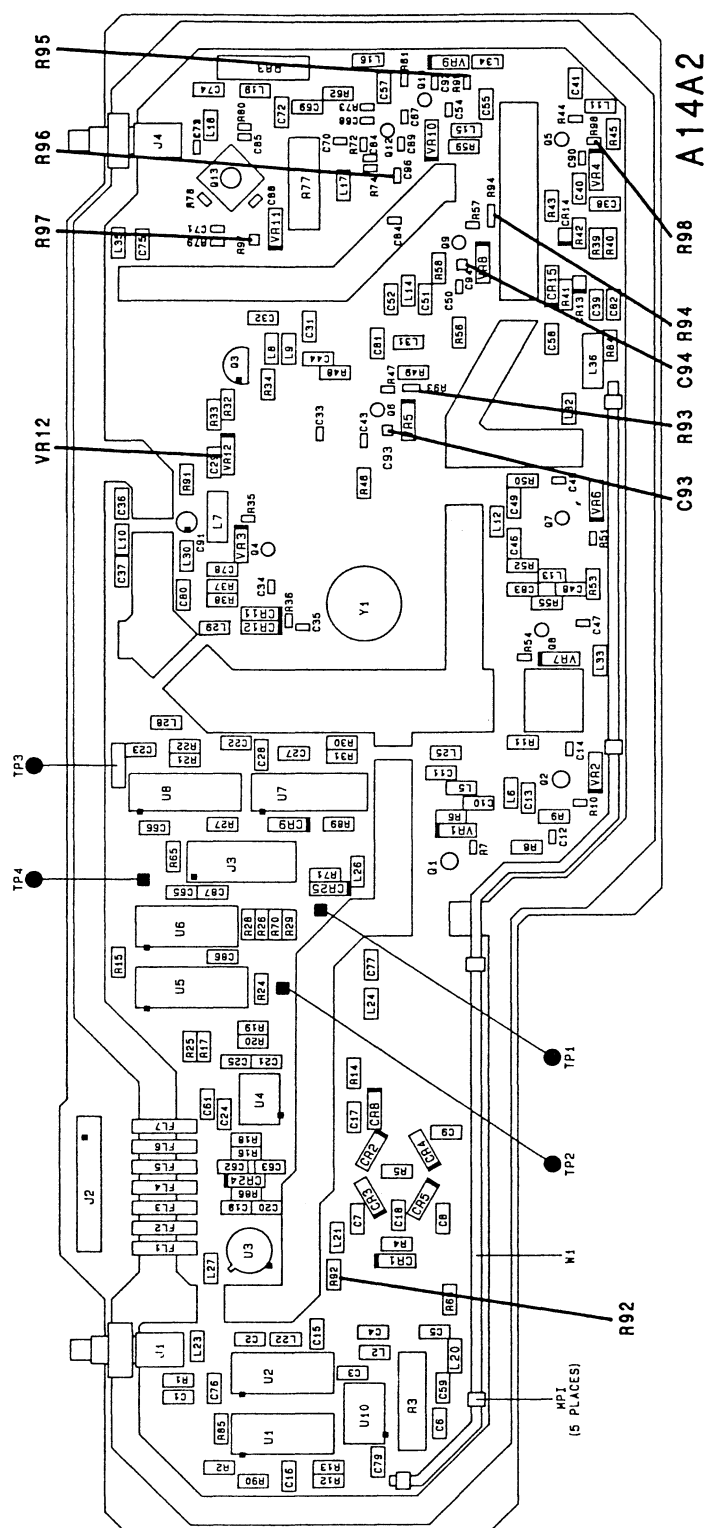
2744A and above

On the schematic:

- L2 - In **PHASE DETECTOR**, change the value of L2 to 430n.

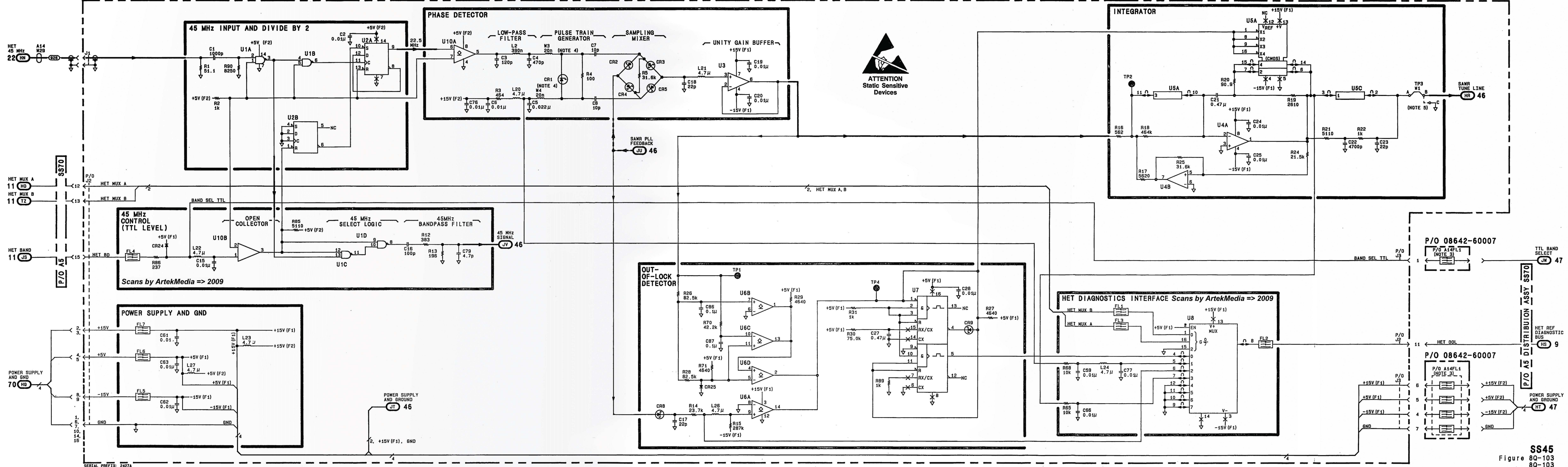


P/O FIGURE 8Q-103 (2526A and above)



CHANGES TO FIGURE 8Q-102 (2526A and above)

P/O A14A2 HETERODYNE LOCAL OSCILLATOR ASSEMBLY (08642-60115)

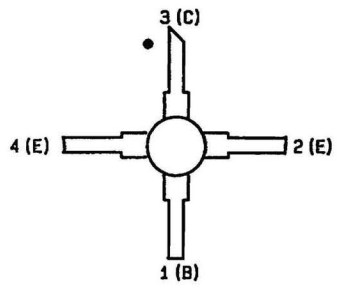


SS45
Figure 8Q-103
8Q-103

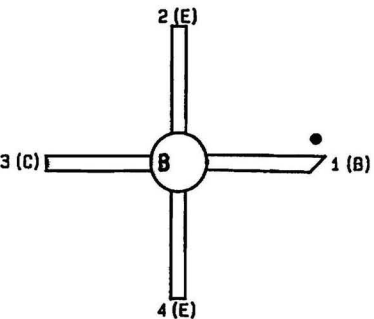
Notes:

- 1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- 2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
- 3. W4 and W5 are printed circuit trace inductors.
- 4. W2 is semi rigid coax cable.

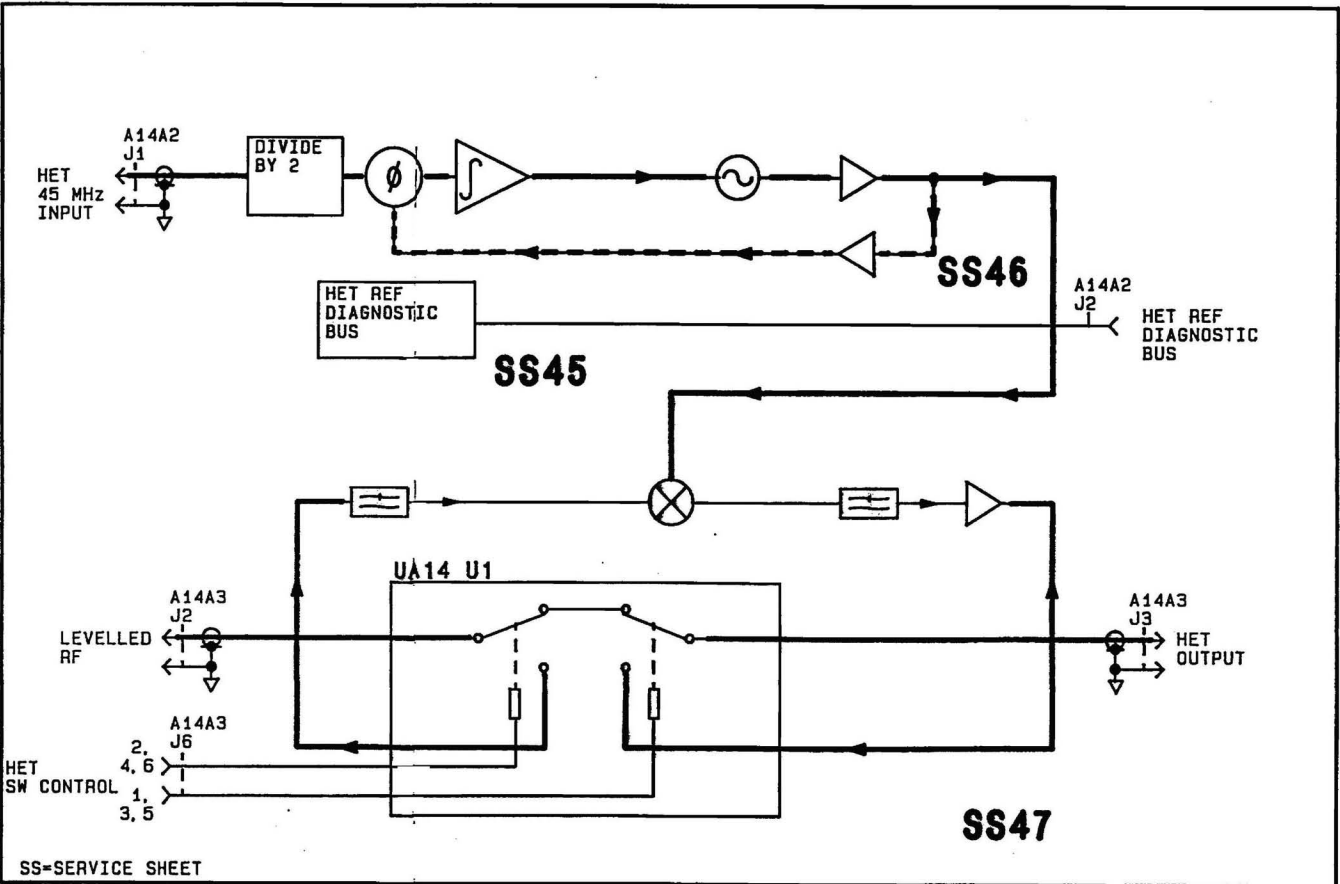
A14A2
Q13
1854-1036



A14A2
Q1, Q2, Q4-Q10, Q12



Schematic General Information



Reference Block Diagram

Component Coordinates

COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y
C9	B, 2	C71	D, 1	L15	D, 2	R32	D, 2	R83	D, 1								
C10	B, 3	C72	D, 2	L16	D, 2	R33	C, 1	R84	D, 3								
C11	C, 2	C73	D, 1	L17	D, 2	R34	D, 2	R91	C, 1								
C12	B, 3	C74	D, 1	L18	D, 1	R35	C, 1										
C13	B, 3	C75	D, 1	L19	D, 1	R36	C, 2	VR1	B, 2								
C14	C, 3	C76	C, 1	L20	C, 1	R37	C, 2	VR2	B, 3								
C29	C, 1	C80	C, 1	L28	C, 1	R38	C, 1	VR3	C, 1								
C31	D, 2	C81	D, 2	L29	C, 1	R39	D, 3	VR4	D, 3								
C32	D, 1	C82	D, 3	L30	C, 1	R40	D, 3	VR5	C, 2								
C33	C, 2	C83	C, 3	L31	D, 3	R41	D, 3	VR6	C, 3								
C34	C, 2	C84	D, 2	L32	C, 3	R42	D, 3	VR7	C, 3								
C35	C, 2	C85	D, 1	L33	C, 3	R43	D, 3	VR8	D, 3								
C36	C, 2	C86	D, 1	L34	D, 3	R44	D, 3	VR9	D, 2								
C37	C, 1	C89	D, 2	L35	D, 1	R45	D, 3	VR10	D, 2								
C38	D, 3	C90	D, 3	L36	D, 3	R46	D, 3	VR11	D, 1								
C39	D, 3	C91	C, 1			R47	D, 3										
C40	D, 3	C92	D, 2	MP1	C, 3	R48	D, 2	Y1	C, 2								
C41	D, 3					R49	D, 2										
C43	C, 2	CR11	C, 1	Q1	B, 2	R50	C, 3										
C44	C, 2	CR12	C, 1	Q2	D, 1	R51	C, 3										
C45	C, 3	CR13	D, 3	Q3	D, 1	R52	C, 3										
C46	C, 3	CR14	D, 3	Q4	C, 2	R53	C, 3										
C47	C, 3	CR15	D, 3	Q5	D, 3	R54	C, 3										
C48	C, 3			Q6	C, 2	R55	C, 3										
C49	C, 3	J3	B, 1	Q7	C, 2	R56	C, 3										
C50	D, 2	J4	D, 1	Q8	D, 2	R57	D, 3										
C51	D, 2			Q9	D, 2	R58	D, 2										
C52	D, 2	L5	B, 2	Q10	D, 2	R59	D, 2										
C54	D, 2	L6	B, 3	Q12	D, 2	R61	D, 2										
C55	D, 2	L7	C, 1	Q13	D, 1	R62	D, 2										
C57	D, 2	L8	D, 2			R72	D, 2										
C58	D, 3	L9	D, 2	R6	B, 2	R73	D, 2										
C59	B, 1	L10	C, 1	R7	B, 3	R74	D, 2										
C67	D, 2	L11	D, 3	R8	B, 3	R77	D, 2										
C68	D, 2	L12	D, 3	R9	D, 3	R78	D, 3										
C69	D, 2	L13	C, 3	R10	D, 3	R79	D, 1										
C70	D, 2	L14	D, 2	R11	C, 3	R80	D, 1										

P/O HETERODYNE LOCAL
A14A2 OSCILLATOR ASSEMBLY
SEE REVERSE SIDE

SS45

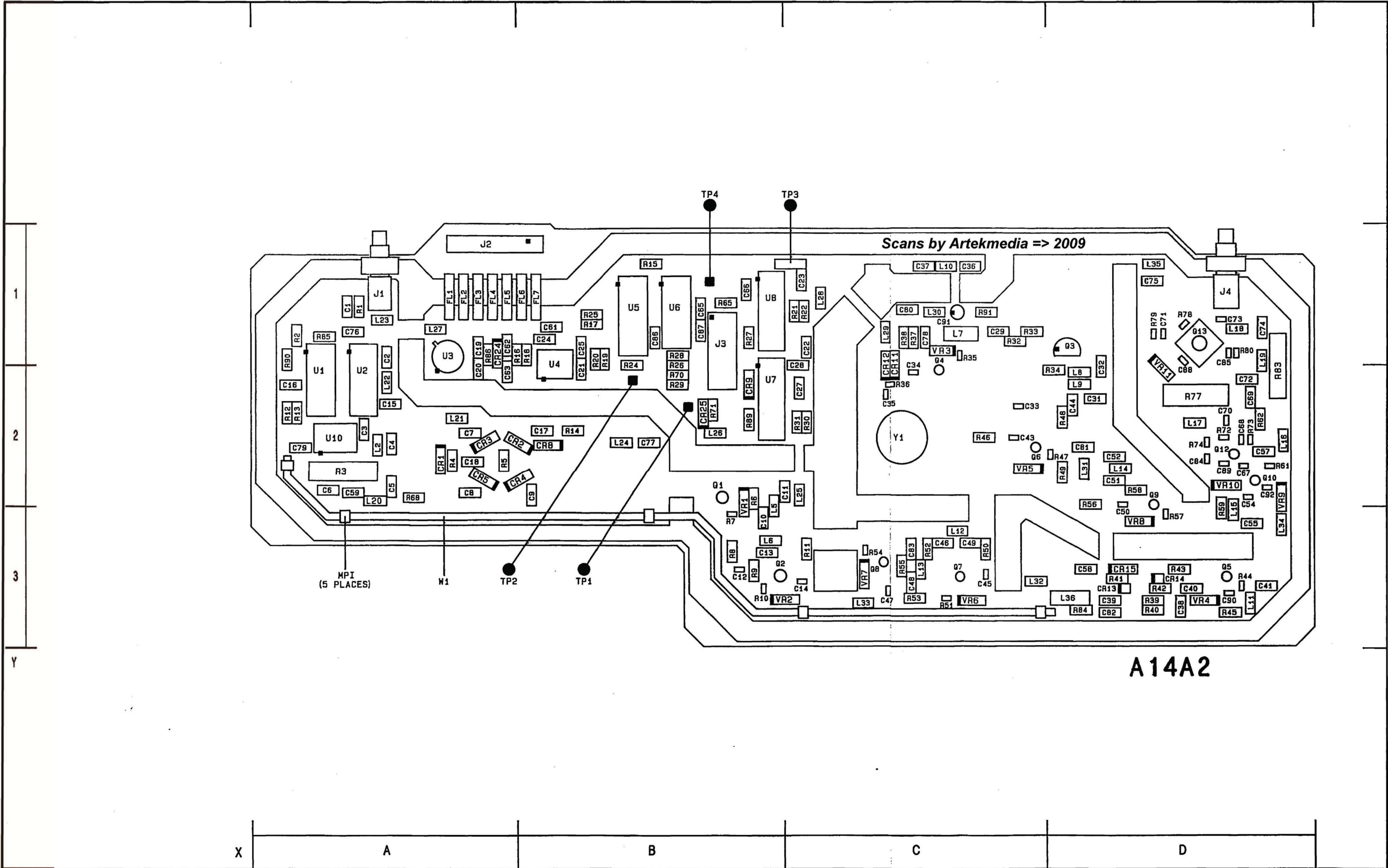


Figure 8Q-104. SERVICE SHEET 46 INFORMATION

Component Locator

CHANGES**All Serial Prefixes**

On the schematic:

- C43, R46 - In **SAWR BUFFER AMPLIFIER**, move C43 to the right of R46.

2427A to 2507A

On the schematic:

- C93 - In **SAWR OSCILLATOR**, change C93 to 3.9p.

2509A and above

On the schematic:

- C93, W3 - In **SAWR OSCILLATOR**, remove C93 and W3.
- In the top left portion of the schematic, change the assembly number to 08642-60215. In the bottom left portion of the schematic, change the serial prefix to 2509A.

2526A and above

On the Component Locator:

- C93, C94, R93, R94, R95, R96, R97, R98 - Note changes to Component Locator shown on page 8Q-104.3

In Component Coordinates:

- C93, C94, R93, R94, R95, R96, R97 - Add the following components and coordinates to the Component Coordinates table:
C93 C,2
C94 D,3
R93 C,2
R95 D,3
R96 D,2
R97 C,1

On the schematic:

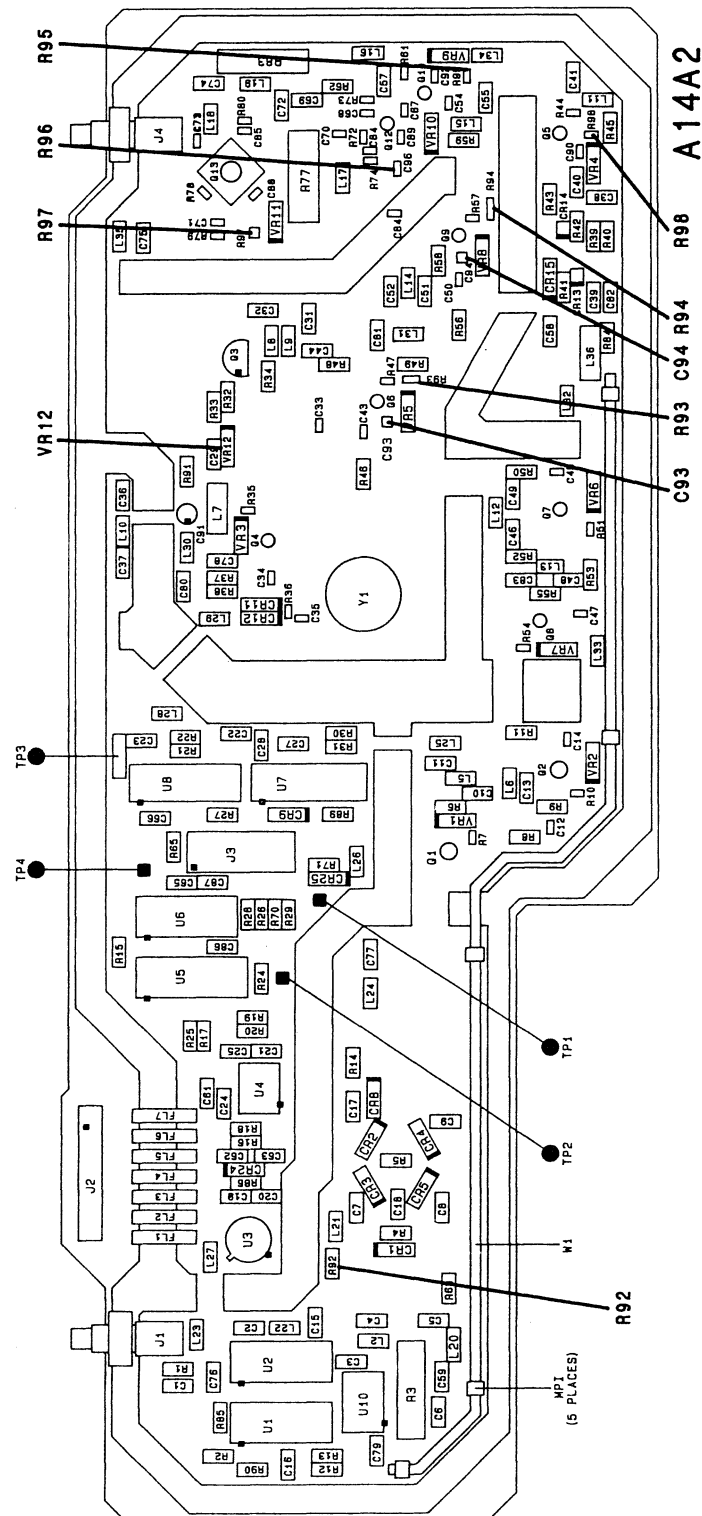
- C89, C90, C93, C94, R32, R93, R94, R95, R96, R97, R98 - Replace SS46 with the foldout on page 8Q-104.5

On the foldout (page 8Q-104.5):

- L16 - In **SAWR OUTPUT AMPLIFIERS**, under **BUFFER AMPS**, replace L16 with a circuit trace. On the circuit board this is a wire jumper.
- R44 - In **45 MHz CONTROL (+15V LEVEL)**, under **45 MHz AMPLIFIER**, change the value of R44 from 1470 to 215 ohms.

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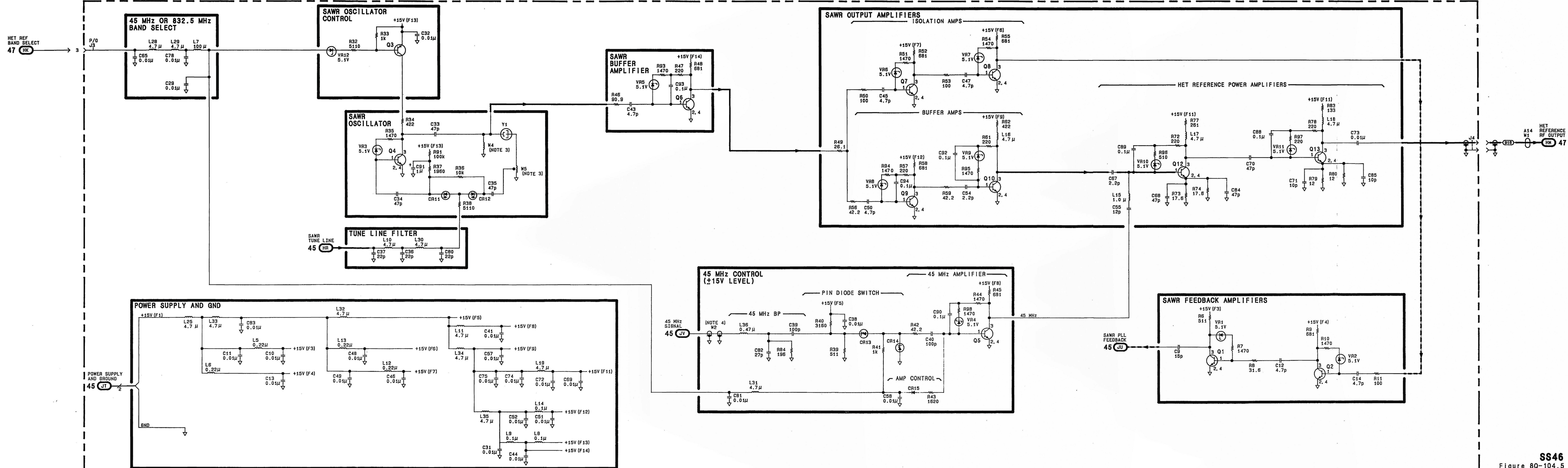


CHANGES TO FIGURE 8Q-104 (2526A and above)

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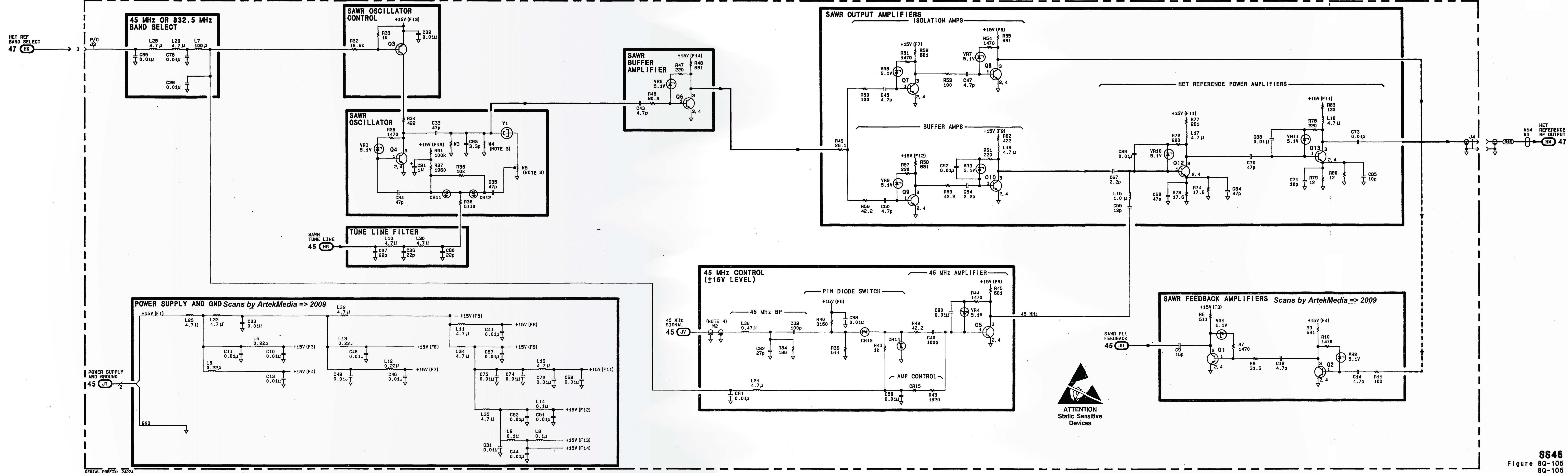
P/O A14A2 HETERODYNE LOCAL OSCILLATOR ASSEMBLY (08642-60315)



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P/O A14A2 HETERODYNE LOCAL OSCILLATOR ASSEMBLY (08642-60115)



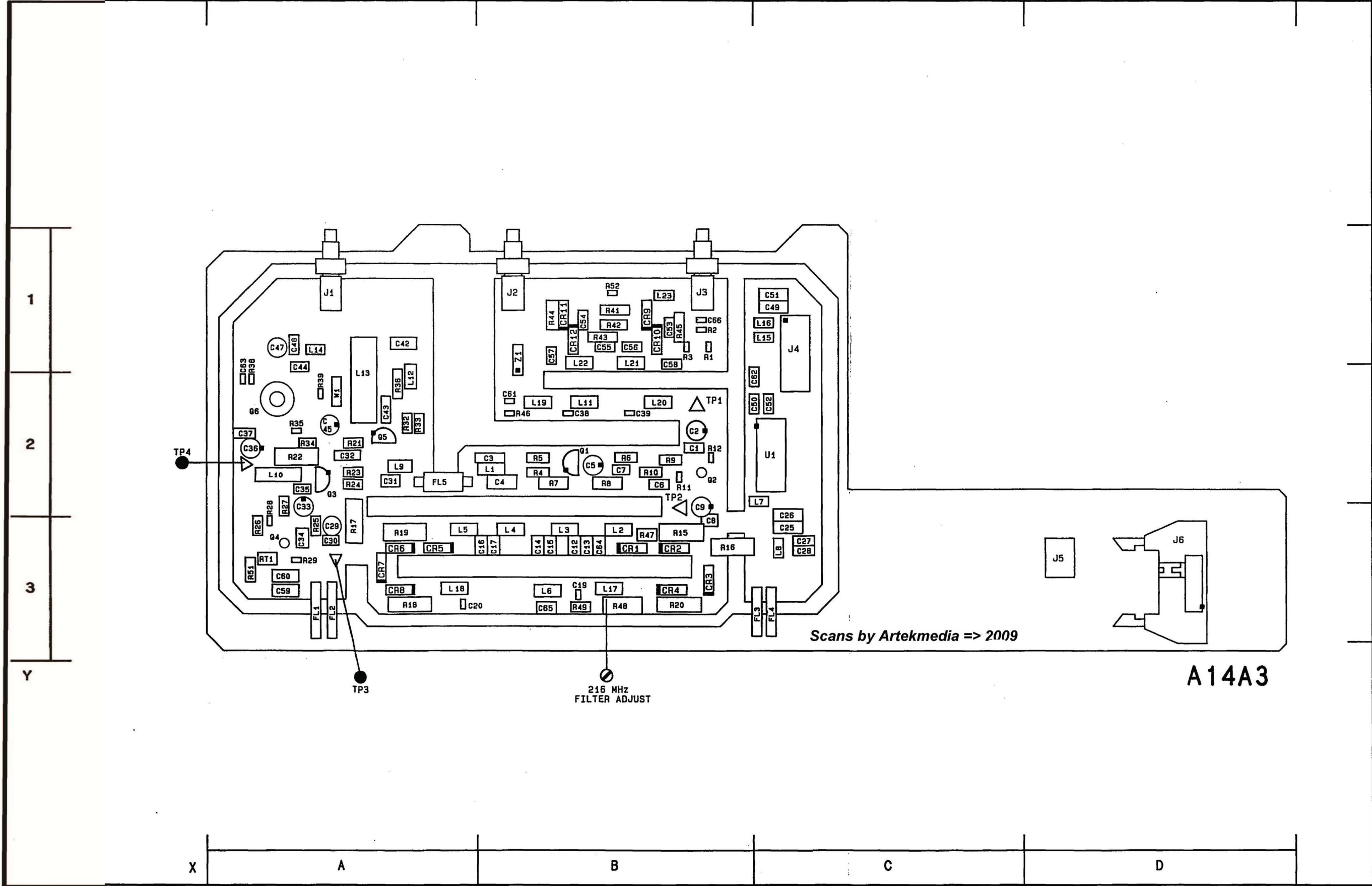
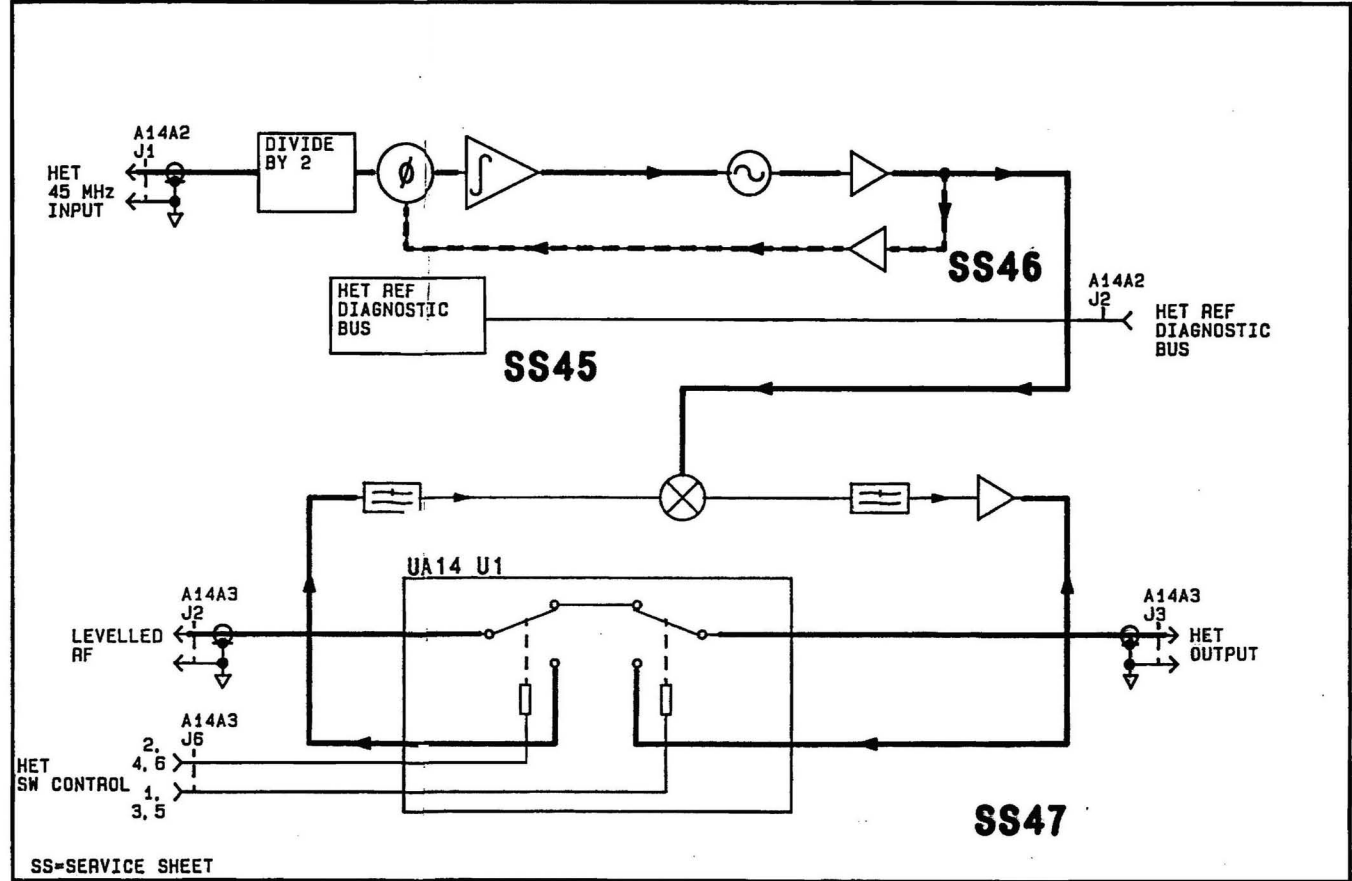


Figure 8Q-106. SERVICE SHEET 47 INFORMATION

Component Locator



Reference Block Diagram

Component Coordinates

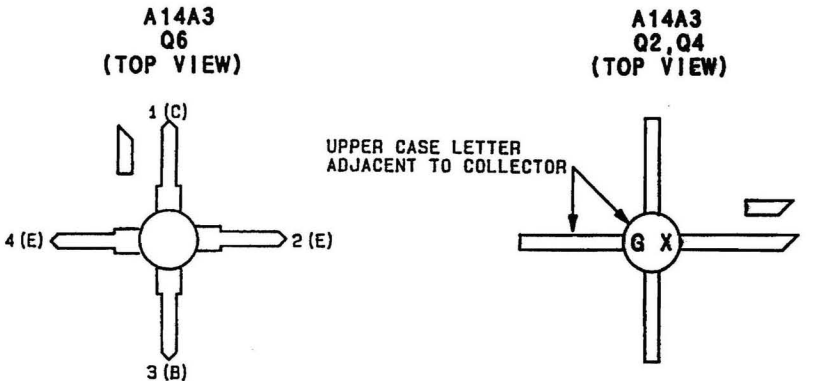
COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y
C1	B, 2	C48	A, 1	FL1	A, 3	Q1	B, 2	R36	A, 2										
C2	B, 2	C49	C, 1	FL2	A, 3	Q3	B, 2	R38	A, 2										
C3	B, 2	C50	C, 2	FL3	C, 3	Q4	A, 3	R39	A, 2										
C4	B, 2	C51	C, 1	FL4	C, 3	Q5	A, 2	R41	B, 1										
C5	B, 2	C52	C, 2	FL5	A, 2	Q6	A, 2	R42	B, 1										
C6	B, 2	C53	B, 1	J1	A, 1	R1	B, 1	R44	B, 1										
C7	B, 2	C54	B, 1	J2	B, 1	R2	B, 1	R45	B, 1										
C8	B, 3	C55	B, 1	J3	B, 1	R3	B, 1	R46	B, 2										
C9	B, 2	C56	B, 1	J4	C, 4	R4	B, 1	R47	B, 3										
C12	B, 3	C57	B, 1	J5	D, 3	R5	B, 2	R48	B, 3										
C13	B, 3	C58	B, 1	J6	D, 3	R6	B, 2	R49	B, 3										
C14	B, 3	C59	A, 3	L1	B, 2	R7	B, 2	R51	A, 3										
C15	B, 3	C60	A, 3	L2	B, 2	R8	B, 2	R52	B, 1										
C16	B, 3	C61	B, 2	L3	B, 3	R9	B, 2												
C17	B, 3	C62	A, 2	L4	B, 3	R10	B, 2												
C18	B, 3	C63	A, 2	L5	A, 3	R11	B, 2												
C19	B, 3	C64	B, 3	L6	B, 3	R12	B, 2	TP1	B, 2										
C20	A, 3	C65	B, 3	L7	C, 3	R13	B, 3	TP2	B, 2										
C25	C, 3	C66	B, 1	L8	A, 3	R14	B, 3	TP3	A, 2										
C26	C, 3			L9	A, 2	R15	B, 3	TP4	A, 3										
C27	C, 3			L10	A, 2	R16	B, 3												
C28	C, 3	CR1	B, 3	L11	B, 2	R17	A, 3												
C29	A, 3	CR2	B, 3	L12	A, 2	R18	A, 3												
C30	A, 3	CR3	B, 3	L13	A, 2	R19	A, 3	U1	C, 2										
C31	A, 2	CR4	B, 3	L14	A, 1	R20	B, 3	W1	A, 2										
C32	A, 2	CR5	A, 3	L15	C, 1	R21	A, 2												
C33	A, 3	CR6	A, 3	L16	C, 1	R22	A, 2												
C34	A, 3	CR7	A, 3	L17	A, 3	R23	A, 2	Z1	B, 1										
C35	A, 2	CR8	A, 3	L18	A, 3	R24	A, 2												
C36	A, 2	CR9	B, 1	L19	B, 2	R25	A, 3												
C37	B, 1	CR10	B, 1	L20	B, 2	R26	A, 3												
C38	B, 2	CR11	B, 1	L21	B, 1	R27	A, 3												
C39	B, 2	CR12	B, 1	L22	B, 1	R28	A, 3												
C42	A, 1			L23	B, 1	R29	A, 3												
C43	A, 2					R30	A, 2												
C44	A, 2					R31	B, 1												
C45	A, 2					R32	A, 2												
C47	A, 1					R33	B, 1												
						R34	A, 2												
						R35	A, 2												

P/O HETERODYNE LOCAL
A14A2 OSCILLATOR ASSEMBLY
SEE REVERSE SIDE

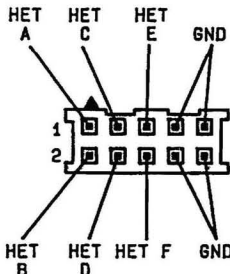
SS46

Notes:

- Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
- A14FL1 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.
- Het switch circuit common (W1 on A14U1) is connected to J6 pins 7-10 through chassis parts. These lines are a ground for the het switch (A14U1) coming from the A17 module.



CABLE PLUG TO A14A3 J6



Schematic General Information

CHANGES

All serial prefixes	<p>On the Component Locator:</p> <ul style="list-style-type: none"> • <u>A14A3R53</u> - Immediately to the left of J1, add R53. <p>In Component Coordinates:</p> <ul style="list-style-type: none"> • <u>A14A3R53</u> - Add R53 (A,1). <p>In Schematic General Information:</p> <ul style="list-style-type: none"> • <u>A14A3Q6</u> -Switch "(C)" and "(B)". • <u>A14A3Q2, Q4</u> - Beginning at the symbol for the angled lead, number the leads clockwise as 1, 2, 3, 4. <p>On the A14A3 schematic:</p> <ul style="list-style-type: none"> • <u>A14A3R52</u> - In 60 MHz LOW PASS FILTER (SWITCHED), change the value of R52 to 26.1 ohms. • <u>A14A3R53</u> - In HET POWER AMP, immediately to the right of the parallel combination of C47 and C48, add the following resistor, R53 10K ohms to ground. • <u>W34, W35, W36</u> - A14 U1 cables with reference designators A14W34, A14W35, and A14W36 should have the A14 deleted. On the lower right portion of the schematic, change "HET OUTPUT" service sheet numbers to 50 (8642B), and, 48 (8642A). • <u>A14A3R52</u> - Add an asterisk (*) to R52 located in the upper right portion of the 60 MHz LOW PASS FILTER (SWITCHED) to indicate a factory selected component.
2531A and above	<p>On the A14A3 schematic:</p> <ul style="list-style-type: none"> • <u>R47,R48,R49,R52</u> - In 60 MHz LOW PASS FILTER (SWITCHED), change the value of R52 to 14.7 ohms. In 6.8 MHz/216 MHz LOW-PASS FILTER, change the following components to their corresponding values: R47 (196 ohms), R48 (500 ohms), R49 (75 ohms).

CHANGES

2642A to 2807A

On the Component Locator:

- A14A3CR13, CR14, CR15 - Replace the portion of the component locator with the partial on page 8Q-106.5.

In Component Coordinates:

- CR13, CR14, CR15 - Add CR13 (B,2), CR14 (A,3), and, CR15 (A,2).

On the A14A3 schematic:

- A14A3CR13 - In 1st HET AMP, add CR13 by connecting the anode to ground and connect the cathode to the base of Q2.
- A14A3CR14 - In 2nd HET AMP, add CR14 by connecting the anode to ground and the cathode to the base of Q4.
- A14A3CR15 - In HET POWER AMP, add CR15 by connecting the anode to ground and the cathode to the base of Q6.

2825A and above

On the A14A3 schematic:

- Use the new schematic partial on page 8Q-106.7 for serial prefixes 2825A and above.
- R10, C7 - In 1ST HET AMP change the value of R10 to 21.5 ohms and C7 to 30p.
- R66 - In 6.8 MHz/216 MHz LOW-PASS FILTER, add R66 14.7k in parallel with C65.
- R27,C35, R51 - In 2ND HET AMP remove R27 and C35. Change R51 to 10 ohms.

On the Component Locator:

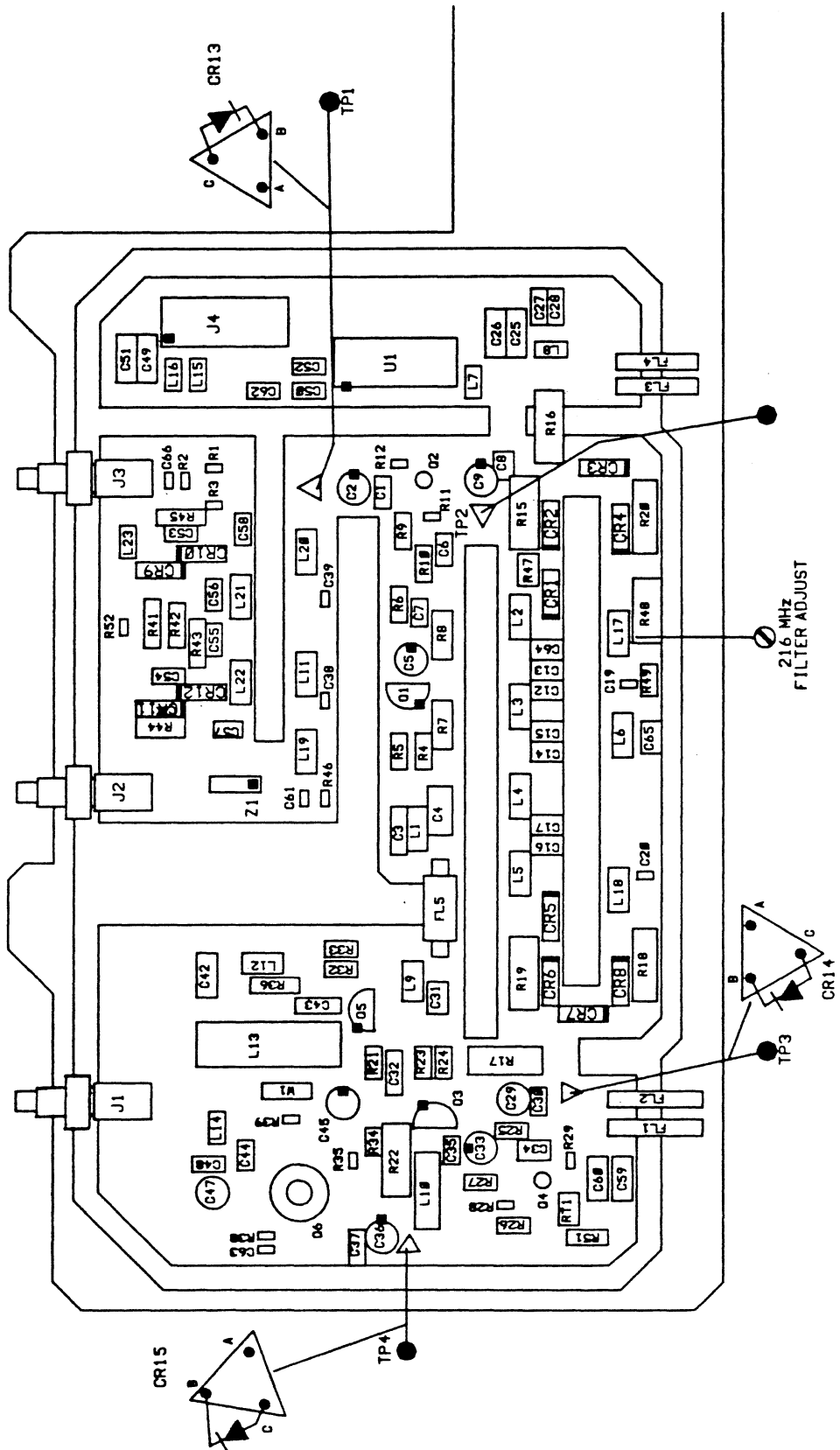
- Use the new component locator on page 8Q-106.6 for serial prefixes 2825A and above.

On the Component Coordinates:

- Delete R27 (A2).
- Add the following or change the coordinates of the following:

C13	(B3)	L7	(B3)	R61	(C2)
C50	(C1)	R16	(B3)	R64	(C2)
C52	(C1)	R50	(A1)	R65	(C2)
C62	(B1)	R53	(A1)	Q7	(C2)
C64	(B3)	R54	(C2)	Q8	(C3)
C67	(C2)	R55	(B2)	Q9	(C2)
C68	(C2)	R56	(C2)	Q10	(B2)
CR14	(A2)	R57	(C2)	U1	(C2)
CR15	(A2)	R60	(C2)		

SS47



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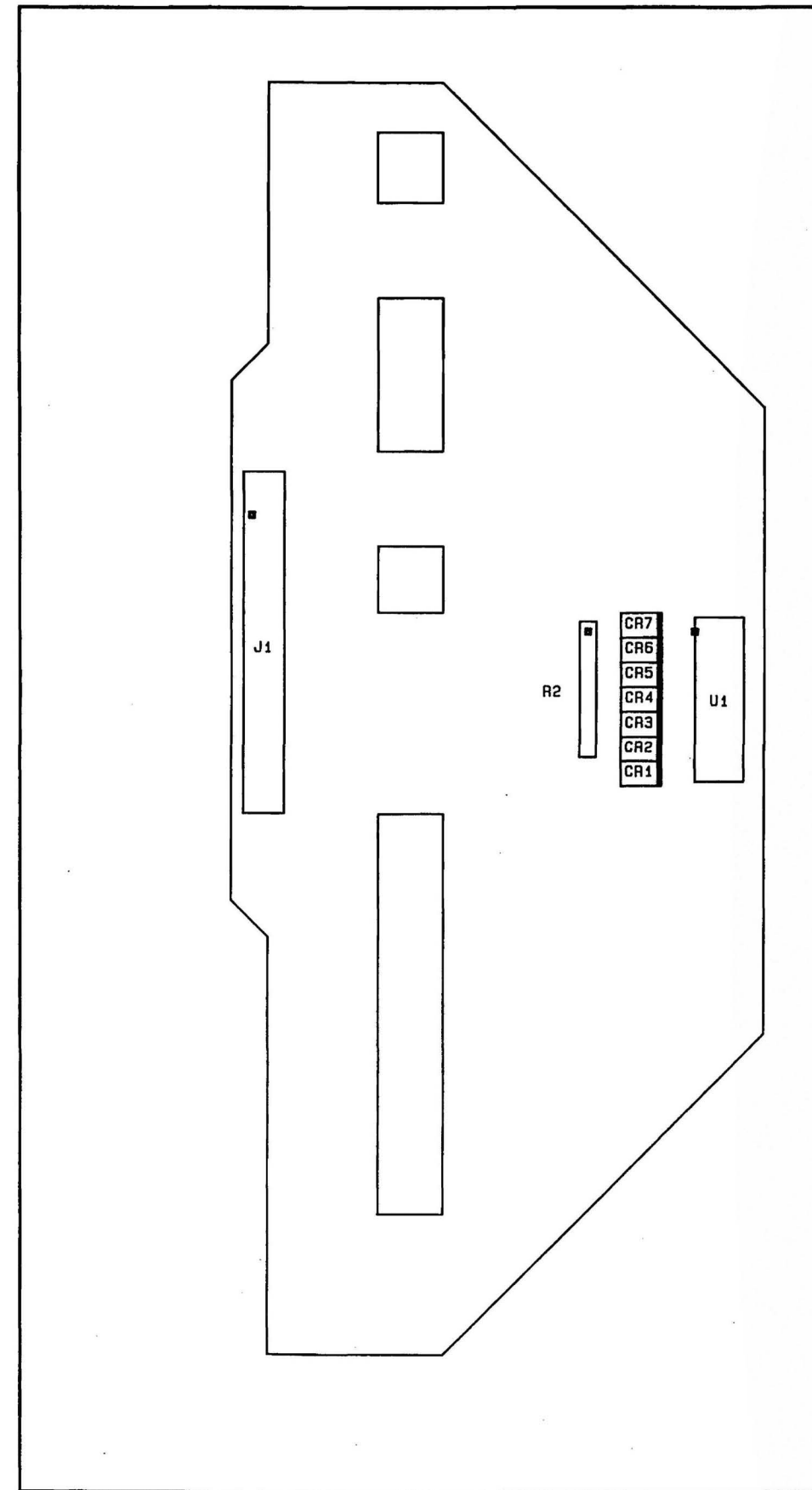
A16 Module

Troubleshooting and Adjustments

The A16 Attenuator Module is not field repairable due to the extreme complexity of generating new calibration data after a repair. If a failure occurs it must be replaced by a complete exchange module. The current part number for an exchange A16 Attenuator Module can be found in the parts list in section six of this manual set.

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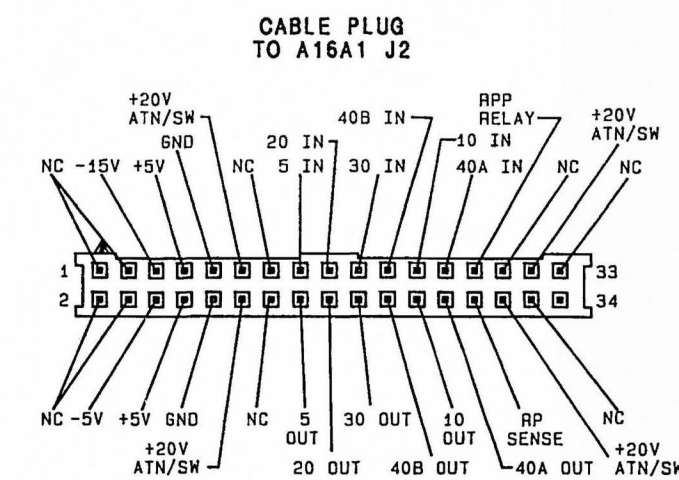
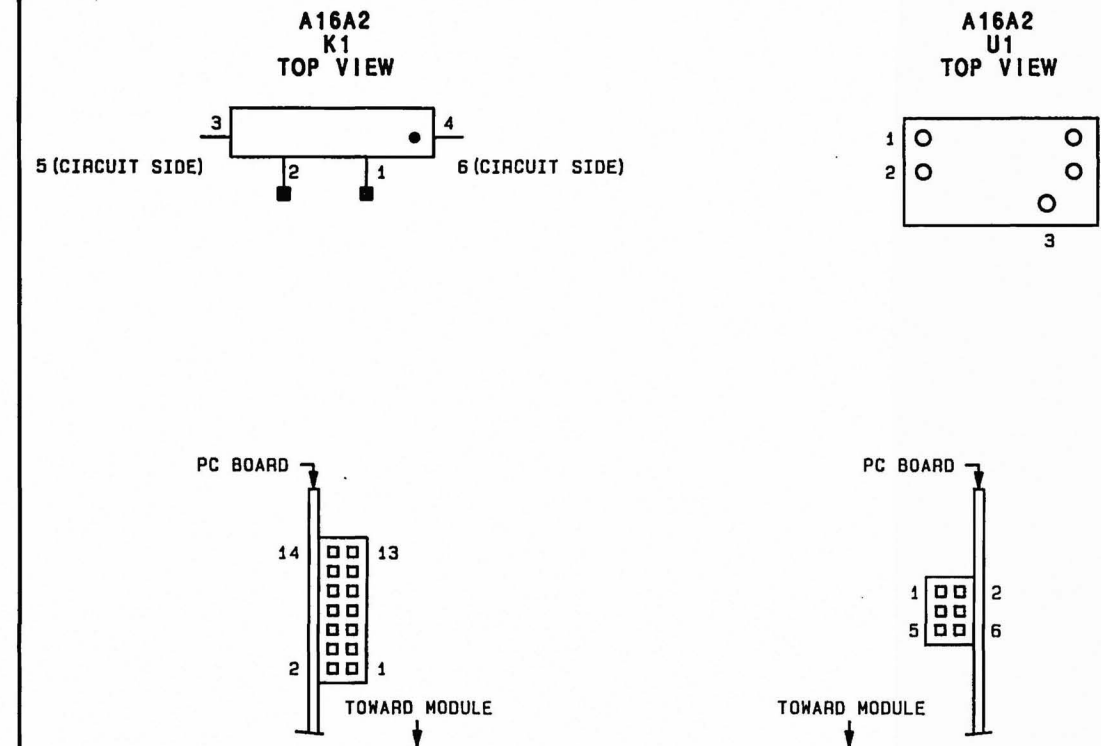
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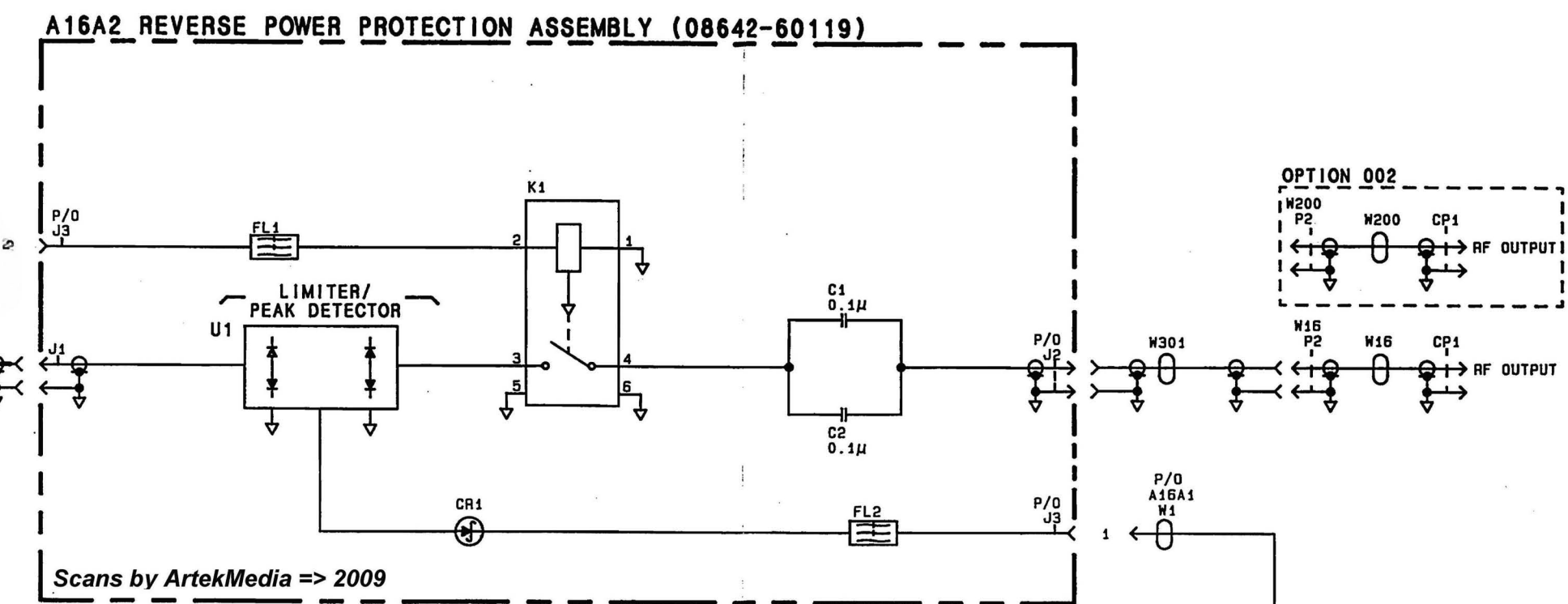
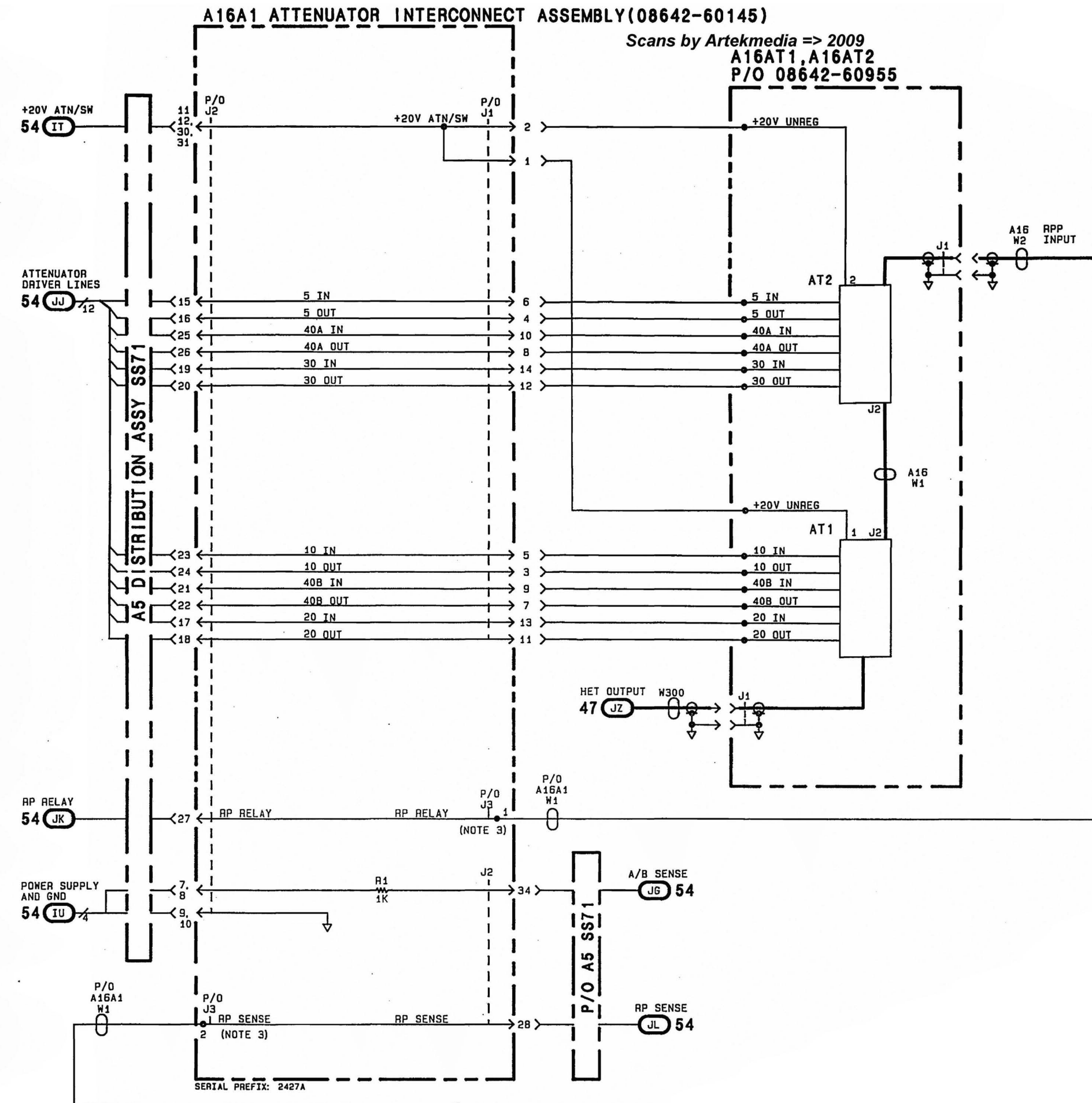
Component Locator

Notes: Scans by ArtekMedia => 2009

1. Each module in the HP 8542 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph B-3.
3. A16A1 W1 consists of two wires and connector soldered to two pads A16A1. (J3 pins 1,2)



Schematic General Information



CHANGES

All Serial Prefixes

On the component locator:

- Delete the entire component locator and replace with the component locator on page 8R-100.3.

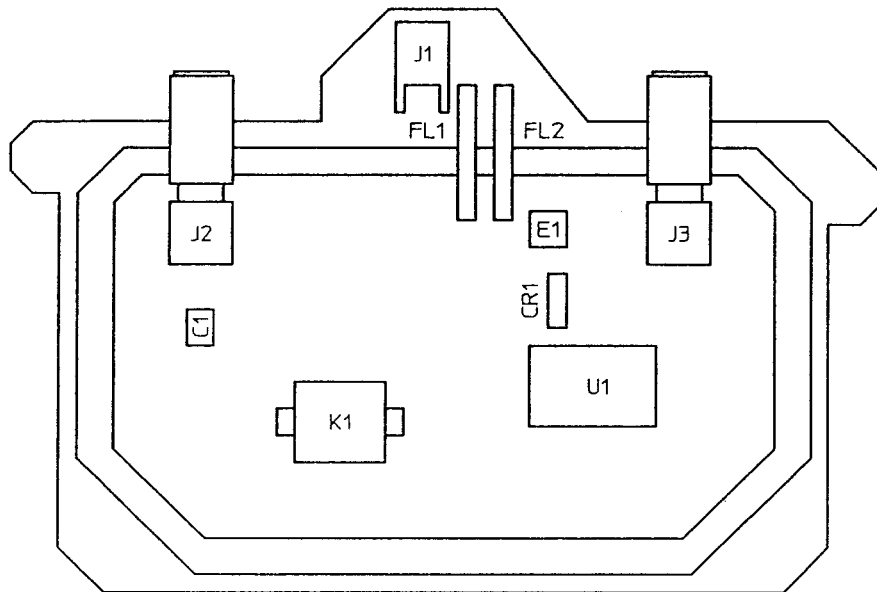
On the schematic:

- Mark the schematic "For Option 003 Only".

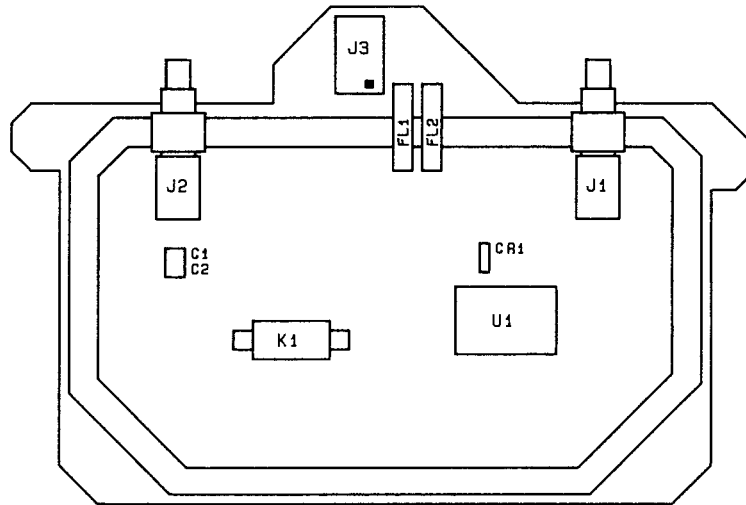
CHANGES

All serial prefixes	On the A16A2 schematic: <ul style="list-style-type: none">• <u>A16A2</u> - Mark the schematic "For Option 003 Only".
2850A and above	On the A16A2 schematic: <ul style="list-style-type: none">• <u>08642-60219</u> - Change the part number of the A16A2 REVERSE POWER PROTECTION ASSEMBLY to 08642-60219. On the A16A2 Component Locator: <ul style="list-style-type: none">• <u>08642-60219</u> - Use the new component locator on page 8R-100.3.

Reserved for future changes.



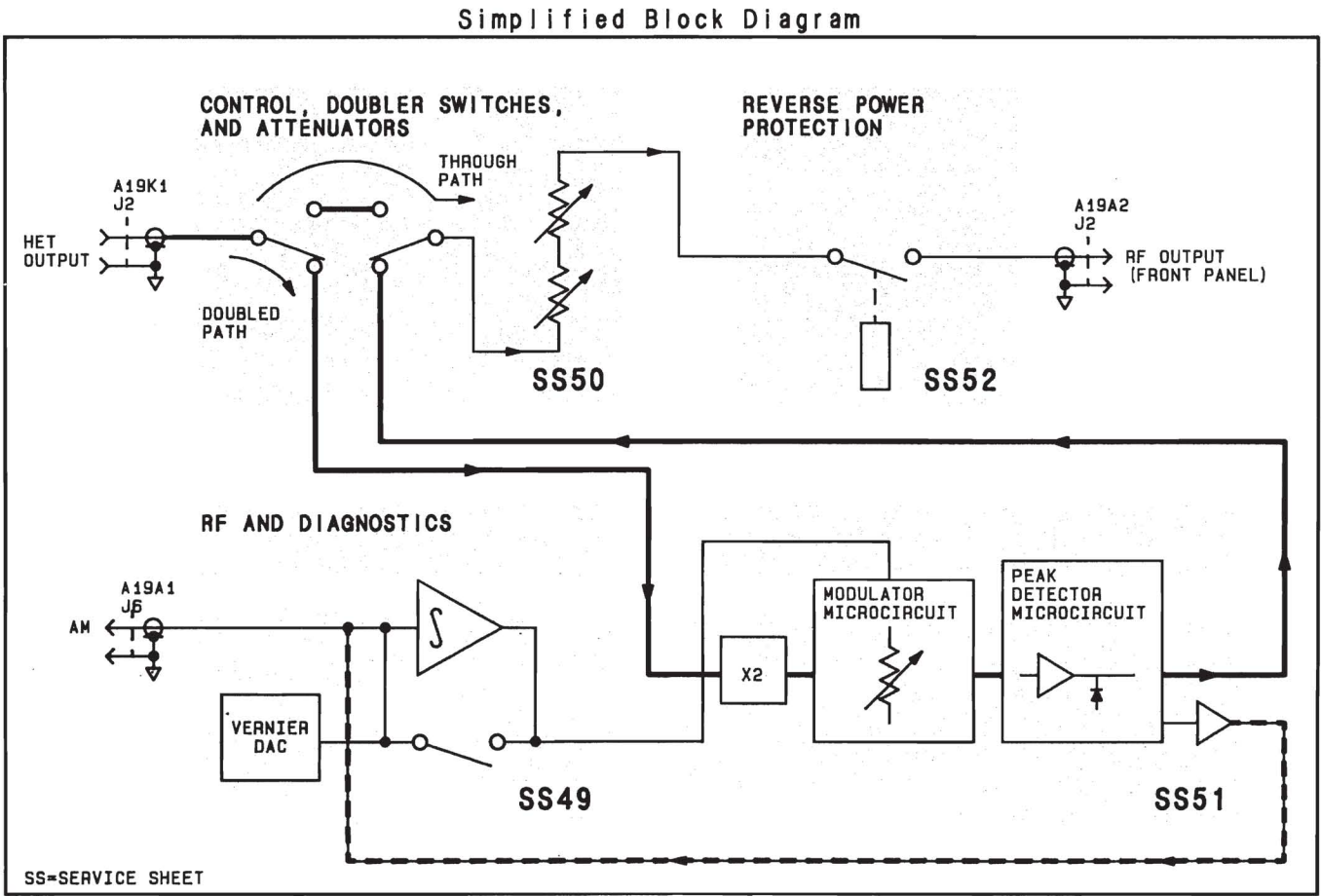
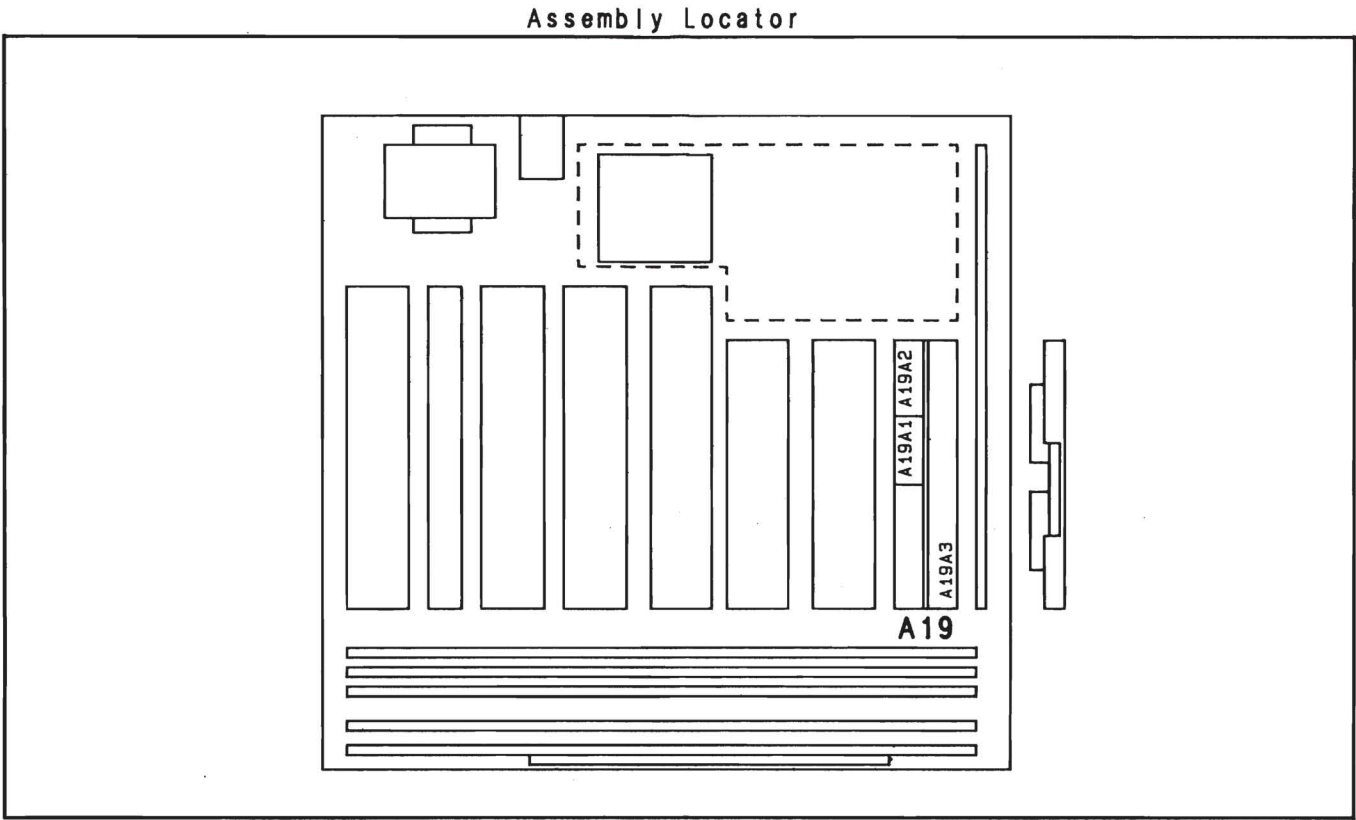
A16A2 Component Locator for the 08642-60219 board, (2850A and above)

**A16A2***A16A2 COMPONENT LOCATOR (P/O Errata)*

A19 Module

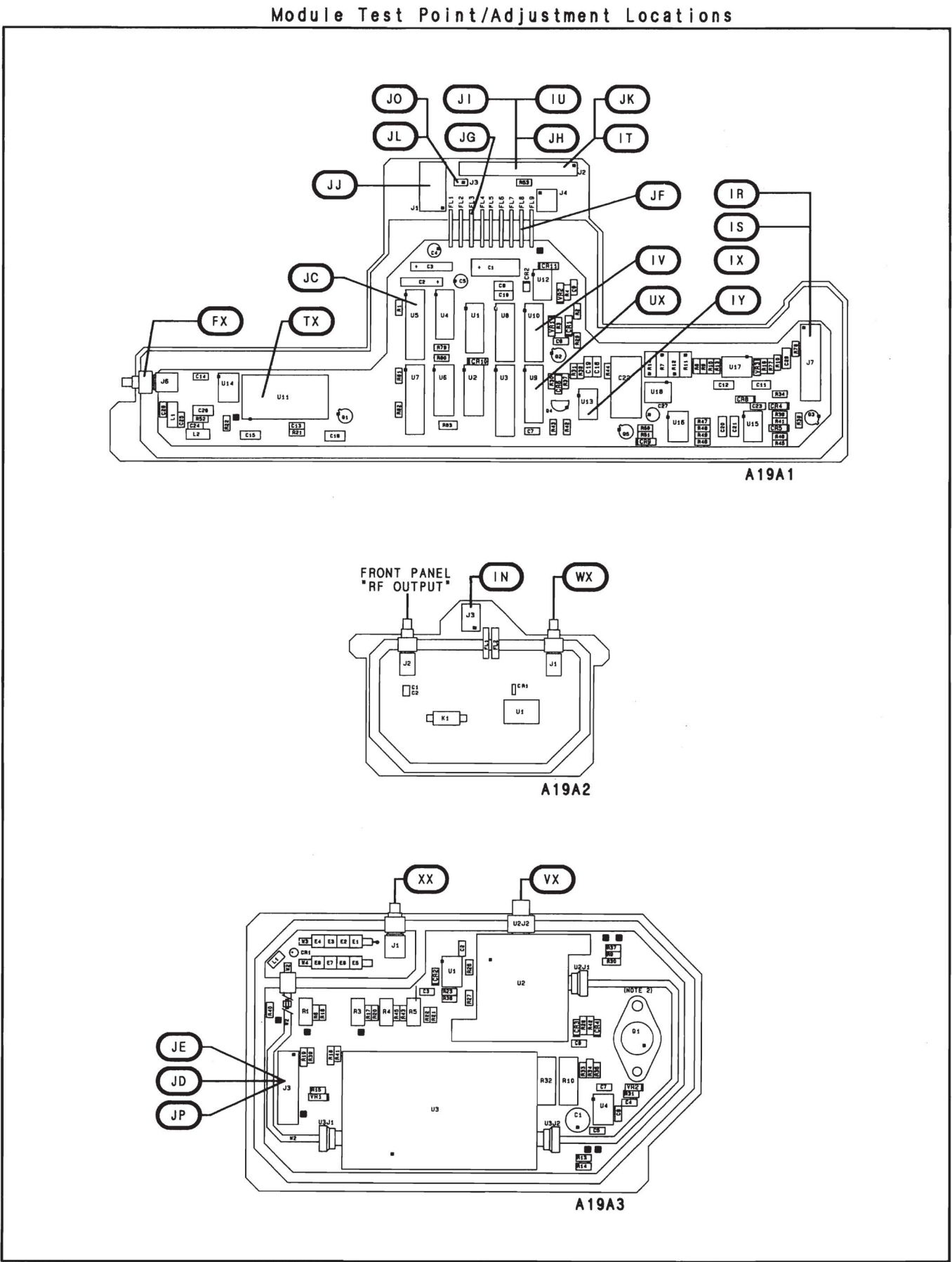
Troubleshooting and Adjustments

The A19 Doubler/Attenuator Module is not field repairable due to the extreme complexity of generating new calibration data after a repair. If a failure occurs it must be replaced by a complete exchange module. The current part number for an exchange A19 Doubler/Attenuator Module can be found in the parts list in section six of this manual set.



SS=SERVICE SHEET

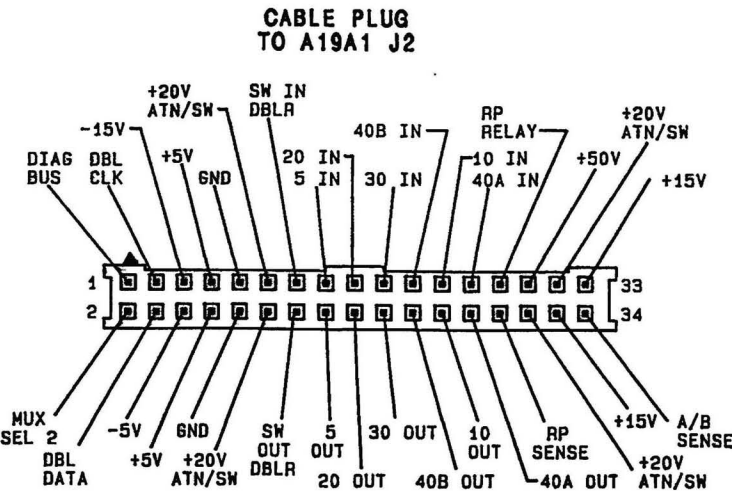
Figure 8S-100 BD16 General Information.



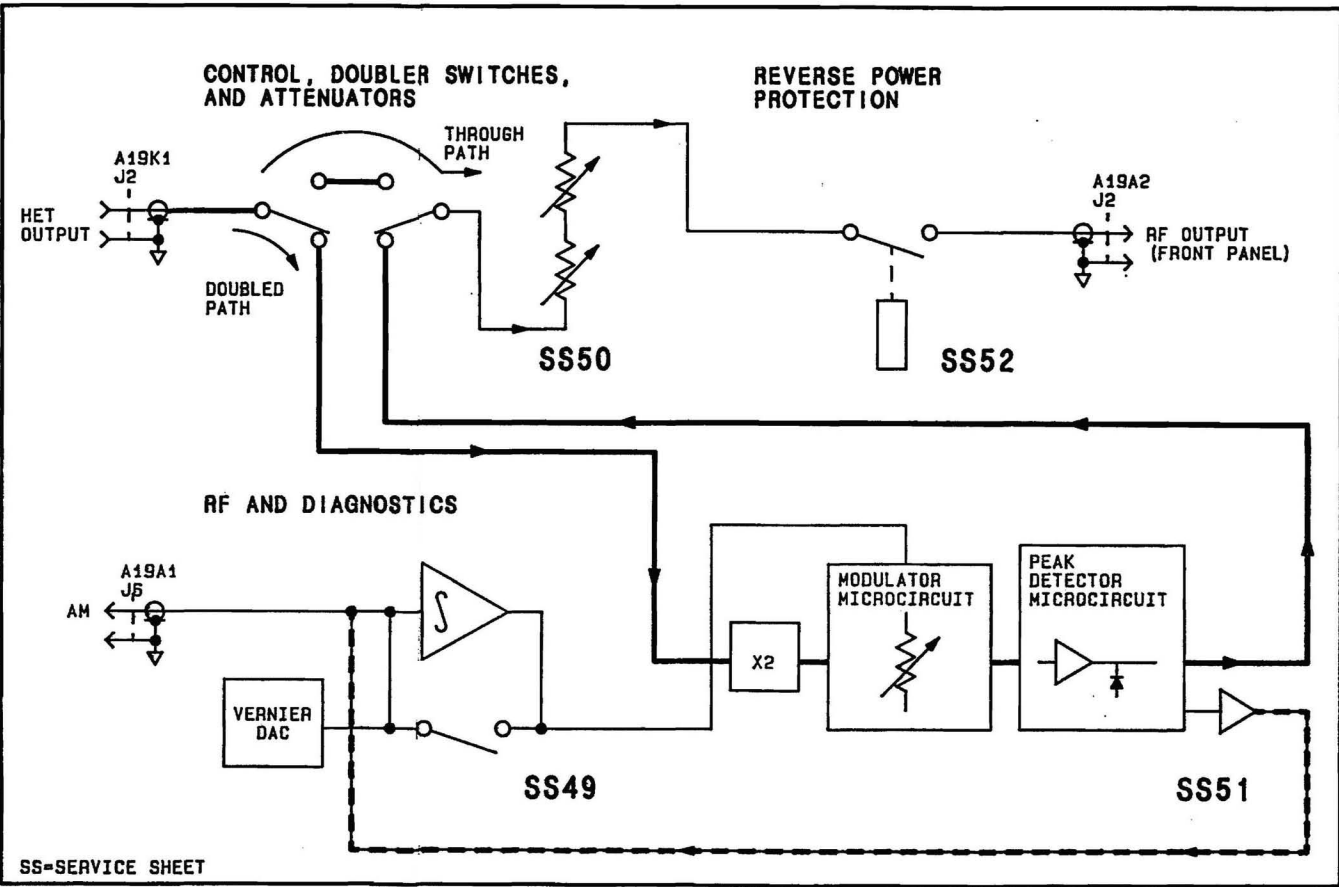
CHANGES

All serial prefixes	<p>In Module Test Point/ Adjustment Locations:</p> <ul style="list-style-type: none">• A19A2 - On the A19A2 illustration on page 8S-100, delete C2, change J3 to J1, J1 to J3, and, add E1 horizontally above and to the left of CR1. <p>On the Block Diagram:</p> <ul style="list-style-type: none">• Change the page number of the block diagram from 85-101 to 8S-101.• <u>J3 pin 28</u> - On the left hand side of the A19A1 block diagram, change J3 pin 28 to J3 pin 2.
---------------------	---

- Notes: Scans by Artekmedia => 2009
1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
 2. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
 3. A19 FL1 is an array of feedthrough filters passing through the center of the module to make connections between two (2) printed circuit boards.



Schematic General Information



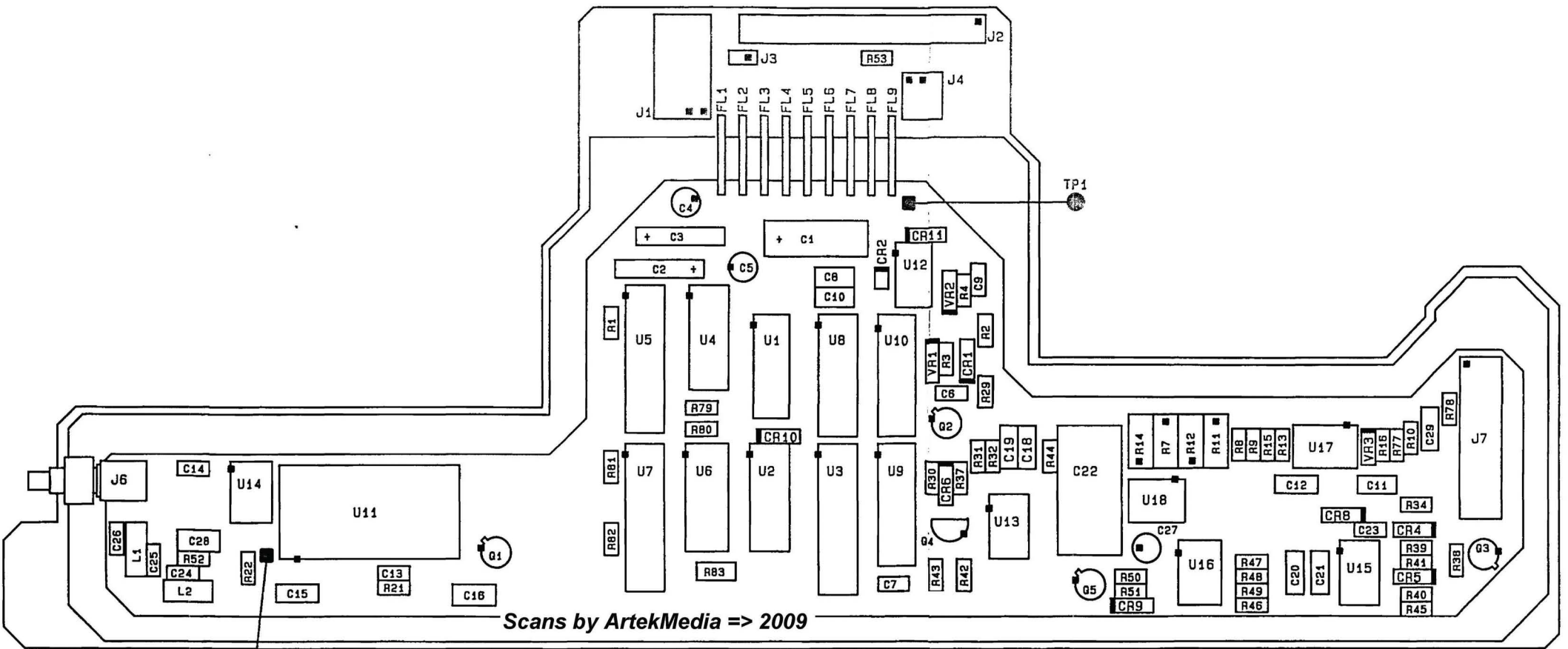
Reference Block Diagram

Component Coordinates

COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y	COMP	X, Y
C1	C, 2	CR1	D, 3	R11	D, 3	TP1	C, 1								
C2	B, 2	CR2	D, 3	R12	D, 3	TP2	A, 3								
C3	B, 2	CR3	D, 3	R13	D, 3										
C4	B, 1	CR4	D, 3	R14	C, 3										
C5	B, 2	CR5	D, 3	R15	C, 3	U9	C, 3								
C6	C, 2	CR6	D, 3	R16	D, 3	U10	C, 2								
C7	C, 2	CR7	D, 3	R17	D, 3	U11	A, 3								
C8	C, 2	CR8	D, 3	R18	B, 3	U12	C, 2								
C9	C, 2	CR9	D, 3	R19	A, 3	U13	C, 3								
C10	C, 2	CR10	D, 3	R20	C, 2	U14	A, 3								
C11	D, 3	CR11	D, 3	R21	C, 2	U15	D, 3								
C12	D, 3			R22	A, 3	U16	D, 3								
C13	D, 3			R23	C, 2	U17	D, 3								
C14	D, 3			R24	C, 3	U18	C, 3								
C15	A, 3			R25	D, 3	VR1	C, 2								
C16	B, 3			R26	D, 3	VR2	C, 2								
C17	C, 3			R27	D, 3	VR3	D, 3								
C18	C, 3			R28	D, 3										
C19	C, 3			R29	D, 3										
C20	D, 3			R30	D, 3										
C21	D, 3			R31	D, 3										
C22	C, 3			R32	C, 3										
C23	D, 3			R33	C, 3										
C24	D, 3			R34	D, 3										
C25	A, 3			R35	D, 3										
C26	A, 3			R36	D, 3										
C27	C, 3			R37	D, 3										
C28	A, 3			R38	D, 3										
C29	D, 2			R39	D, 3										
				R40	D, 3										
				R41	D, 3										
				R42	C, 3										
				R43	C, 3										
				R44	C, 3										
				R45	D, 3										
				R46	D, 3										
				R47	D, 3										
				R48	D, 3										
				R49	D, 3										
				R50	C, 3										
				R51	C, 3										
				R52	A, 3										
				R53	A, 3										
				R54	C, 3										
				R55	D, 3										
				R56	D, 3										
				R57	D, 3										
				R58	D, 3										
				R59	D, 3										
				R60	D, 3										
				R61	D, 3										
				R62	D, 3										
				R63	D, 3										

A19A1 MODULE **BD 16**

SEE REVERSE SIDE



CHANGES

All Serial Prefixes

On the schematic:

- R45 - In INTEGRATOR, change R45 value to 990 ohms.

2517A and above

On the Component Locator:

- C6, R43 - Replace U18 with the following two component moves: Move C6 to the immediate right of C22. Move R43 to the right of C22, underneath C6.

In Component Coordinates:

- C6 - Change C6 coordinates to C,3.

On the schematic:

- A19A1 - In the upper left portion of the schematic, change the A19A1 part number to 08642-60218.
- A19A1 R30, Q1, U18, C16 - Replace the appropriate portion of SS49 with the schematic partial on page 8S-102.2, P/O FIGURE 8S-103 (2517A and above).

2640A and above

On the schematic:

- Replace the entire schematic diagram with the revised schematic on page 8S-102.3.

CHANGES**All Serial Prefixes**

On the schematic:

- R45 - In INTEGRATOR, change R45 value to 990 ohms.

2517A and above

On the Component Locator:

- C6, R43 - Replace U18 with the following two component moves: Move C6 to the immediate right of C22. Move R43 to the right of C22, underneath C6.

In Component Coordinates:

- C6 - Change C6 coordinates to C,3.

On the schematic:

- A19A1 - In the upper left portion of the schematic, change the A19A1 part number to 08642-60218.
- A19A1 R30, Q1, U18, C16 - Replace the appropriate portion of SS49 with the schematic partial on page 8S-102.2, P/O FIGURE 8S-103 (2517A and above).

2640A and above

On the schematic:

- Replace the entire schematic diagram with the revised schematic on page 8S-102.3.

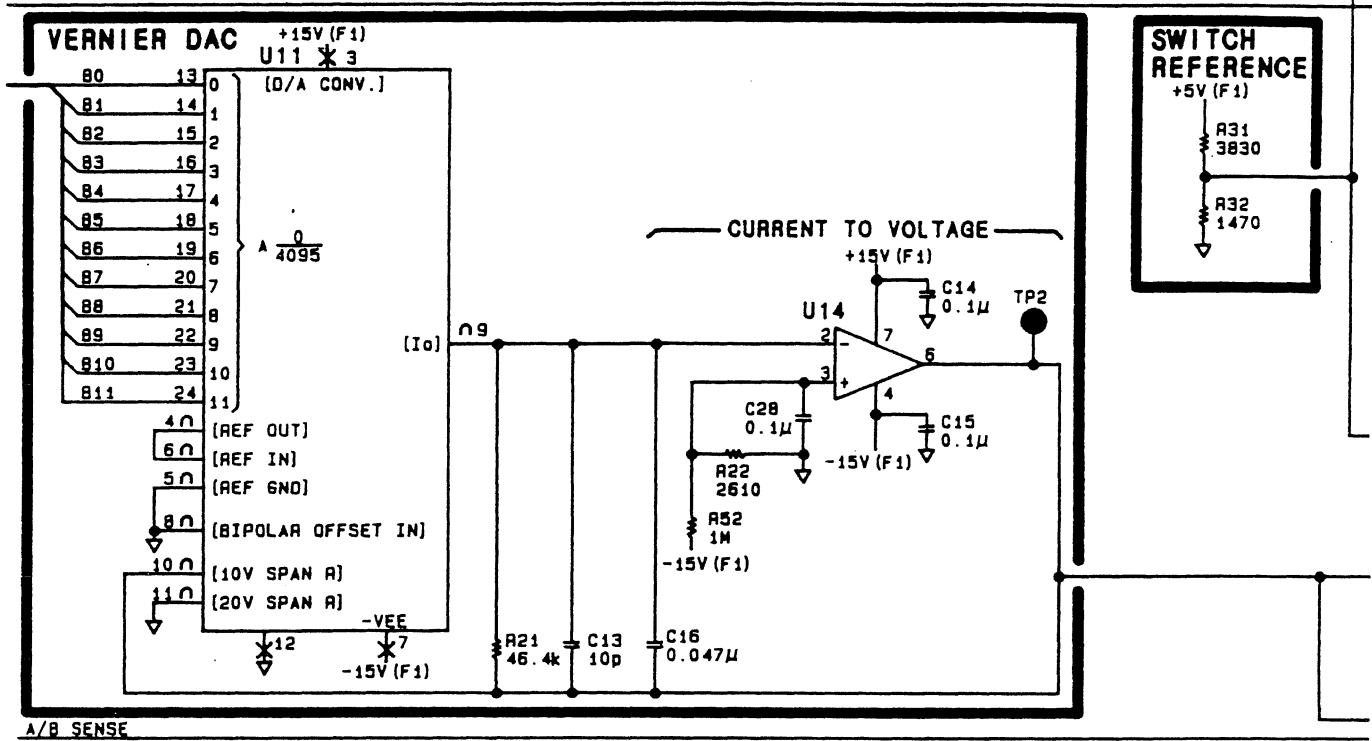
2721A and above

On the schematic:

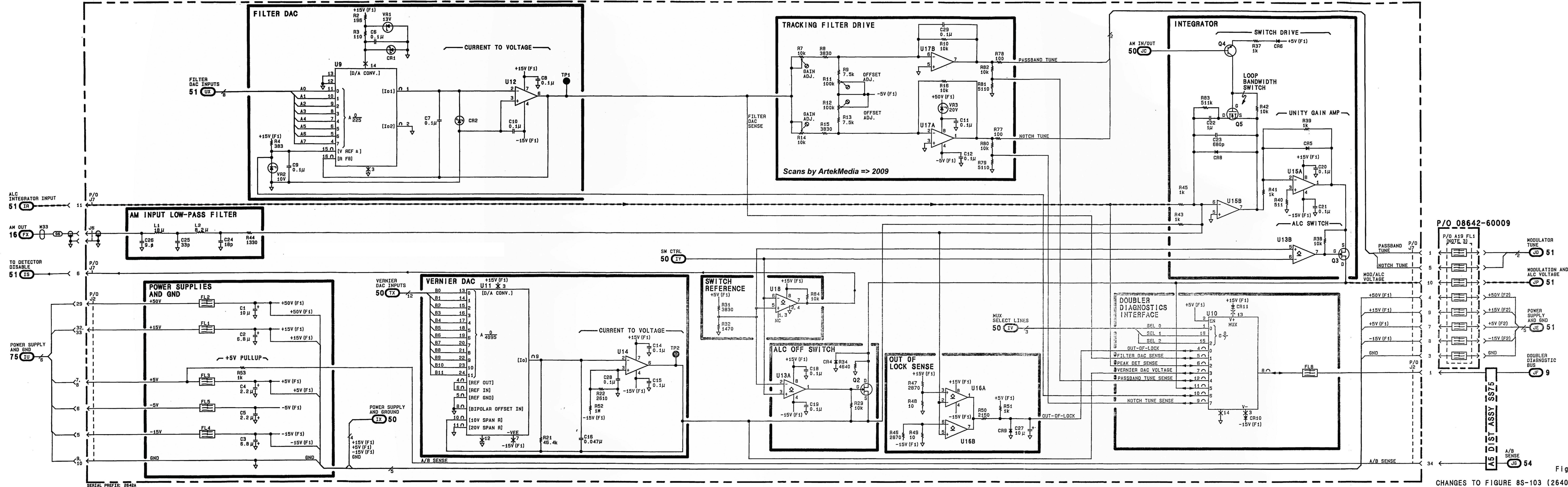
- R7, R14 - In TRACKING FILTER DRIVE, change R7 and R14 to 20K pots.

SM CTRL

50 IY

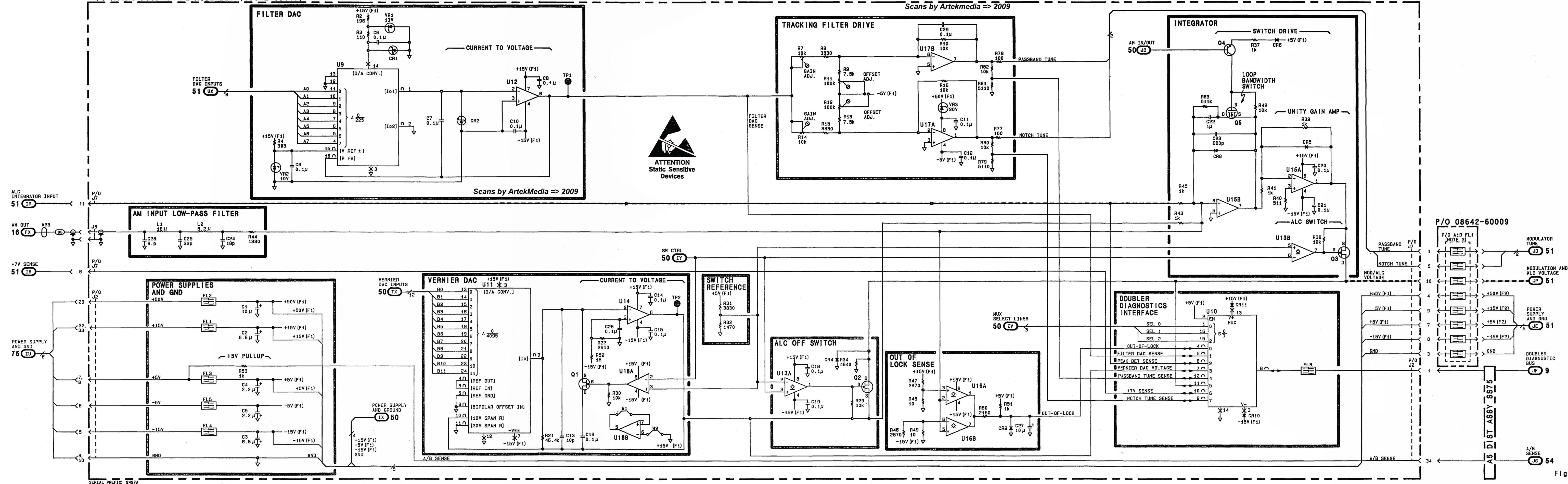


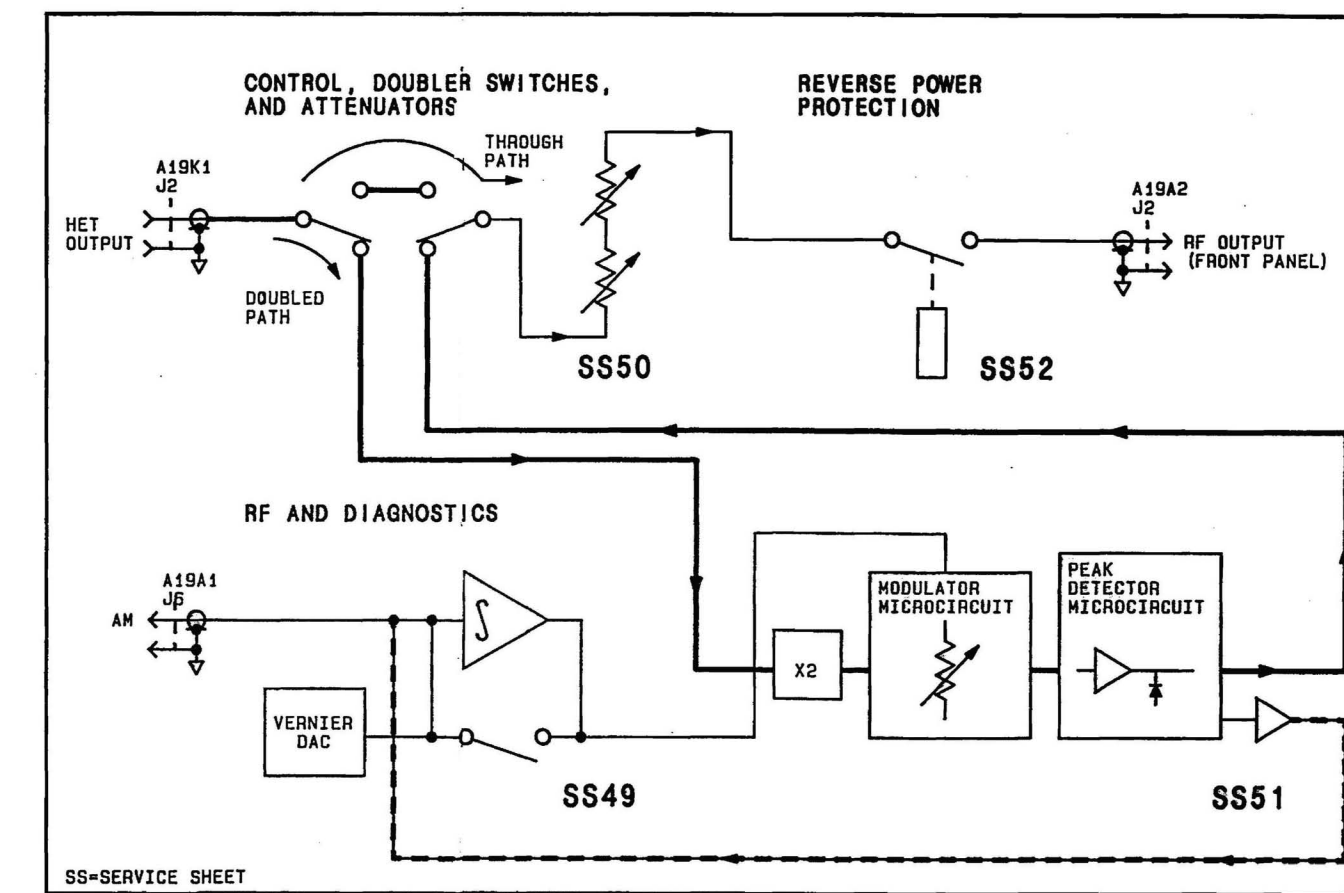
P/O FIGURE 8S-103 (2517A and above)



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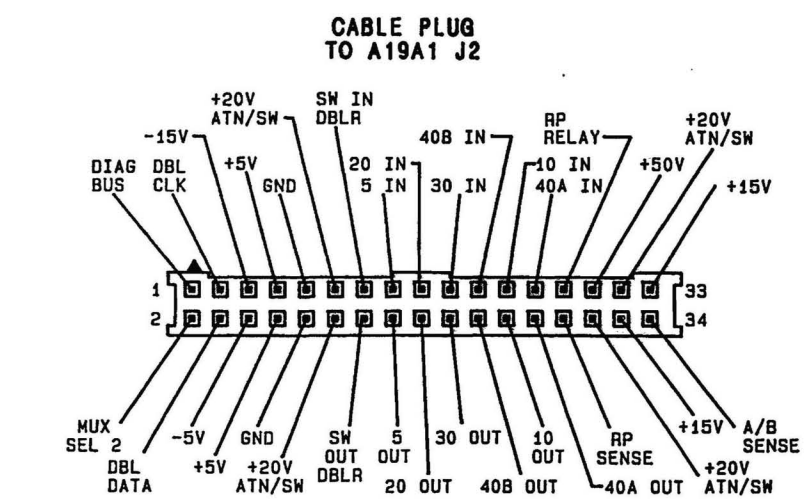




Component Locator

SEE REVERSE SIDE P/O DOUBLER #2 SS49
A19A1 ASSEMBLY

1. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
2. A19A1 W9 consists of two wires and a connector soldered to two pads on A19A1. (J3 pins 1,2)
3. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.



8S-104

CHANGES

All Serial Prefixes

In Schematic General Information:

- A19A1 W3 - In Note 2, change A19A1 W9 to A19A1 W3.

On the schematic:

- A19A1 W3 - On the left side of the schematic, it should be noted that A19A1 W3, RP SENSE, does not go through A5 (DISTRIBUTION ASSY).

2517A and above

On the Component Locator:

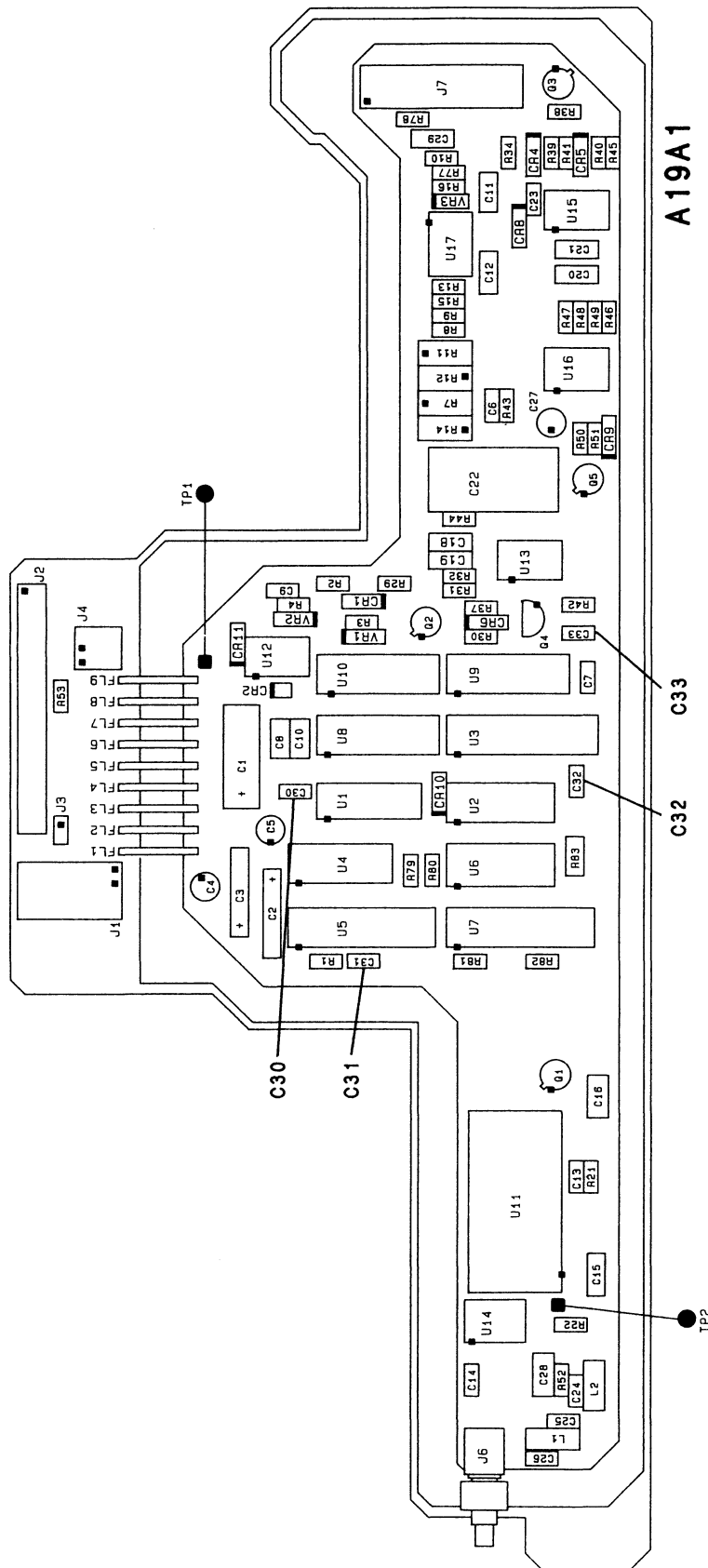
- A19A1 C30, C31, C32, C33 - Note changes to component locator as shown on page 8S-104.2.

In Component Coordinates:

- A19A1 C30, C31, C32, C33 - Add components and grid coordinates as follows:
C30 C,2
C31 B,2
C32 C,3
C33 C,3

On the schematic:

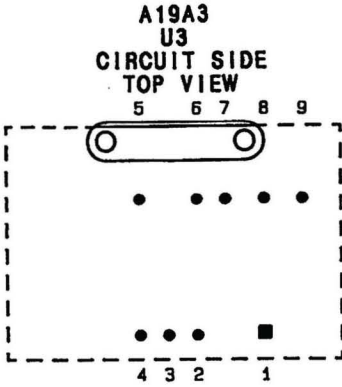
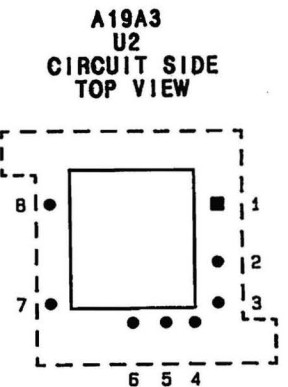
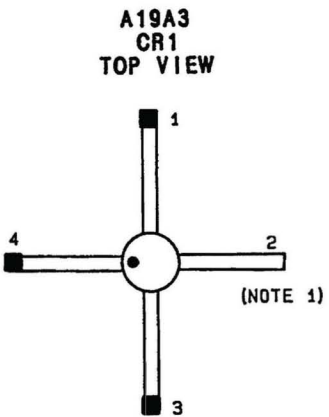
- A19A1 - In the upper left portion of the schematic, change the part number for A19A1 to 08642-60218.
- A19A1 C30, C31, C32, C33 - In **POWER SUPPLY AND GND**, add C30-C33 to the +5V(F1) line, going to ground.



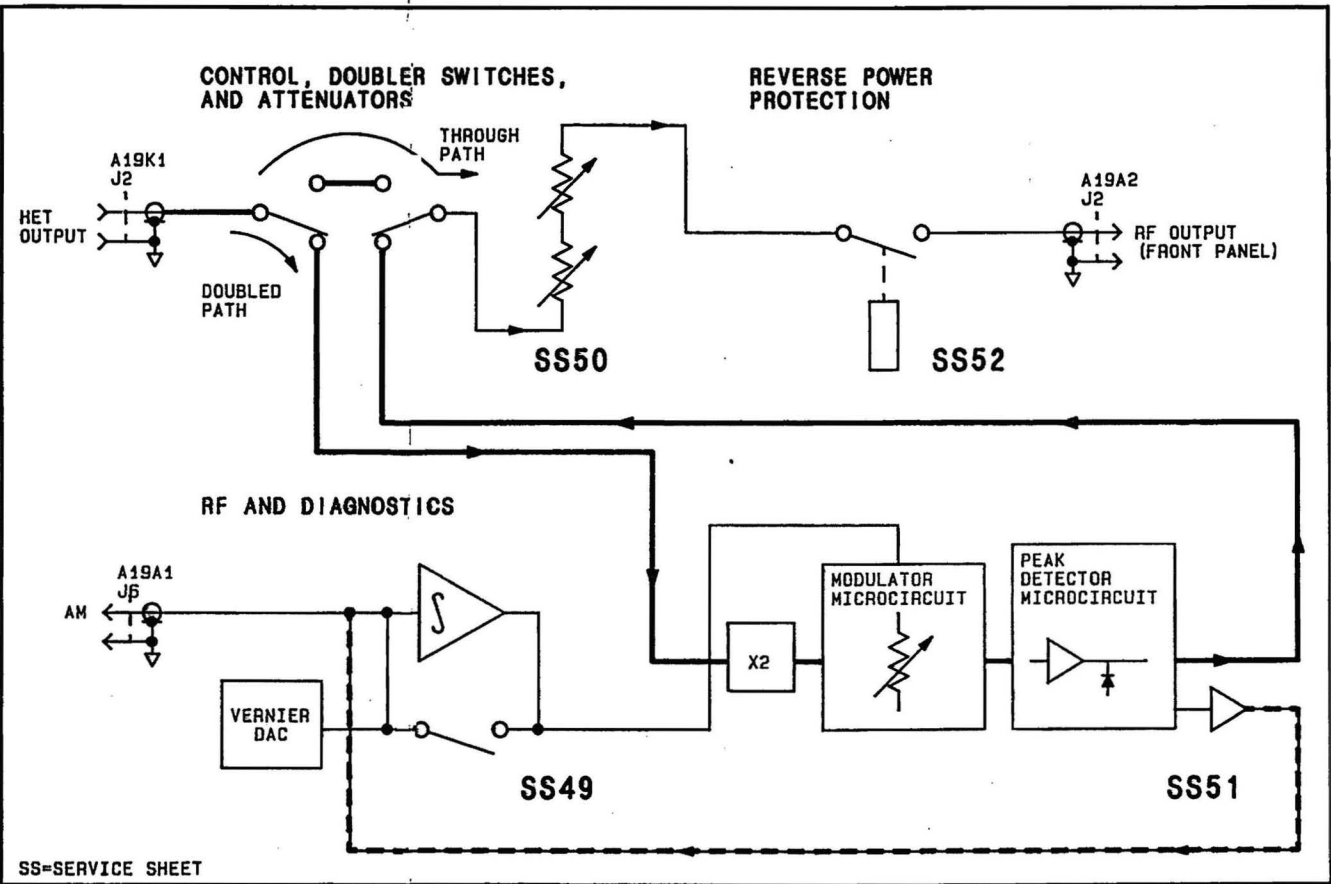
P/O FIGURE 8S-102 (2517A and above)

Notes: Scans by ArtekMedia => 2009

- 1. Do not touch CR1 with soldering iron. Heat pad only.
- 2. Q1 mounts to heatsink.
- 3. Each module in the HP 8642 has a nine digit module identification code. The first four digits comprise the module configuration code. When servicing a module, note any changes that apply specifically to its module configuration code.
- 4. All circuit boards are manufactured using a hot air leveled process. These boards require extra care when replacing components. Refer to General Service Information, paragraph 8-3.
- 5. A19 FL1 is an array of feed through filters passing through the center of the module to make connections between two (2) printed circuit boards.



Schematic General Information



Reference Block Diagram

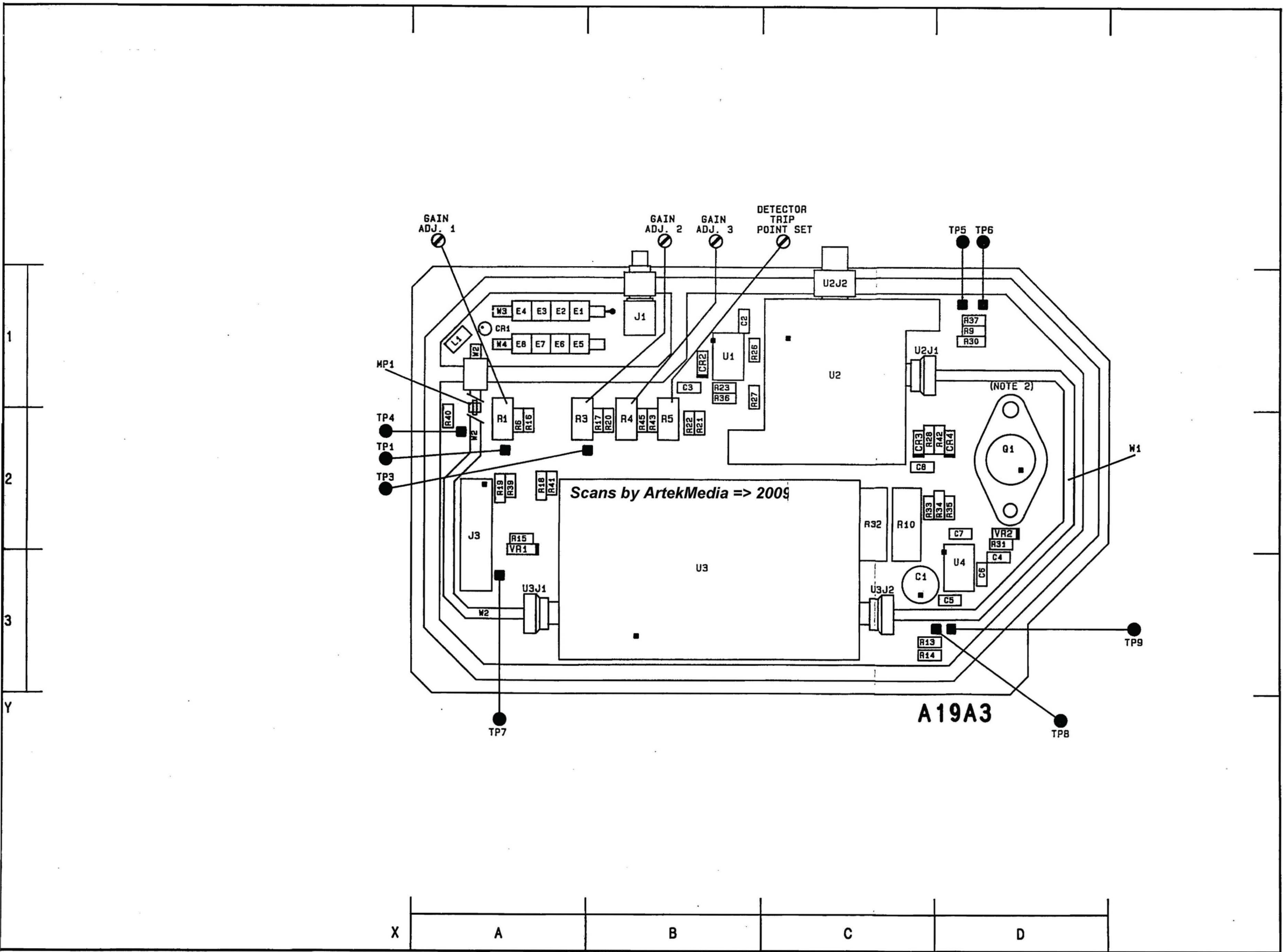
Component Coordinates

COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y	COMP	X,Y
C1	C, 3	R6	A, 2	TP7	A, 3												
C2	B, 1	R9	D, 1	TP8	D, 3												
C3	B, 1	R10	C, 2	TP9	D, 3												
C4	D, 3	R13	C, 3														
C5	D, 3	R14	C, 3	U1	B, 1												
C6	D, 3	R15	A, 3	U2	C, 1												
C7	D, 2	R16	A, 2	U3	B, 3												
C8	C, 2	R17	B, 2	U4	D, 3												
		R18	A, 2														
CR1	A, 1	R19	A, 2	VR1	A, 2												
CR2	B, 1	R20	B, 2	VR2	D, 2												
CR3	C, 2	R21	B, 2														
CR4	D, 2	R22	B, 2														
		R23	B, 1														
E1	A, 1	R26	B, 1														
E2	A, 1	R27	B, 1														
E3	A, 1	R28	C, 2														
E4	A, 1	R30	D, 1														
E5	A, 1	R31	D, 2														
E6	A, 1	R32	C, 2														
E7	A, 1	R33	C, 2														
E8	A, 1	R34	D, 2														
		R35	D, 2														
J1	B, 1	R36	B, 1														
J3	A, 2	R37	D, 1														
		R39	A, 2														
L1	A, 1	R40	A, 2														
		R41	A, 2														
MP1	A, 1	R42	D, 2														
		R43	B, 2														
Q1	D, 2	R45	B, 2														
R1	A, 2	TP1	A, 2														
R2	A, 2	TP3	A, 2														
R4	B, 2	TP4	A, 2														
R5	B, 2	TP5	D, 1														
		TP6	D, 1														

P/O DOUBLER #2
A19A1 ASSEMBLY SS50

SEE REVERSE SIDE

Component Locator



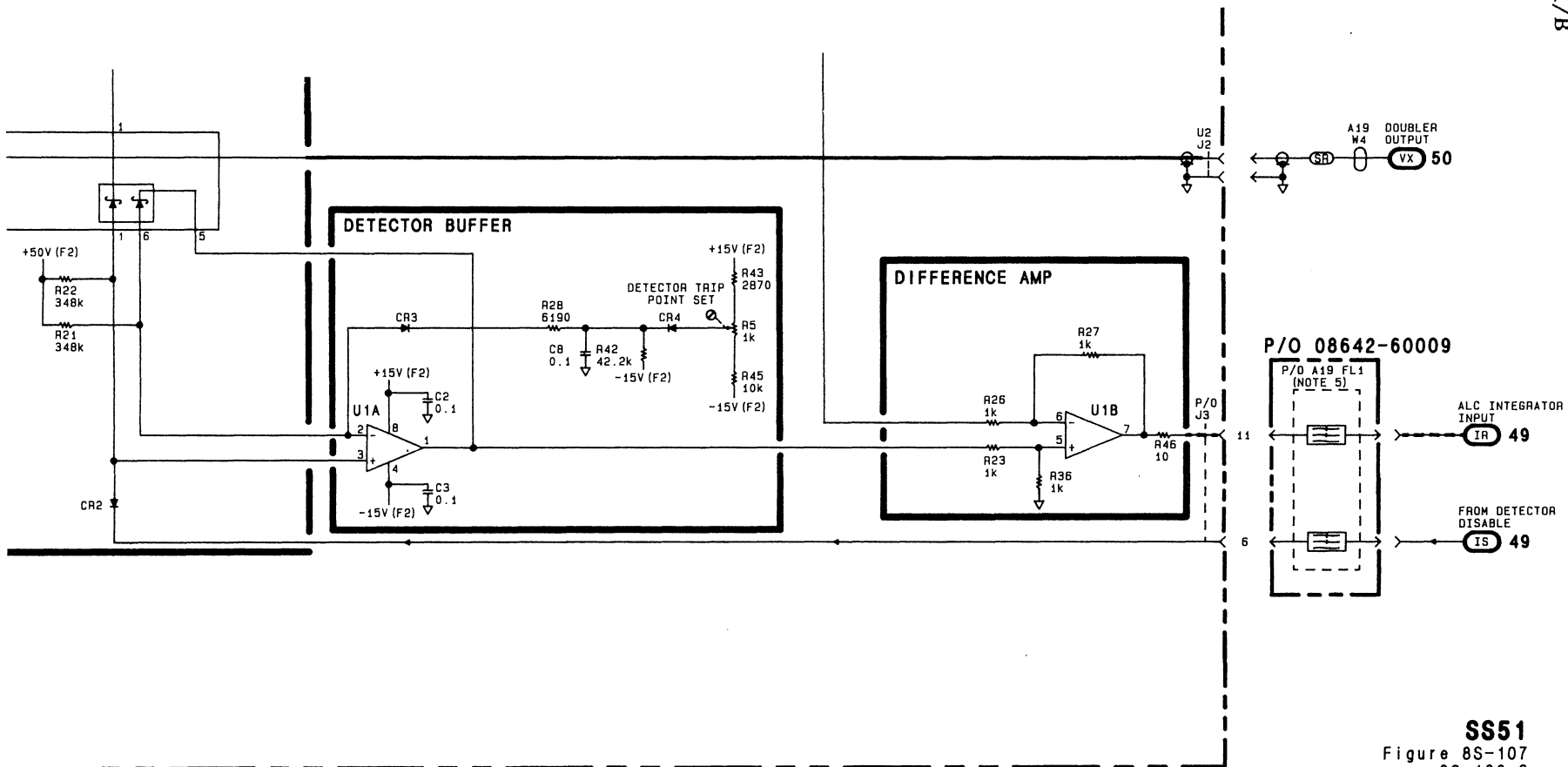
CHANGES

<p>All serial prefixes</p>	<p>On the Component Locator:</p> <ul style="list-style-type: none"> • <u>R46</u> - Add R46 immediately below R5. • <u>L2</u> - Add L2 immediately below J1 <p>In Component Coordinates:</p> <ul style="list-style-type: none"> • <u>R46</u> - Add R46 (B,2). • <u>L2</u> - Add L2, (B,1). <p>On the A19A3 schematic:</p> <ul style="list-style-type: none"> • In the upper left portion of the schematic, change the A19A3 assembly number to 08642-60220. • <u>R46</u> - In DIFFERENCE AMP, add R46 between pin 7 of U1 and pin 11 of J3, assign it a value of 10 ohms.
<p>2640A and above</p>	<p>On the A19A3 schematic:</p> <ul style="list-style-type: none"> • In the upper left portion of the schematic, change the A19A3 assembly number to 08642-60320. • Use the schematic partial with the schematic on page 8P-106.3.
<p>2640A to 2834A</p>	<p><u>L2</u> - In DOUBLER, change the value of L2 to 180NH.</p> <p>On the A19A3 schematic:</p> <ul style="list-style-type: none"> • <u>L1</u> - In DOUBLER, change the value of L1 to 82NH.
<p>2735A and above</p>	<p>On the A19A3 schematic:</p> <ul style="list-style-type: none"> • R1 - In the center left of the SS51 schematic locate MODULATOR MICROCIRCUIT and change the value of R1 to 10k.
<p>2835A and above</p>	<p>On the A19A3 schematic:</p> <ul style="list-style-type: none"> • <u>L1</u> - In DOUBLER locate L1 and change it's value to 100NH.

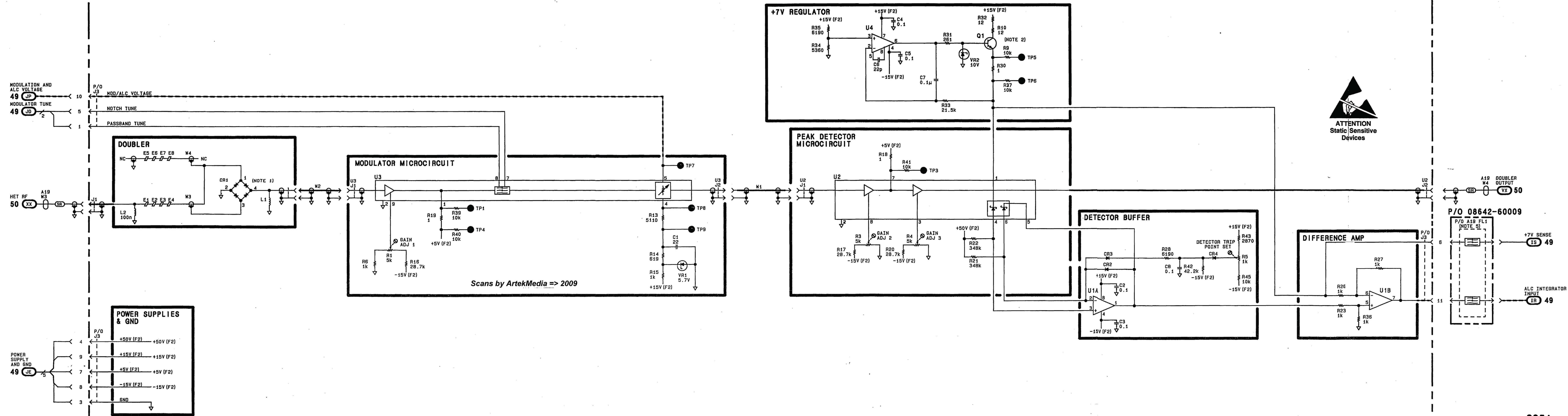
rev.11AUG86

CHANGES TO FIGURE 8S-107 (2640A AND ABOVE)

SS51
8S-106.3

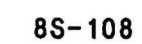


SS51
Figure 8S-107
8S-106.3





SEE REVERSE SIDE



CHANGES

All Serial Prefixes

On the Component Locator:

- Above K1, add "NOTE 3."

In Schematic General Information:

- Add "NOTE 3"; Small gold disc(s) are tunable stubs, positioned on the circuit board for optimum SWR characteristics. There may be more than 1 tunable stub, and the positioning may vary on the RF path from J1 to C1.

On the schematic:

- Add Z1, a tunable stub, from the circuit main signal path (U1 Pin 5) to ground. Add "NOTE 3" to the nearest available space.
- C2 - In REVERSE POWER PROTECTION ASSEMBLY, remove C2.

2640A and Above

On the schematic:

- A19A2 - In REVERSE POWER PROTECTION ASSEMBLY, add C4, 0.1 u, in parallel with C1.

On the Component Locator:

- A19A2 - Add C4 directly below C1.

In Component Coordinates:

- A19A2 - Add C4, A, 2.

CHANGES

<p>All serial prefixes</p>	<p>On the A19A2 schematic:</p> <ul style="list-style-type: none"> • C1 - In REVERSE POWER PROTECTION ASSEMBLY, change the value of C1 to .22uF. • C2 - In REVERSE POWER PROTECTION ASSEMBLY, remove C2. • Z1, NOTE 3 - Add Z1, a tunable stub, from the circuit main signal path (U1 Pin 5) to ground. Add "NOTE 3" to the nearest available space. <p>On the Component Locator:</p> <ul style="list-style-type: none"> • C2 - Delete C2. • NOTE 3 - Above K1, add "NOTE 3". <p>On the Component Coordinates:</p> <ul style="list-style-type: none"> • C2 - Delete C2 from the coordinates table. <p>In Schematic General Information:</p> <ul style="list-style-type: none"> • NOTE 3 - Add "NOTE 3" : Small gold disc(s) are tunable stubs, positioned on the circuit board for optimum SWR characteristics. There may be more than 1 tunable stub, and the positioning may vary on the RF path from J1 to C1.
<p>2640A only</p>	<p>On the A19A2 schematic:</p> <ul style="list-style-type: none"> • C4 - In REVERSE POWER PROTECTION ASSEMBLY, add C4, 0.1uF in parallel with C1. <p>On the A19A2 Component Locator:</p> <ul style="list-style-type: none"> • C4 - Add C4 directly below C1. <p>On the A19A2 Component Coordinates:</p> <ul style="list-style-type: none"> • C4 - Add C4, (A,2).
<p>2917A and above</p>	<p>On the A19A2 schematic:</p> <ul style="list-style-type: none"> • 08642-60219 - Change the part number of the A19A2 REVERSE POWER PROTECTION ASSEMBLY to 08642-60219. <p>On the A19A2 Component Locator:</p> <ul style="list-style-type: none"> • 08642-60219 - Use the new component locator on page 8S-108.3.

Reserved for future changes.

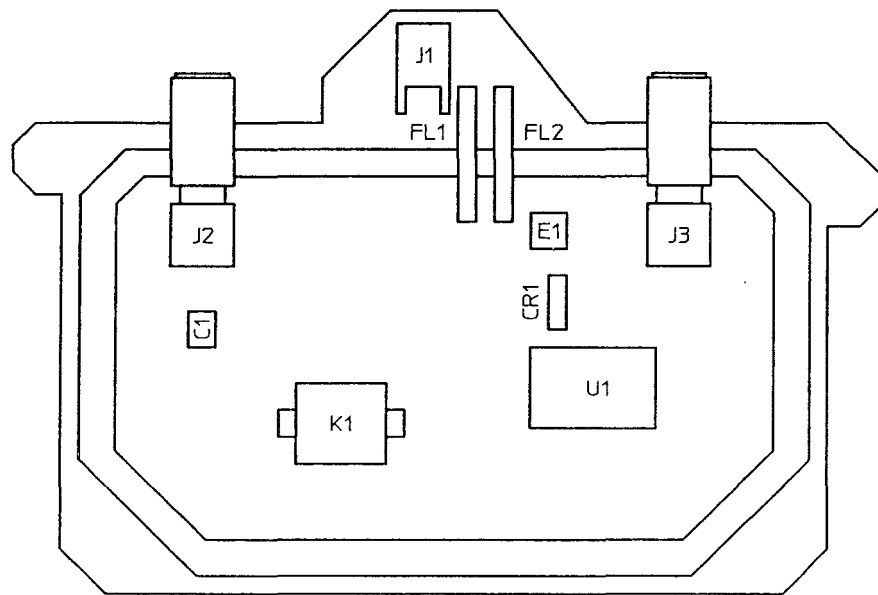
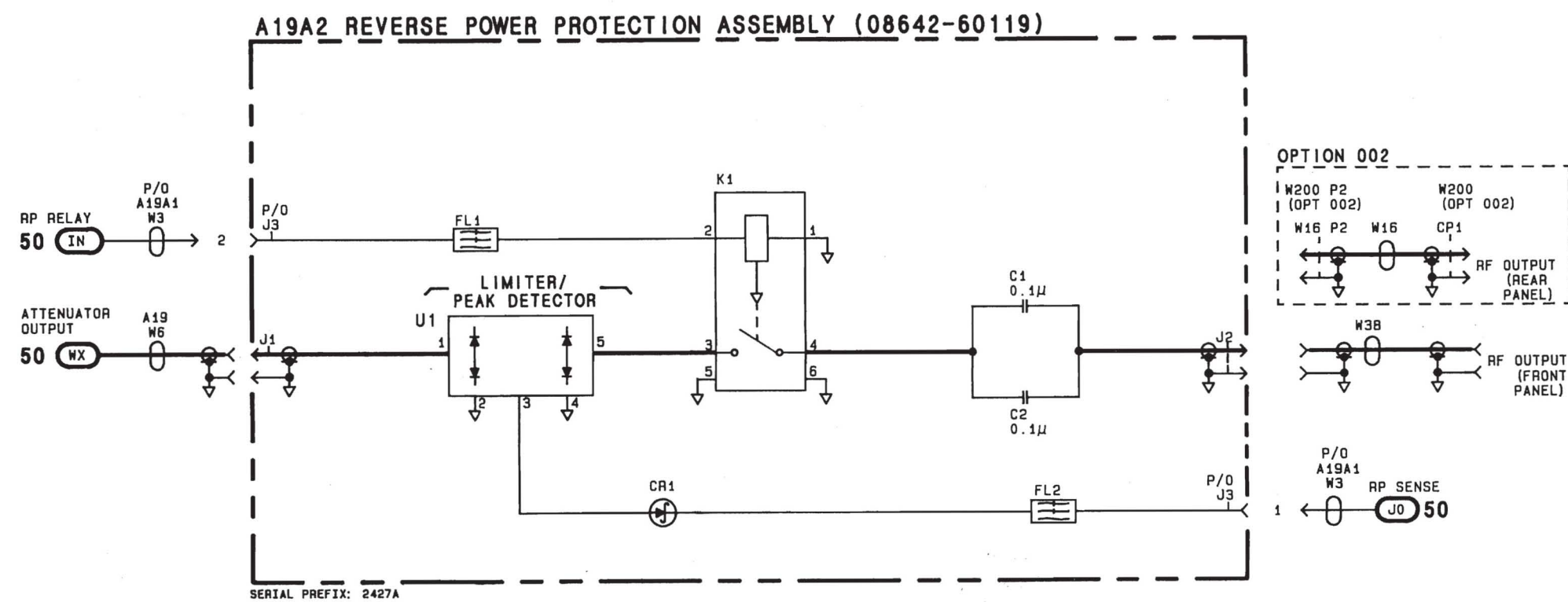


Figure 8S-108. Component Locator for the 08642-60219 board, (2917A and above)



SS52
Figure 85-109
85-109

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A17 and A18 Modules

Troubleshooting and Adjustment Contents

Details of Circuit Operation SS53 and SS54

Overall Description	8T-2
Detailed Description	8T-2
Power Transformer SS53	8T-2
A18 Circuits SS53	8T-2
A17 Circuits SS53	8T-3
+15 Volt Supply SS53	8T-3
+5.2 Volt Supply SS53	8T-4
+50 Volt Supply SS53	8T-4
Negative Supplies SS53	8T-4
Attenuator Driver SS54	8T-4

Troubleshooting Hints for the A17 Power Supply Regulators

+15 Volt Regulator	8T-7
-15 Volt Regulator	8T-8
+5.2 Volt Regulator	8T-9
-5.2 Volt Regulator	8T-10
+50 Volt Regulator	8T-11

Troubleshooting Hints for the A18 Power Supply Rectifier- Filter Board

Unregulated Power Supplies	8T-12
Voltages at Fuse Outputs	8T-12

Adjustments

Adjustment Procedure	8T-13
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Overall Description (BD17)

The HP 8642 requires five regulated power supplies for internal circuit operation. These are +50, +15, +5.2, -5.2 and -15 Volt supplies. The line transformer has primaries selectable for 100, 120, 220 and 240 Volt operation. It also has secondary taps for the various supplies. The +15, +5.2, -5.2 and -15 Volt unregulated supplies are obtained by full wave center-tapped rectification. The +50 Volt unregulated supply is a full-wave bridge configuration. The + and -15 Volt winding is shunted by a TRIAC when the voltage peaks exceed a predetermined value (about 70 Volt pk-pk). This affords protection against input overvoltage (greater than about 32%) and results in blowing of the line fuse.

After rectification, each supply is capacitively filtered for approximately 1 Vp-p of ripple. Bleeder resistors are provided to discharge the filter capacitors (about 30 second time constant) when the instrument is unplugged. The entire unregulated portion of the power supply remains active whenever the instrument is plugged in. This provides the necessary power to keep the oven on for the optional high stability time base.

After filtering, each unregulated supply is fused and the + and -20 Volt legs are sent through a relay which controls the on and standby states. This relay also switches the fan on and off.

The regulators are of the series pass type. Each one consists of an op-amp to compare the output to a reference, a driver transistor to boost current and a common-emitter series pass element. The references are powered from the unregulated + and -20 Volt supplies to get them started at turn on. They are then switched over (by means of diode/resistor networks) to the + and -15 Volt regulated supplies to minimize ripple on the references. For standby mode, the input to the + and -15 Volt regulators is removed. This brings down the references which causes the other supplies to fall to zero Volts also. The reference diodes are 1% low drift Zeners. Each supply is remote sensed and passed through a voltage divider. This is adjusted for the correct output voltage. Low drift, tight tolerance resistors are used here to maintain the 0.1% accuracy spec on the supplies. This tight spec also requires careful grounding of the references and the voltage dividers using the separate "sense ground".

Several other protection and convenience features appear on each supply. Foldback current limiting is employed to prevent destruction of parts or fuse blowing resulting from supply output shorts. The voltage across a sense resistor is monitored and when a predetermined value is exceeded, the drive to the series pass transistor is reduced as necessary. Overvoltage protection by means of an SCR triggered by a zener diode is used on all supply outputs. Reverse voltage is kept to one diode drop with a diode on each supply. Finally, an LED is provided (in series with a zener diode and resistor) to indicate when a supply is up and close to the correct voltage.

The attenuator driver provides the proper drive signals to control the attenuator and RF switches in the HP 8642A and B. It also drives the relay for the reverse power protection circuit. The HP 8642A attenuator requires continuous drive signals whereas the HP 8642B requires pulsed outputs.

Detailed Description (SS53)

Power Transformer

The power transformer for the HP 8642 has multiple input and output windings. The primary windings provide for selection of four different line voltages, 100, 120, 220 and 240Volts. The secondaries consist of three separate windings. One center tapped winding provides (18.7 VAC per side) voltages for the +/-15V supplies. Another center tapped winding (9.0VAC per side) provides the drive for the +/- 5.2V supplies. The third (53.4VAC) provides the voltage for the +50V supply.

A18 Circuits

The A18 board contains the rectifier and filter circuitry. C6 reduces coupling of high frequency power line noise into the regulator circuits and helps prevent noise from the +/- 20V rectifiers from getting out to the power line, C7 does the same for the +/- 5.2V supplies. Q1 is a TRIAC used for input overvoltage protection. It is triggered at about 70V pk-pk by Zener diodes VR1 and VR2.

CR1 provides full wave rectification for +20V. C1 filters +20V and R2 provides a bleed down resistance for C1. CR2 and CR3 rectify -20V, C2 filters -20V and R3 is the bleeder resistor for C2. K1 switches the +/- 15V power supplies on and off via the front panel switch. CR11 prevents inductive voltage spikes at the front panel switch.

U1 is used to provide a regulated -14V supply for the instrument's DC fan. R7 and R8 set this voltage. CR12 protects U1 when the instrument is turned off. C8 and C9 prevent oscillation in U1.

CR4 is the rectifier for +10V. C3 filters +10V and R4 is the bleeder resistor for C3. CR5 and 6 rectify the -10V supply, C4 filters -10V and R5 bleeds down C4 at turn off.

CR7-10 provide full wave rectification for +50V. C5 filters +50V and R6 is C5's bleeder resistor.

A17 Circuits

The A17 board contains the regulator circuits for the five power supplies and the attenuator driver circuits. Only the positive supplies will be described here as the negative ones are identical except for component polarities, loop compensation values and current limit points.

+15 Volt Supply

+15V is regulated by a series pass transistor, Q2. It is driven by comparison amplifier U3C through an additional gain stage consisting of Q3, R7 and R51. R6, R10, C8 and C9 provide loop compensation to prevent oscillations. The inputs to U3C consist of a 6.3 volt reference determined by VR3 at pin 10 and the supply output remotely sensed and divided down to equal the voltage of VR3 at pin 9.

VR3 is a low drift temperature compensated Zener diode. It is biased from +15V through R15, R16 and CR6 when the supplies are on. To get it started at turn on since the +15V is not present, the bias is provided by the +20V divided down by R13 and R14. CR5 turns this bias off when +15V comes up. This prevents the ripple present on the unregulated supply from getting onto the Zener reference.

The power for U3A-D is provided in the same manner as the bias for VR3. This is accomplished by CR3, R4, R11 and R12 for the positive supply, and CR9, R10, R29 and R30 for the negative supply. (See +50V DC Regulator U3A and 15V DC Regulator U3D.)

The voltage divider for the other input to U3C consists of two precision resistors R17 and R19 for low drift, and an adjustable resistor R18 with minimal adjustment range to minimize drift. The supply is remote sensed on the instruments distribution board to maximize accuracy at the load.

Foldback current limiting is provided by U1. R23 is used to sense the amount of current flowing through Q2. The voltage across it is monitored by U1. R20, R21, R22 establish a reference voltage at U1 pin 2 about 0.2V below the supply output voltage (+15.0V) at U1 pin 3 with no load. This allows up to 4.1A to flow through R23 (.05 ohms) and Q2 before current limiting takes place. If the load current exceeds this value the voltage between U1 pin 2 and 3 reverses polarity and the output of U1 goes negative which reduces base drive to Q3 through CR2. This in turn reduces base drive to Q2 and drops the supply output voltage.

As the voltage at Q2 collector drops the reference voltage at U1 pin 2 drops faster than the supply output voltage at U1 pin 3 (due to the effect of R20 connected to the -20V supply). This causes the current limit point to "fold back" to a lower value than the original 4.1A, and the supply output voltage drops further. The current limit point continues to foldback to a minimum of about .8 Amp in case of a short circuit or until equilibrium is reached (between .8 and 4.1A).

At turn on R20 pulls U1 pin 2 negative to allow the supply to start up. R8 and R9 provide about -4V for the negative supply to U1 to allow input and output voltages to include ground.

C11 provides compensation for light loads on the supply. CR1 prevents reverse voltage at the supply output. VR1 and Q4 provide overvoltage protection. If the voltage exceeds about 17 volts, VR1 turns on Q4, shorting the supply to ground. VR2, R24 and DS1 indicate when the supply is on and above about 13.5V.

+5.2V Supply

+5.2V is regulated by Q8 as a series pass transistor. It is driven by U4D through Q9, R43 and R64. R44, 45 and C26,27 provide compensation to prevent oscillation. The reference input to U4D is derived from VR3 (from +15V DC Regulator U3C pin 10) through a low drift voltage divider consisting of R53, 54 and 81. The supply output is remotely sensed and fed directly into the other input of U4D.

Foldback current limiting is provided by U4C. R50 senses the output current. The voltage across R50 is sensed by U4D which turns Q9 off through CR14 if excessive current is drawn. Foldback limiting is accomplished in the same manner as in the +15V supply with R47, 48, 49 setting a reference voltage at U4C pin 9 about .067V below no load supply output voltage. This results in initial current limiting at about 6.7 Amps, folding back to about 1.1 Amps with a short circuit. C17, VR7, Q10, CR15, VR8, R55 and DS3 provide the same functions as similar parts in the +15V regulator. Q10 shorts the supply for overvoltages exceeding about 6.5V and DS3 will be lit for supply voltages above 4V.

+50V Supply

+50V is regulated by series pass transistor Q14. It is driven by U3A through Q16, R80 and R69. R70,83 and C20,22 provide compensation. The inputs to U3A are Zener reference VR3 (from +15V DC Regulator U3C pin 10) and +50V divided down by precision resistors R75 and 77 and adjustable resistor R76.

Foldback current limiting is provided by Q15. R74 senses the current output. If the current is excessive, the voltage drop across R74 turns on Q17. This turns on Q15 which reduces the base drive to Q14. The initial current limit point is set by R71, and 65 at about .19Amps folding back to about .06 Amps with a short circuit. R73 and C23 roll off the gain above 10KHz to prevent oscillation in current limit mode. C21 provides compensation. CR18 prevents reverse voltage at the output. VR12 and Q19 provide overvoltage protection above about 57V. DS5 indicates that the supply is up and above 47V. DS5 is biased from +15V to prevent excessive current draw from +50V. DS5 is turned on by Q18 which is driven by +50V through VR11 and R78.

Negative Supplies

The -15V and -5.2V regulators operate identically to the +15V and +5.2V regulators except for foldback current limit points as follows:

Supply	Initial Current Limit	Foldback Limit
-15V	1.7 Amps	0.32 Amps
-5.2V	2.1 Amps	0.36 Amps

Attenuator Driver (SS54)

The control lines for the various attenuator sections are passed through U101 and U102 to invert them. These signals are then ANDed together by U104-107 with the timing pulses for the HP 8642B and a TTL HIGH for the HP 8642A. This yields two out-of phase outputs for each control line that are either pulsed or continuous. The two signals are applied to an individual attenuator section and, depending on which is HIGH and which is LOW, will cause the specific pad to be either switched in or out.

The selection for an HP 8642A or B is done by U120. If the input at J3 pin 8 is LOW, U120 will cause a TTL HIGH to be sent to U104-107 which gives continuous outputs. This is the proper selection for the HP 8642A. For an HP 8642B, the control input is HIGH. This causes the pulses from U114 and U115 to be sent through U120 to U104-107.

Two different timing circuits are used for the HP 8642B. One is for the attenuator solenoids and the other is for the doubler RF switch. Each timing circuit has three one-shots to set three different time constants. One is the pulse width output to the attenuator. The other two determine the 'dead' time

between allowed switching pulses. This is necessary to prevent overheating of the solenoids. The two different timing circuits function identically except for the length of the pulses so only the attenuator pulse circuit will be described.

A positive edge at U116 pin 13 goes through to U114 pin 2 and U114 pin 10. This triggers U114A and B which outputs a 20msec HIGH pulse on U114 pin 13 and a 43msec LOW pulse on pin 12. The 20msec pulse energizes the attenuator through U104-107. There is also a 20msec LOW pulse output at U114 pin 4. The positive edge at the end of this pulse triggers U121A which puts out a 78msec LOW pulse at U121 pin 4. The 43msec and 78msec LOW pulses are ANDed together to produce a 98msec "ATN LEVEL LOCK" pulse which is sent back to the controller to tell it that the attenuator is not ready to be switched again. This signal also goes back and locks out the trigger input at U116 pin 12. Two one-shots are used for lockout. The 43msec output has 55msec to reset after it times out while the 78msec one shot is still active. This allows retriggering immediately after the 78 msec timeout without waiting for set up time on the one-shots.

The other three one-shots are set for time constants of 39, 57 and 58msec respectively. They are used to pulse the solenoid for the doubler RF switch in the 8642B, and to produce the 97msec "ATN BAND LOCK" pulse for the controller.

The attenuator driver outputs are open collector relay driver chips which pull down to ground when activated.

The attenuator driver circuitry also contains a chip (U117) to drive the "HET SW CONTROL" line. This is an open emitter pull up which either floats or drives to +20V (unregulated) to activate the HET switch relay which selects non-HET bands.

The reverse power protect circuit biases the detector for reverse power sensing and also trips the protection relay when needed. R112,103 and 104 bias the detector (J3 pin 47) at 5.2V and U118 pin3 at 1.75V. When the detector senses an overload condition (RF level > +28dBm), it drives the input at J3 pin 47 above 7.7V and U118 pin 3 above 2.6V. Since U118 pin 2 is referenced at 2.6V by R105, 107, this causes the output of the comparator, U118, to go LOW. This in turn causes U119 pin 5 to go HIGH and pin 6 to go LOW. Pin 5 going HIGH turns off Q101 which opens the reverse power protect relay (reverse power relay is on the A16 Module (HP 8642A) or the A19 Module (HP 8642B)). Pin 6 going LOW alerts the instrument controller that this has happened. To reset this condition, the overload condition must be removed and the instrument controller must clock a negative edge into U119 pin 1.

A17 POWER SUPPLY REGULATOR TABLES

Overall Equipment

Power Supply Test Connector Board	08642-80053
Power Supply Test Connector Cable	08642-60959

NOTE

The Power Supply Test Connector Board and Cable plugs into A17 J2 in place of W10. The Power Supply Test Connector Board connects all of the power supply sense lines properly to allow the power supply to be operated and isolated from the instrument. Connect the Power Supply Test Connector Board to A17 J2 through the Power Supply Test Connector Cable.

Troubleshooting procedures for the A17 or A18 boards are not provided. Tables with common problems and possible causes are provided to assist in troubleshooting these boards. Use of these tables and reading the circuit descriptions provided should suffice for troubleshooting any problem on these boards.

Use the Power Supply Test Connector Board to isolate the power supply from the instrument when troubleshooting.

Table 8T-1. +15 Volt Regulator

Condition	Possible Problem/Solution
Supply Oscillating	Possible defective C9, C8, C11, R6 or R10
Can't adjust to $15V \pm 1.5mV$	Check U3 pin 10 for $6.3V \pm 63mV$ If U3 pin 10 is good, R17,R18 or R19 may be bad. If U3 pin 10 is bad, VR3 may be bad.
Output at about 1V, crowbar tripped.	VR1 or Q4 bad Loss of sense line return Defective U3
Output at zero Volts	Q2 open No base drive to Q2 R51,R7 or Q3 open No base drive to Q3 R10 open U3 defective Pin 4 of U3 not at about 10 to 15V Defective CR3,R12 or R11 Pin 3 of U3 at about 0V Defective CR5,R14 or R13
Excess ripple	CR4 open CR3 or R12 shorted CR6 or R15 open CR5 or R14 shorted R11 or R13 open
No foldback current limiting	CR2 or R22 open Defective U1 Pin 4 of U1 not at -3 to $-5V$ R8 or R9 defective
Always in foldback, no short on the output	R20 or R21 open Defective U1
Fuse for +15 blows	Q2 or Q3 shorted Foldback inoperative and output shorted Problem with attenuator driver circuit

Table 8T-2. -15 Volt Regulator

Condition	Possible Problem/Solution
Supply Oscillating	Possible defective C13, C12, C15, R59 or R28
Can't adjust to $-15V \pm 1.5mV$	Check U3 pin 12 for $-6.3V \pm 63mV$ If U3 pin 12 is good, R35, R36 or R37 may be defective If U3 pin 12 is bad, VR6 may be defective
Output at about 1V, crowbar tripped	VR4 or Q7 shorted Loss of sense return Defective U3
Output at Zero Volts	Open Q5 No base drive to Q5 R52, R25 or Q6 open No base drive to Q6 R28 open Defective U3 Pin 11 of U3 not at about -12 to $-15V$ CR9 or R29 open R30 shorted Pin 12 of U3 at about 0V CR11 or R32 open R31 shorted
Excess ripple	CR10 open CR9 or R29 shorted CR12 or R33 open CR11 or R32 shorted R30 or R31 open
No foldback current limiting	CR8 or R40 open Defective U2 Pin 7 of U2 not at about 2 to 4V Defective R26 or R27
Always in foldback, no short on output	R39 or R38 open Defective U2
Fuse on $-15V$ blows	Q5 or Q6 shorted Foldback inoperative and output shorted

Table 8T-3. +5.2 Volt Regulator

Condition	Possible Problem/Solution
Supply Oscillating	Defective C27, C26, C17, R44 or R45
Can't adjust to $5.2V \pm 520\mu V$	VR3 defective Defective R81, R53 or R54
Output at about 1V, crowbar tripped	VR7 or Q10 shorted Loss of sense return Defective U4
Output at zero Volts	Open Q8 No base drive to Q8 Q9, R43 or R64 open No base drive to Q9 R45 open Defective U4
No foldback current limiting	CR14 or R49 open Defective U4
Always in foldback, no short on output	R48 or R47 open Defective U4
Fuse for +5.2 blows	Q8 or Q9 shorted Foldback inoperative and output shorted

Table 8T-4. -5.2 Volt Regulator

Condition	Possible Problem/Solution
Oscillation	Defective C29, C28, C19, R57 or R58
Can't adjust to $-5.2V \pm 520\mu V$	Check U3 pin 12 for $-6.3V \pm 63mV$ VR6 defective R82, R66 or R67 defective
Output at about 1V, crowbar tripped	VR9 or Q13 shorted Loss of sense return Defective U4
Output at zero Volts	Q11 open No base drive to Q11 Q12 or R56 open No base drive to Q12 R58 open Defective U4
No foldback current limiting	CR16 or R62 open Defective U4
Always in foldback, no short on output	R61 or R60 open Defective U4
Fuse for -5.2V blows	Q11 or Q12 shorted Foldback inoperative and output shorted

Table 8T-5. +50 Volt Regulator

Condition	Possible Problem/Solution
Supply Oscillation	C22, C20, C21, R83 or R70 defective
Can't adjust to +50V \pm 5mV	U3 pin 3 not at 6.3V \pm 63mV VR3 defective R75,R76 or R77 defective
Output at about 1V, crowbar tripped	VR12 or Q19 shorted Loss of sense return Defective U3
Output at zero Volts	Q14 open No base drive to Q14 R69,R80 or Q16 open No base drive to Q16 R70 open Defective U3
No foldback current limiting	Q15,Q17,R72,R73 or R71 open
Always in foldback, no short at output	Q15 or Q17 shorted R65 open
Fuse for +50V blows	Q14 or Q16 shorted Foldback inoperative and output shorted

A18 POWER SUPPLY RECTIFIER-FILTER BOARD TABLE**Table 8T-6. +50 Unregulated Power Supplies**

Condition	Possible Problem/Solution
Line fuse blows	Wrong voltage selection Wrong fuse size VR1, VR2 or Q1 shorted C1, C2, C3, C4 or C5 shorted CR1, CR2, CR3, CR4, CR5, CR6, CR7, CR8, CR9 or CR10 shorted
Excess ripple on +15 unregulated	C1 defective 1/2 of CR1 open (voltage will also be low)
No input to +15 regulator	CR1 open F1 open K1 defective
Excess ripple on -15 unregulated	C2 defective CR2 or CR3 open (voltage will also be low)
No input to -15 regulator	CR2 and CR3 open F2 open Defective K1
Excess ripple on +5.2 unregulated	1/2 of CR4 open (voltage will also be low) C3 defective
No input to +5.2 regulator	CR4 open F3 open
Excess ripple on -5.2 unregulated	C4 defective CR5 or CR6 open (voltage will also be low)
No input to -5.2 regulator	CR5 and CR6 open F4 open
Excess ripple on +50 unregulated	C5 defective CR7, CR8, CR9 or CR10 open (voltage will also be low)
No input to +50 regulator	CR8 and CR10 or CR7 and CR9 open F5 open

Table 8T-7. Voltages at Fuse Outputs

A18 Fuse	DC Voltage	Ripple Vpp (50/60 Hz)
F5	56 to 71 Vdc	0.6 to 1.3 Vpp
F1	18 to 23 Vdc	0.6 to 1.8 Vpp
F3	7.5 to 10 Vdc	0.6 to 1.6 Vpp
F4	-9 to -11 Vdc	0.5 to 1.5 Vpp
F2	-20 to -25 Vdc	0.4 to 1.3 Vpp

Adjustments

ADJUSTMENT PROCEDURE FOR A17

Overall Equipment

DVM HP 3456A

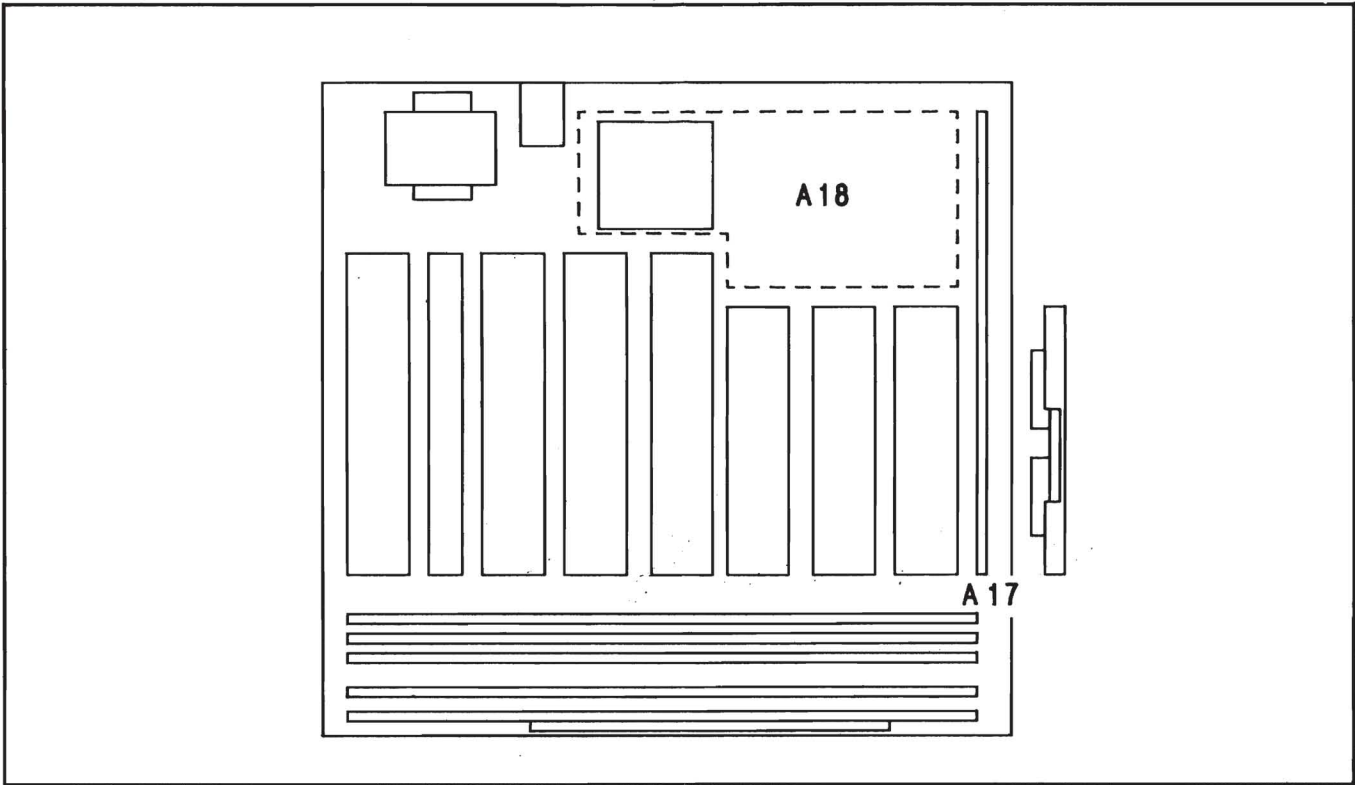
Procedure

1. Set the HP 8642 POWER switch to ON.
2. Ensure that all five LED indicators are on.
3. Attach the ground lead of the DVM to A17 TP6.
4. Attach the + lead of the DVM to A17 TP1.
5. Select DC Volts on the DVM.
6. Adjust A17 R18 for +15.000V \pm 0.030V.
7. Attach the + lead of the DVM to A17 TP2.
8. Adjust A17 R36 for -15.000V \pm 0.030V.
9. Attach the + lead of the DVM to A17 TP3.
10. Adjust A17 R53 for +5.2000V \pm 0.010V.
11. Attach the + lead of the DVM to A17 TP4.
12. Adjust A17 R66 for -5.2000V \pm 0.010V.
13. Attach the + lead of the DVM to A17 TP5.
14. Adjust R76 for +50.000V \pm 0.100V.

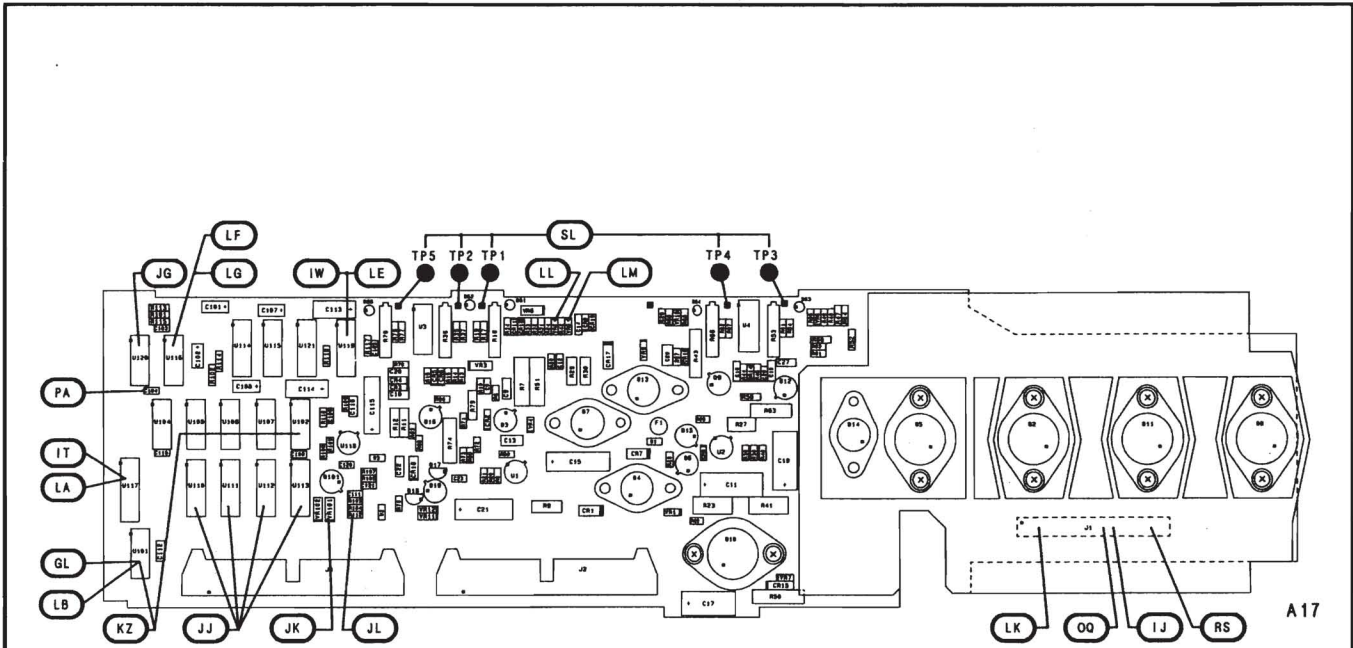
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Assembly Locator



Module Test Point/Adjustment Locations



Simplified Block Diagram

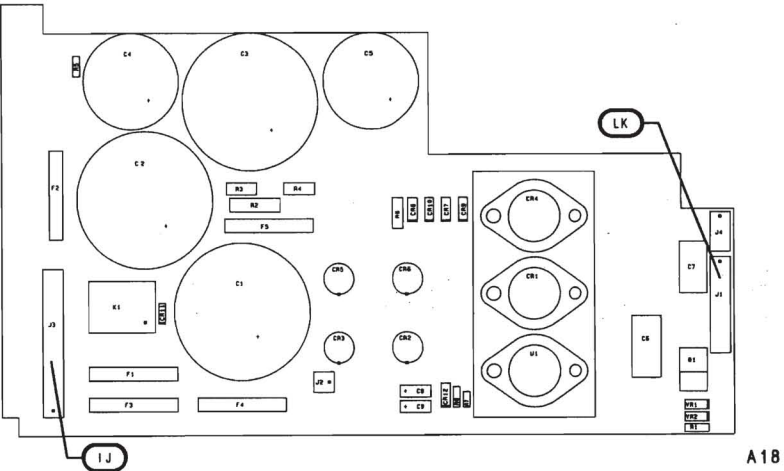
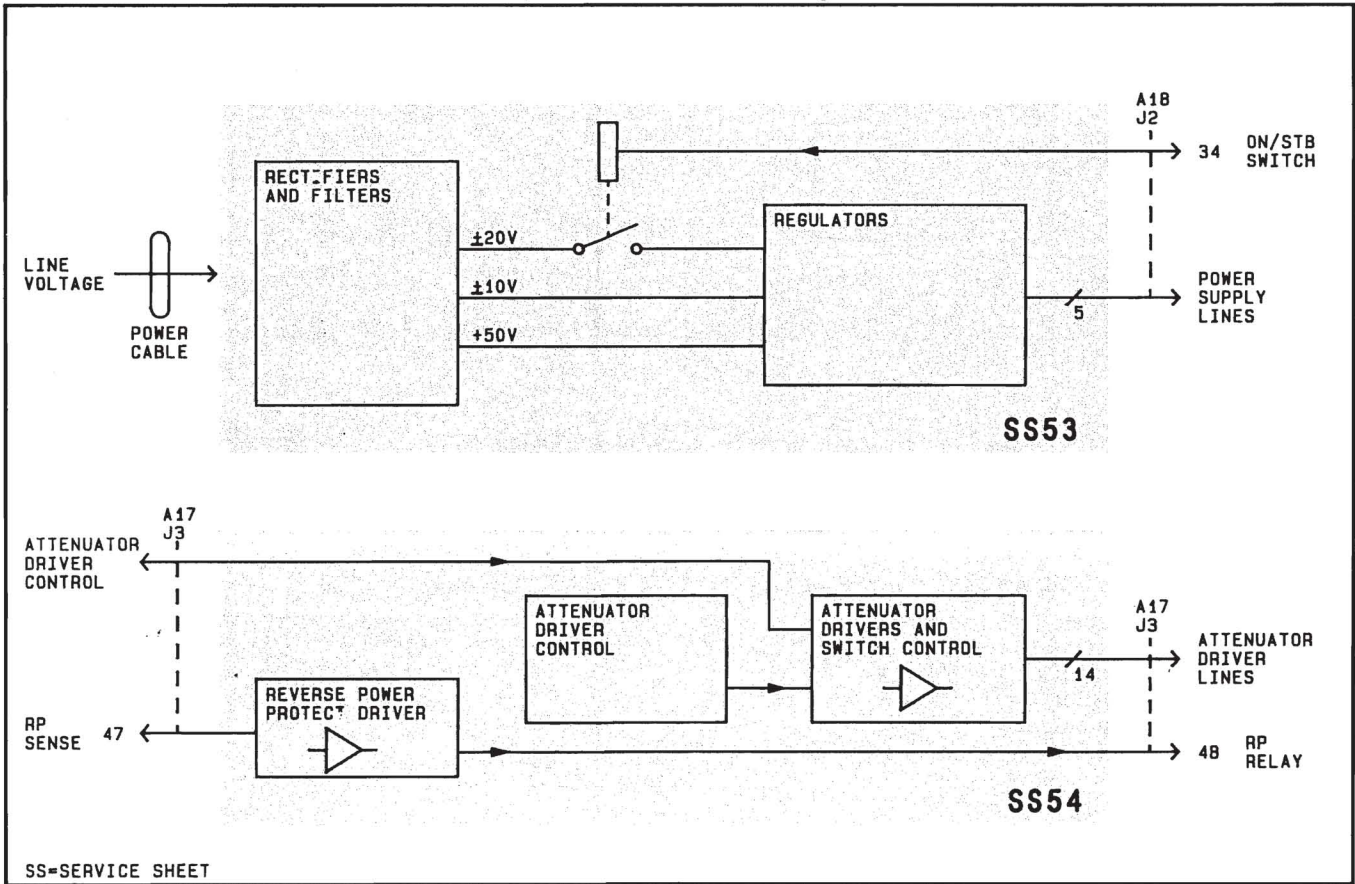


Figure 8T-100 BD17 General Information.

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CHANGES**2709A and above**

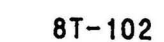
On the schematic:

- A17 - Change the *A17 POWER SUPPLY REG/ATTENUATOR DRIVER MODULE* part number to 08642-60227.





Reference Block Diagram
Component Coordinates

A17, A18 MODULE **BD 17**

CHANGES**All serial prefixes****In NOTES:**

- Add the Diagram of A8, shown on page 8T-102.3 to the area below "Notes" showing device pin configurations.

On the schematic:

- To the right of A8 J4 pin numbers add:

Pin #1 = BLACK

Pin #4 = BROWN

Pin #2 = RED

Pin #3 = WHITE

2533A and above**On the schematic:**

- A17R84 - In **+50V DC REGULATOR**, add a resistor from the collector to the emitter of Q15. Designate it R84 and assign a value of 1K ohms. Note that the component locator for A17 is on page 8T-104, and that R84 is mounted to the back of the board directly under Q14.

2709A and above**On the schematic:**

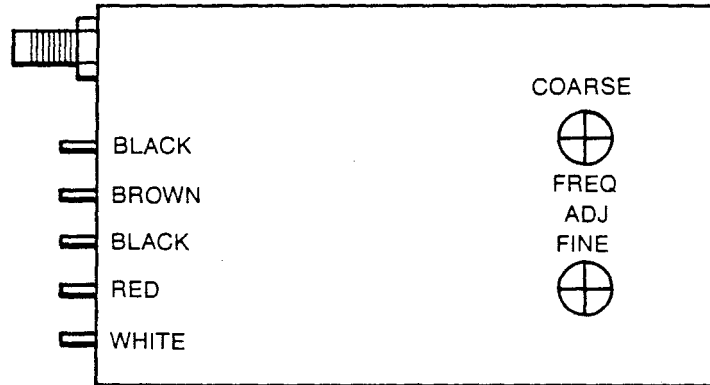
- A17 - Change the A17 part number to 08642-60227 and replace the appropriate portion of the schematic with the schematic partial on page 8T-102.5.

2810A and above**On the A17 schematic:**

- A17 - Change the A17 assembly part number to 08642-60327.

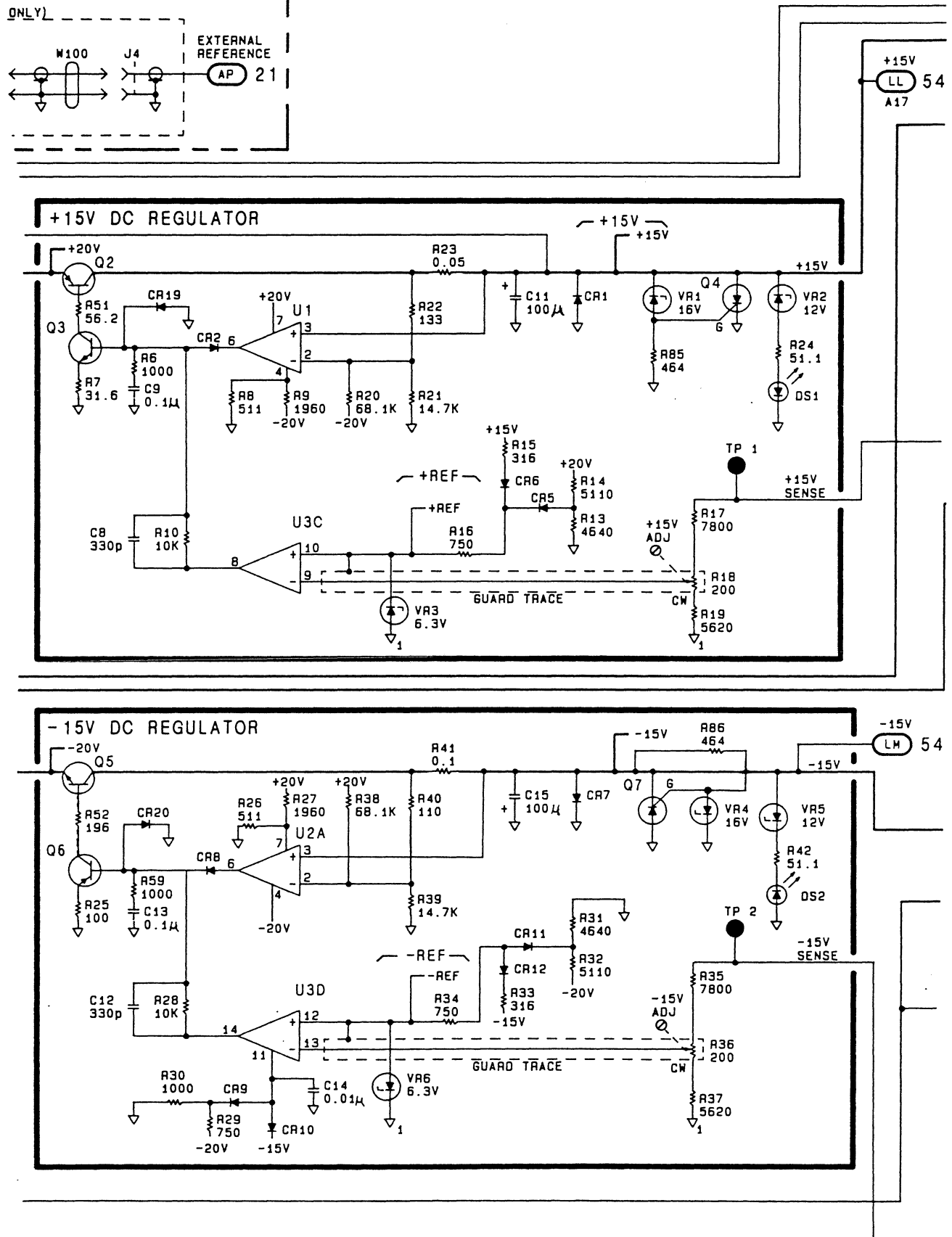
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End Plate View OPT 001

P/O A17 POWER SUPPLY REGULATOR/ATTENUATOR DRIVER



SS53

Figure 8T-103. P/O A17 Power Supply Reg/Attenuator Driver Module.

8T-102.4

3 MODULE (08642-60227)

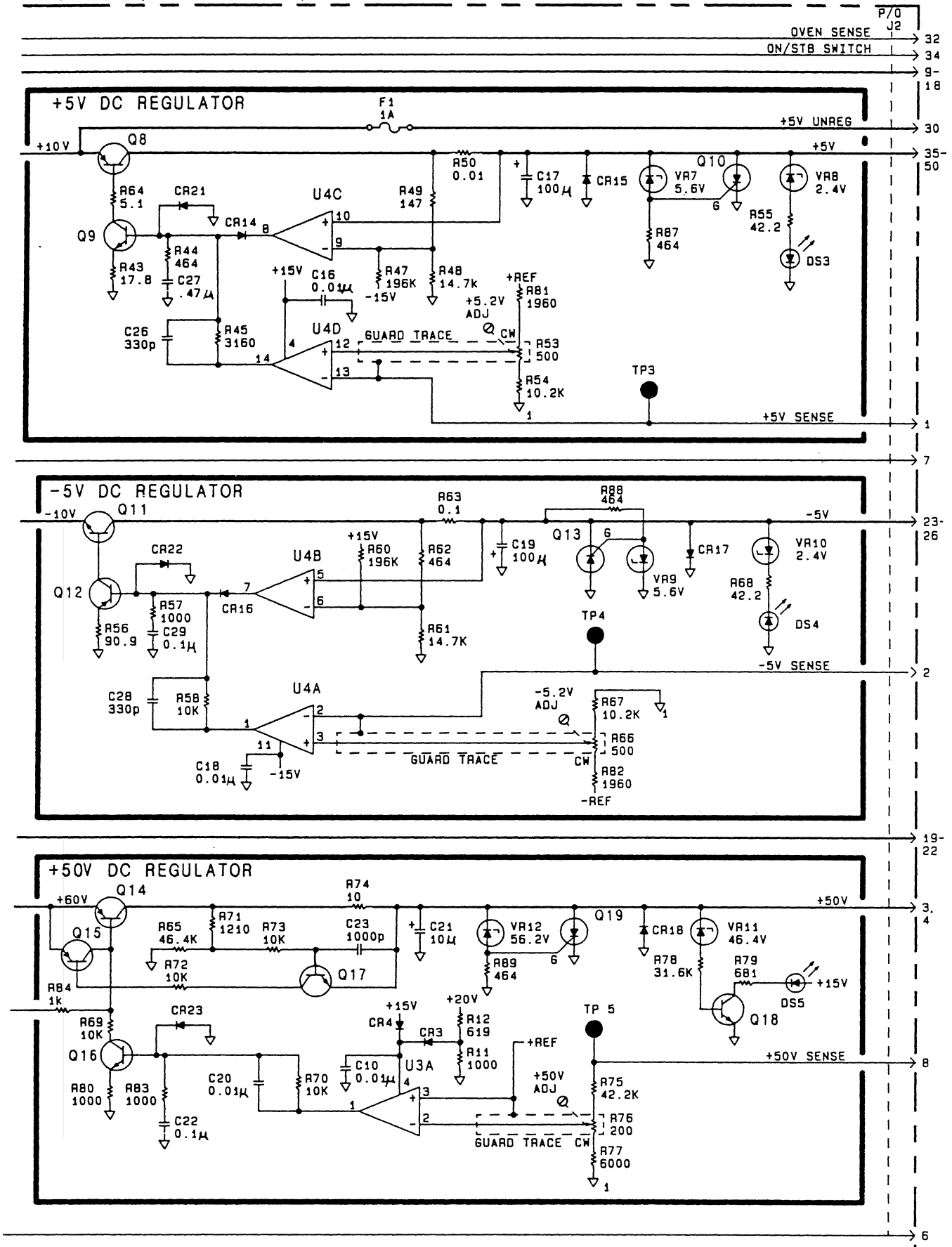
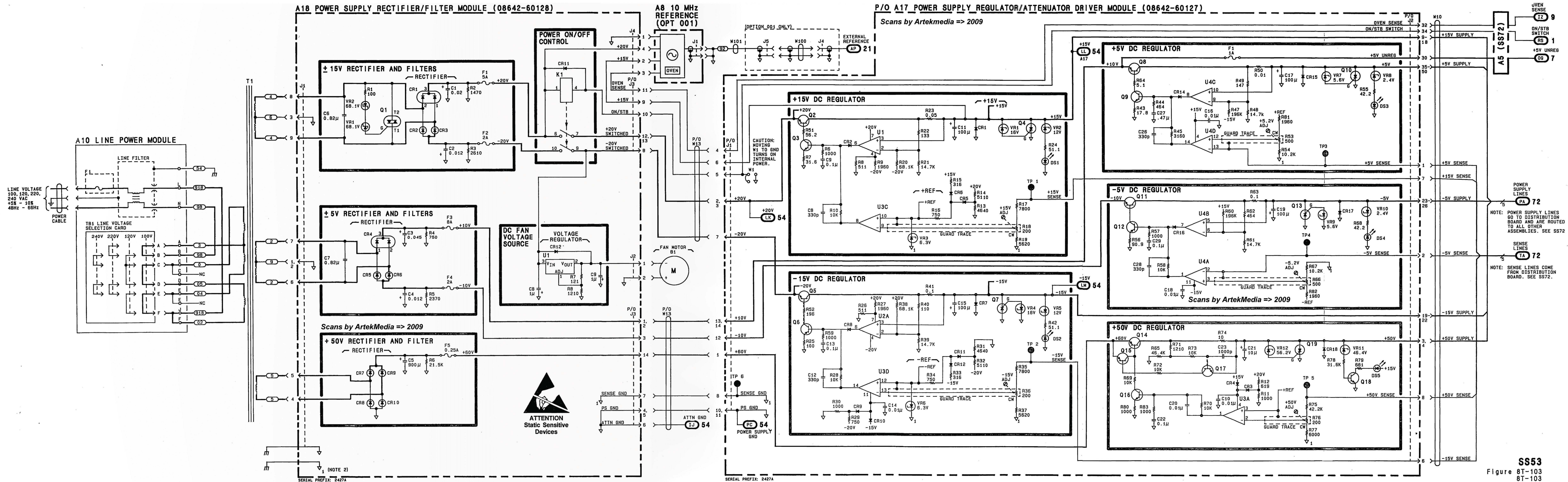


Figure 8T-103. P/O A17 Power Supply Reg/Attenuator Driver Module.

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P/O A17, A18 SEE REVERSE SIDE P/O REG/ATTN DRIVER MODULE, POWER SUPPLY RECTIFIER/FILTER ASSY **SS53**

- ### Schematic General Information

CHANGES**2509A and above**

On the schematic:

- R113, R114, R116 - In ATTENUATOR DRIVER CONTROL, change R113 to 56.2K, R114 to 82.5K, and R116 to 56.2K.

2533A and above

On the Component Locator:

- A17R84 - Add R84 to the center of Q14 and indicate that it is attached to the back of the board.

2709A and above

On the Component Locator:

- Replace the A17 component locator with the new A17 component locator on page 8T-104.3.

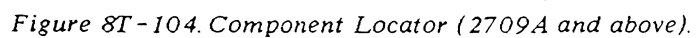
On the schematic:

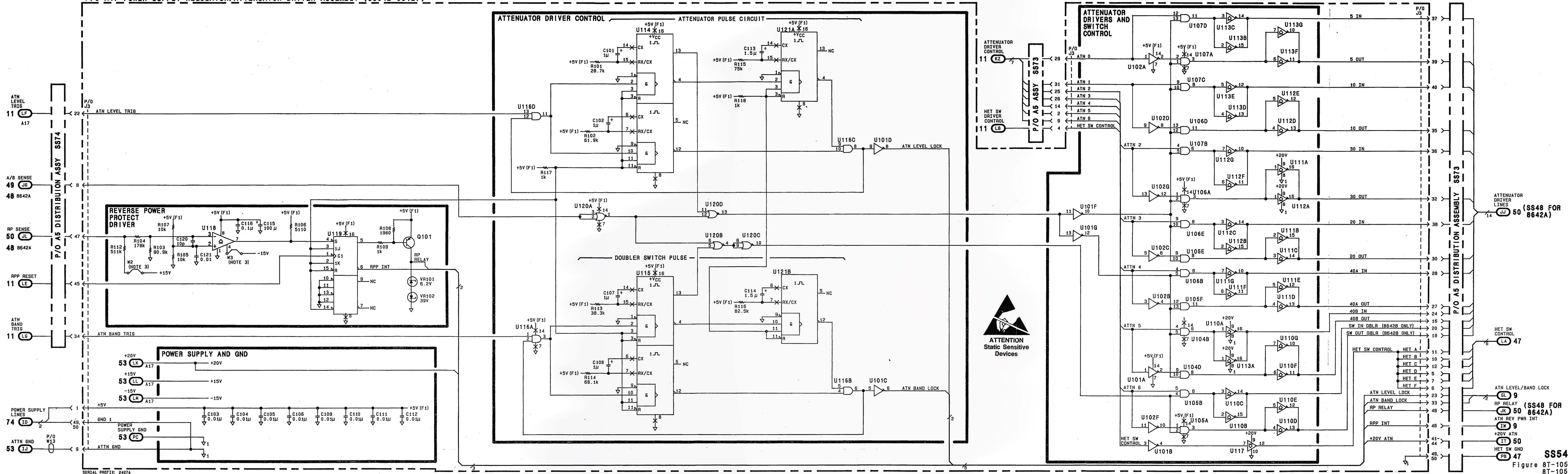
- A17 - Change the board number of A17 to 08642-60227.

2810A and above

On the A17 schematic:

- A17 - Change the A17 assembly part number to 08642-60327.





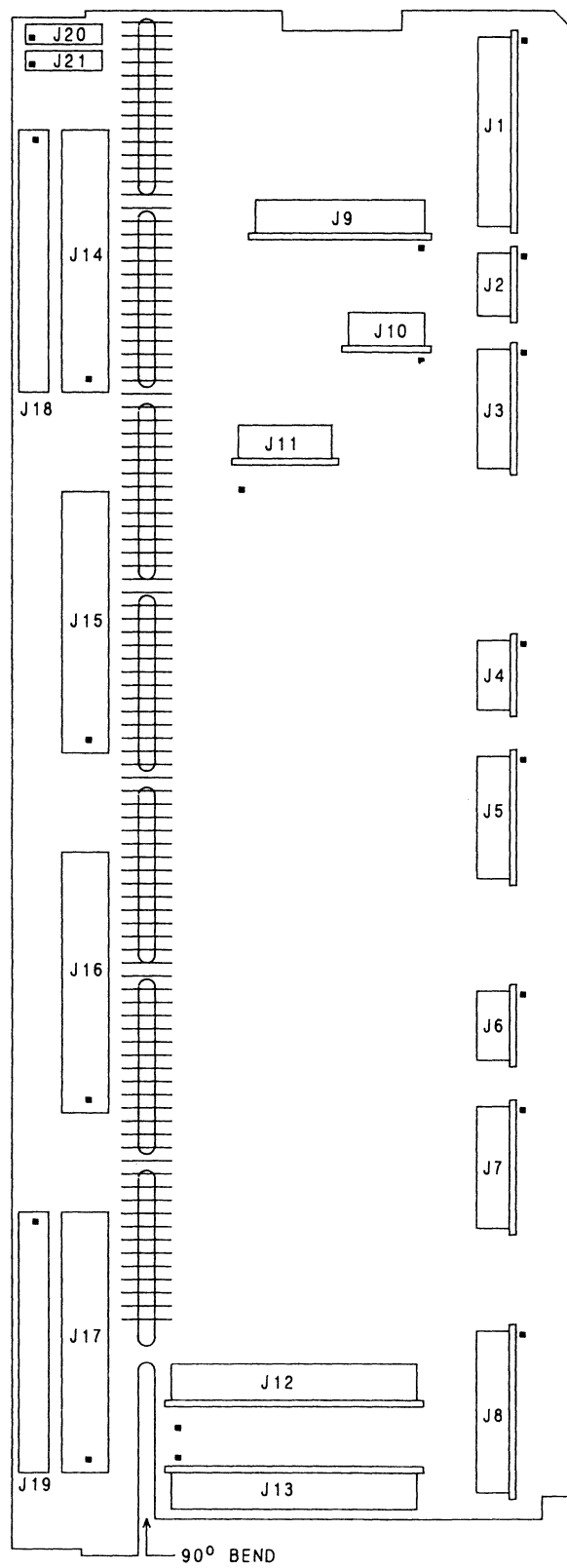
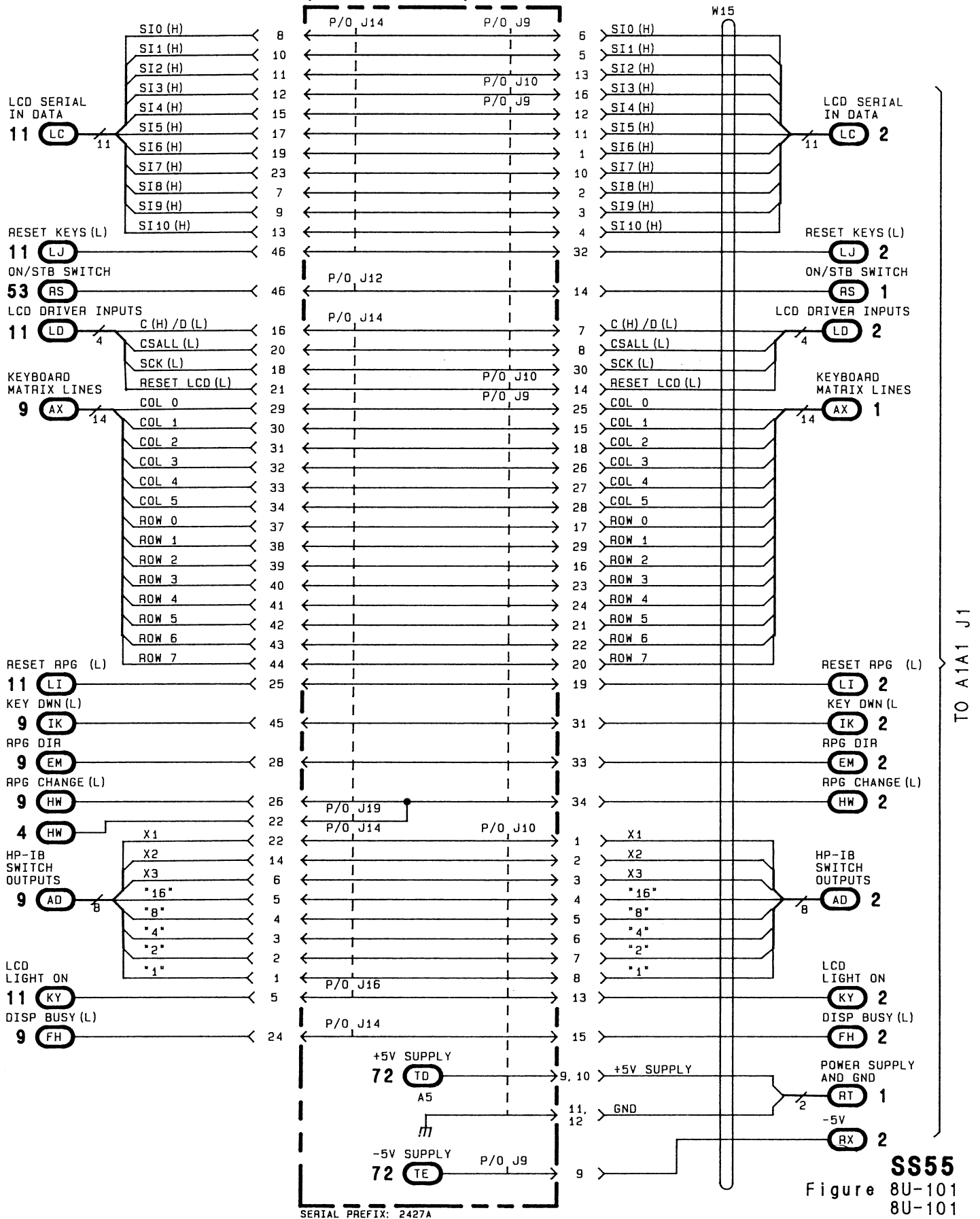


Figure 8U-100 Component Locator

**P/O A5 POWER SUPPLY/DIGITAL
DISTRIBUTION ASSEMBLY
(08642-60126)**



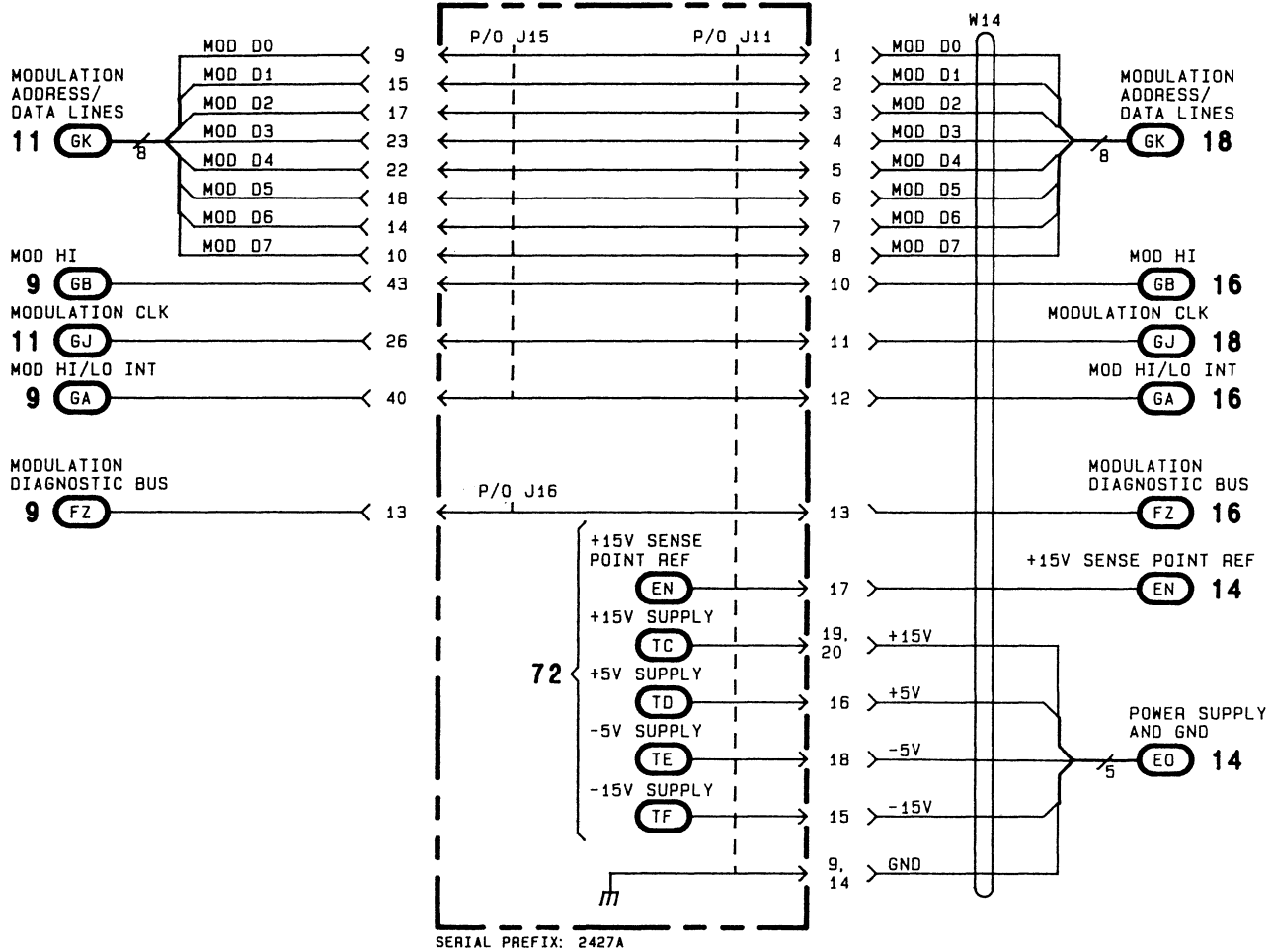
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Figure 8U-101
8U-101

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TO A2 J1

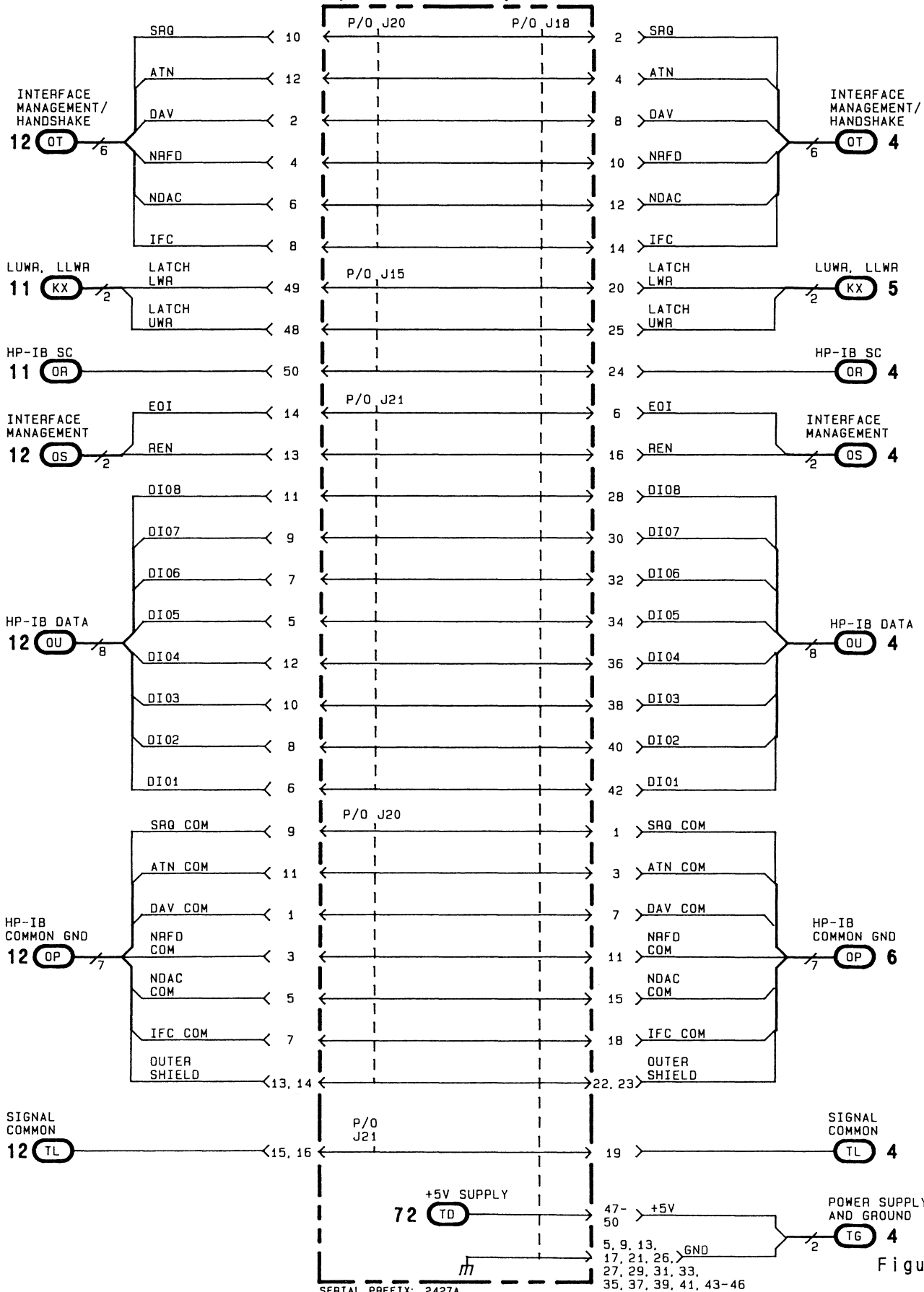
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Figure 8U-103
8U-103

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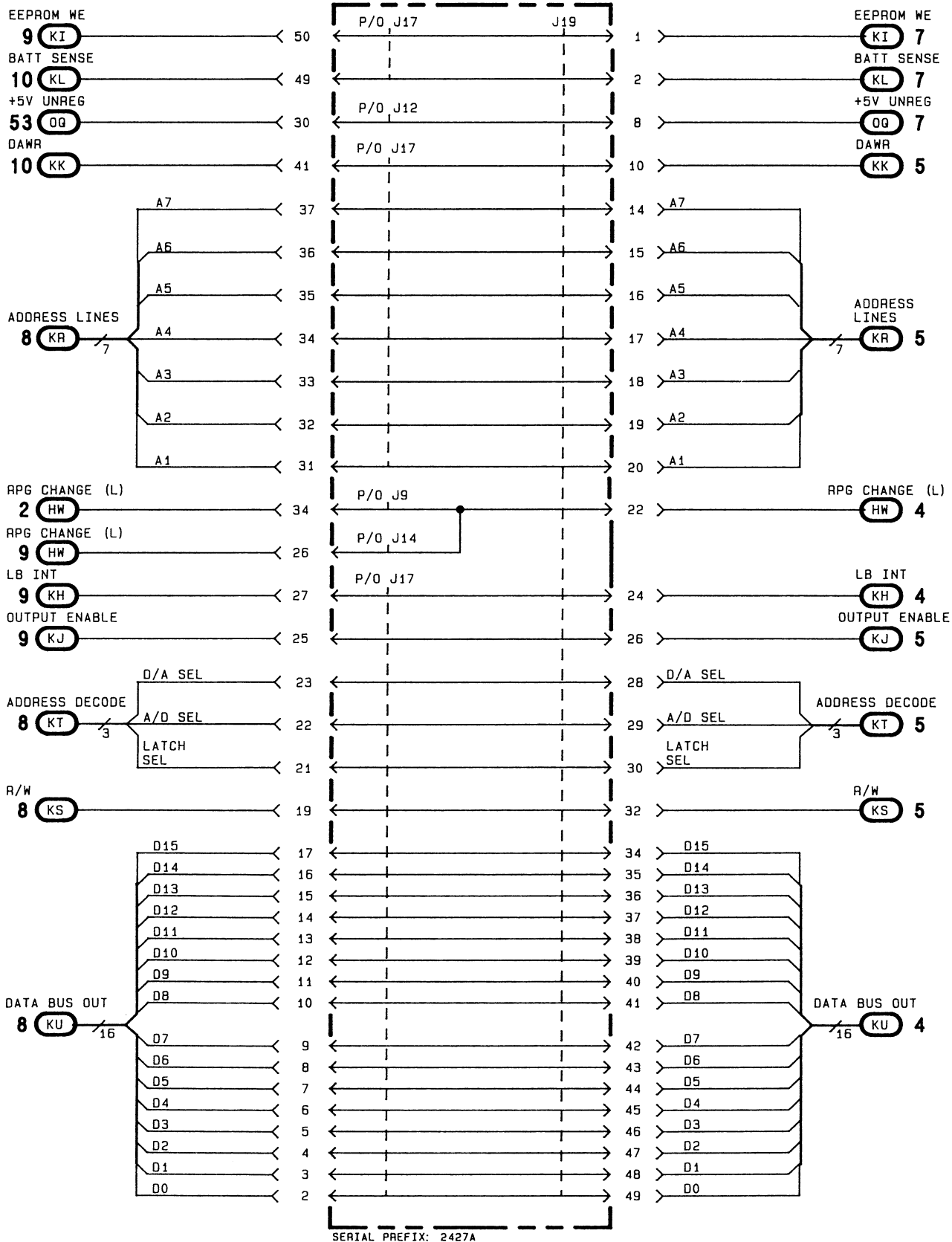


P/O A3 P5

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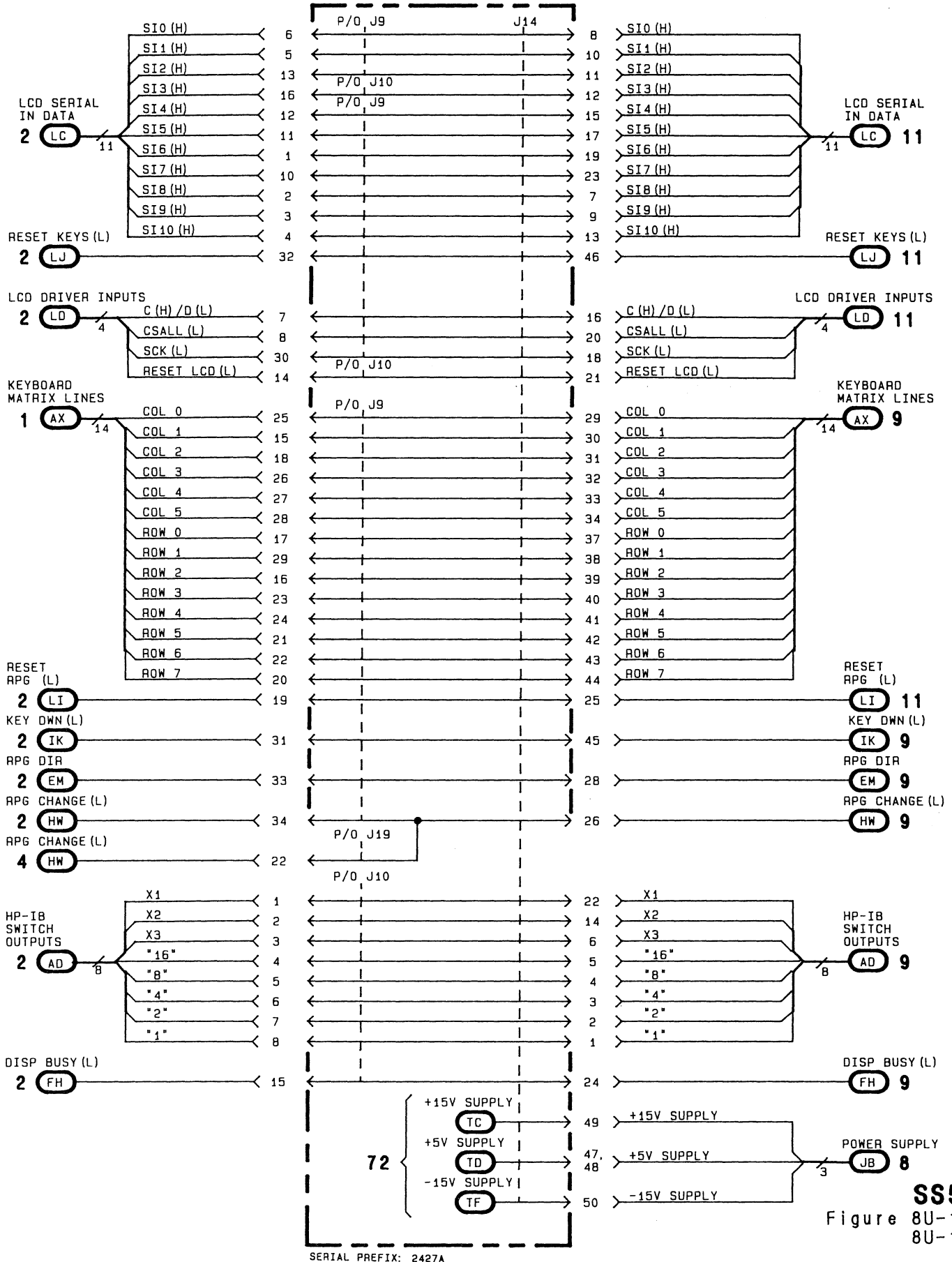


SS58
Figure 8U-107
8U-107

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A4 P4

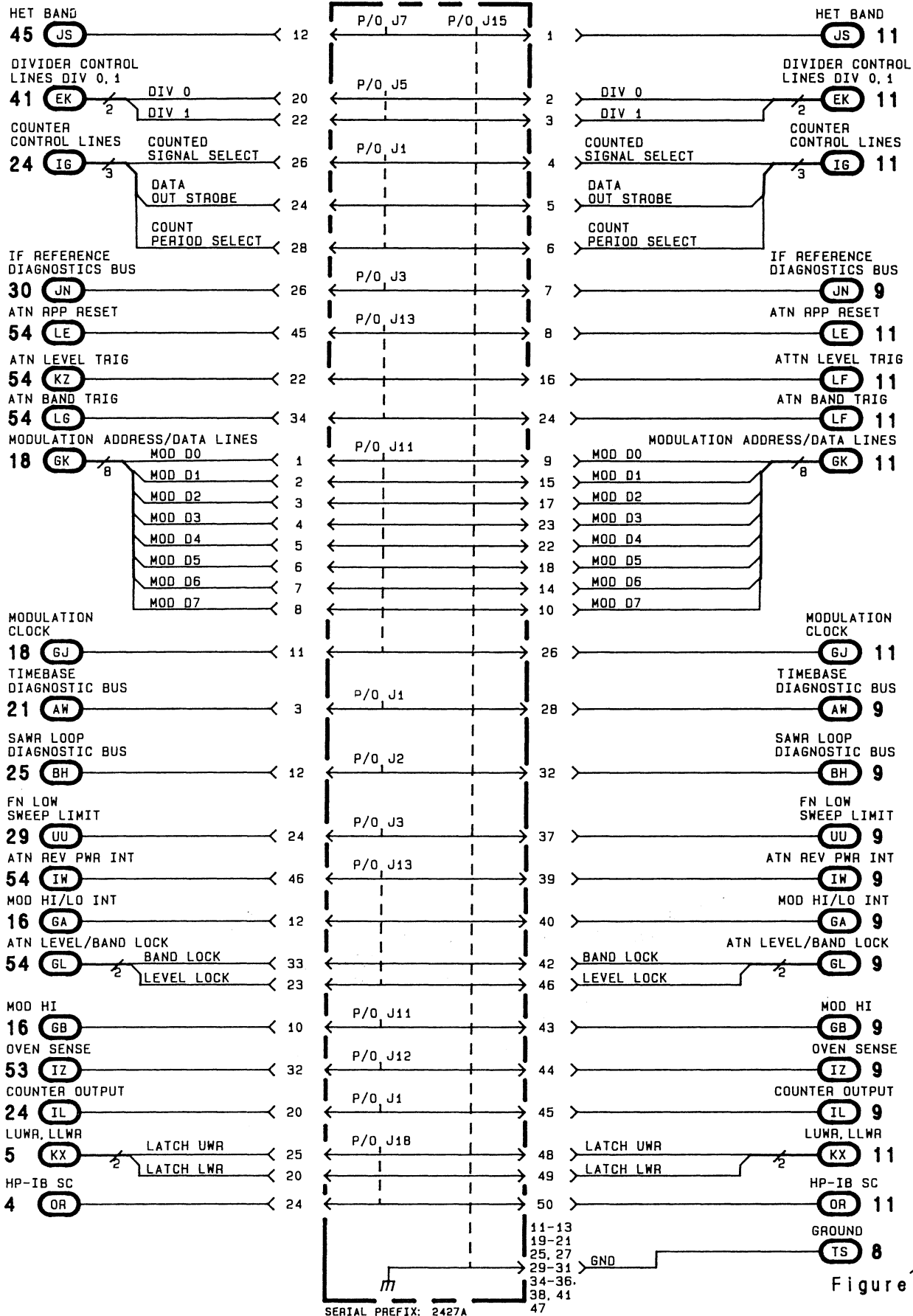
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Figure 8U-109
8U-109

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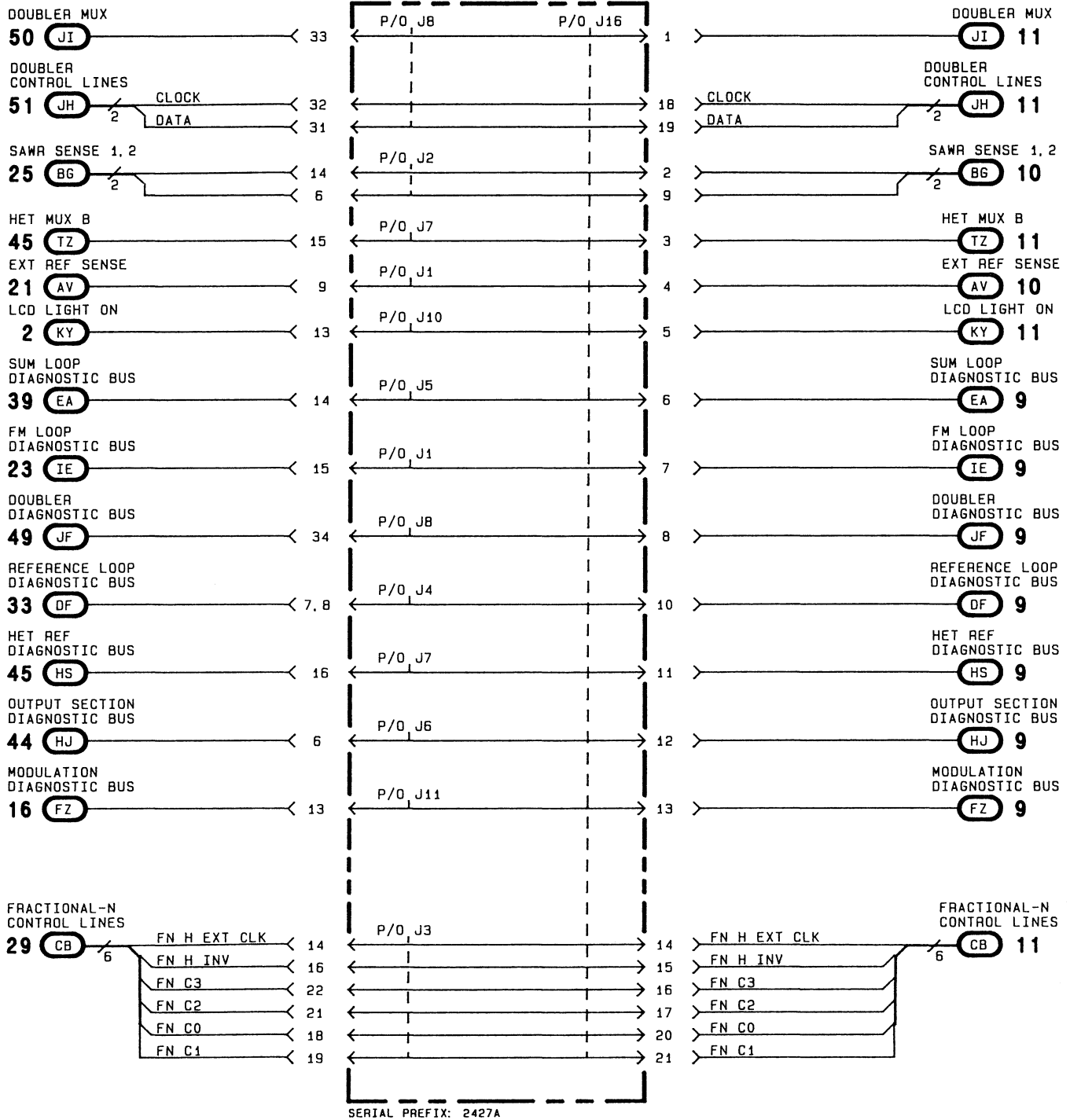
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Figure 8U-111
8U-111

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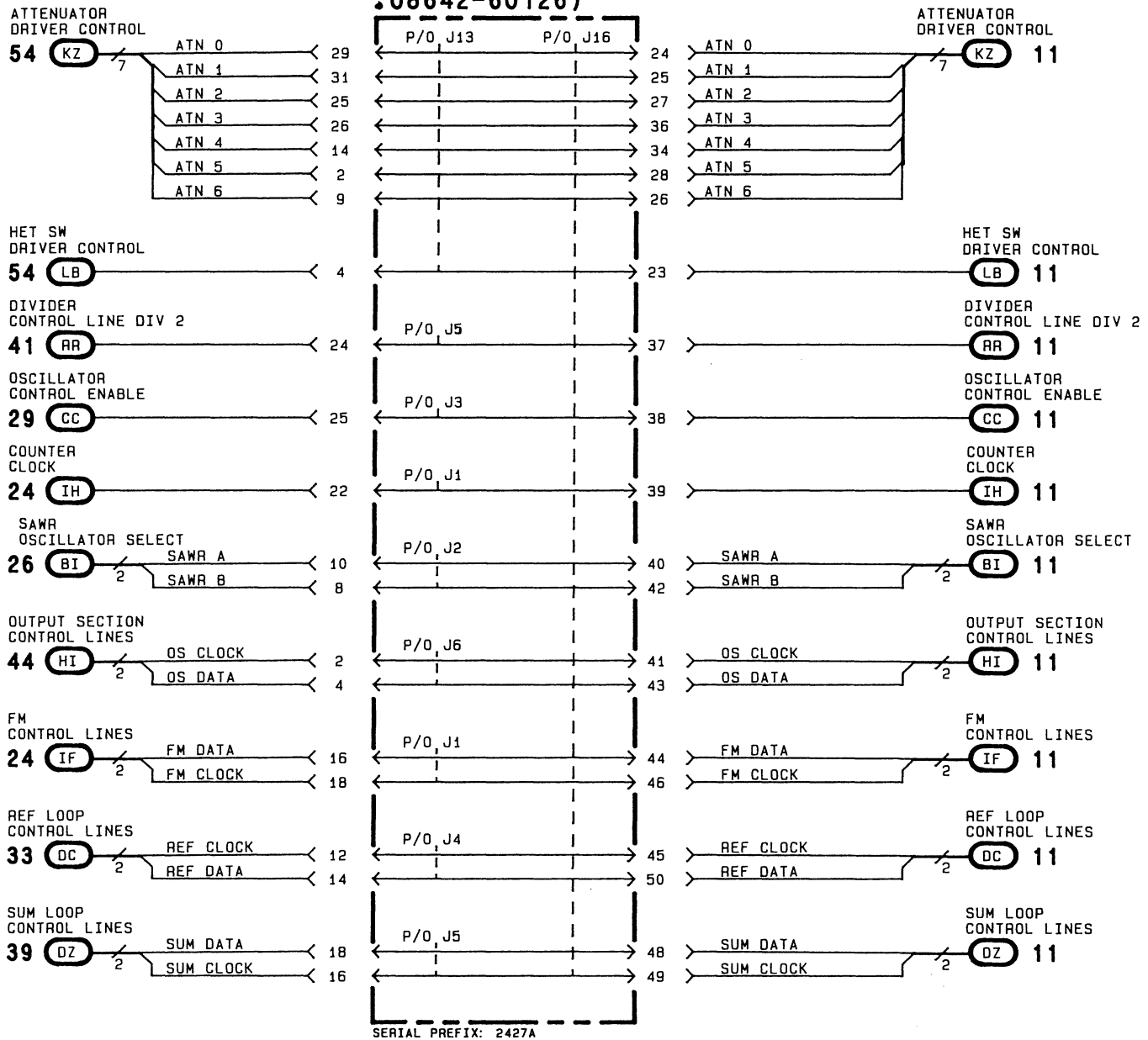


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A4 P2 (2 OF 2)

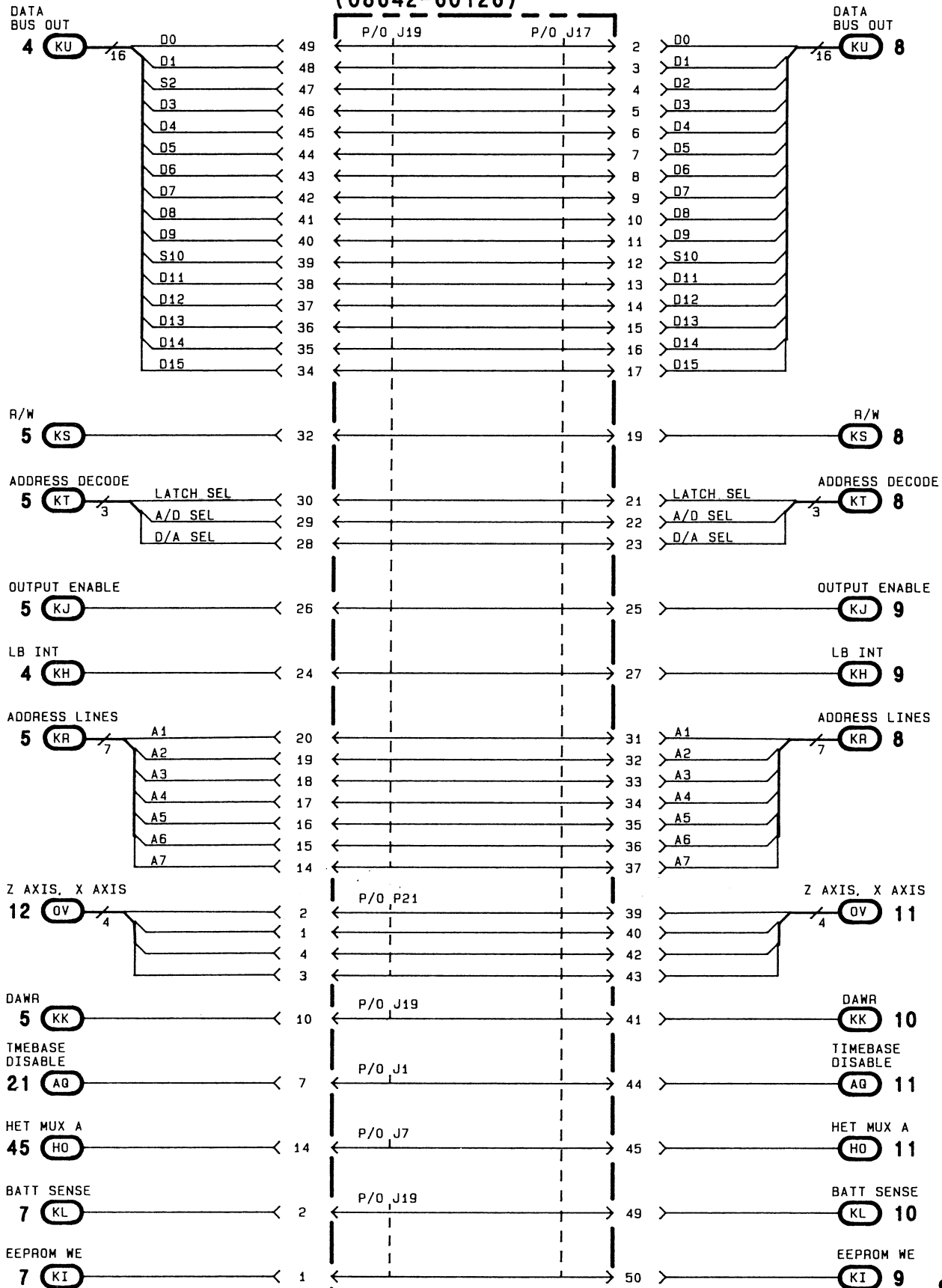
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Figure 8U-115
8U-115

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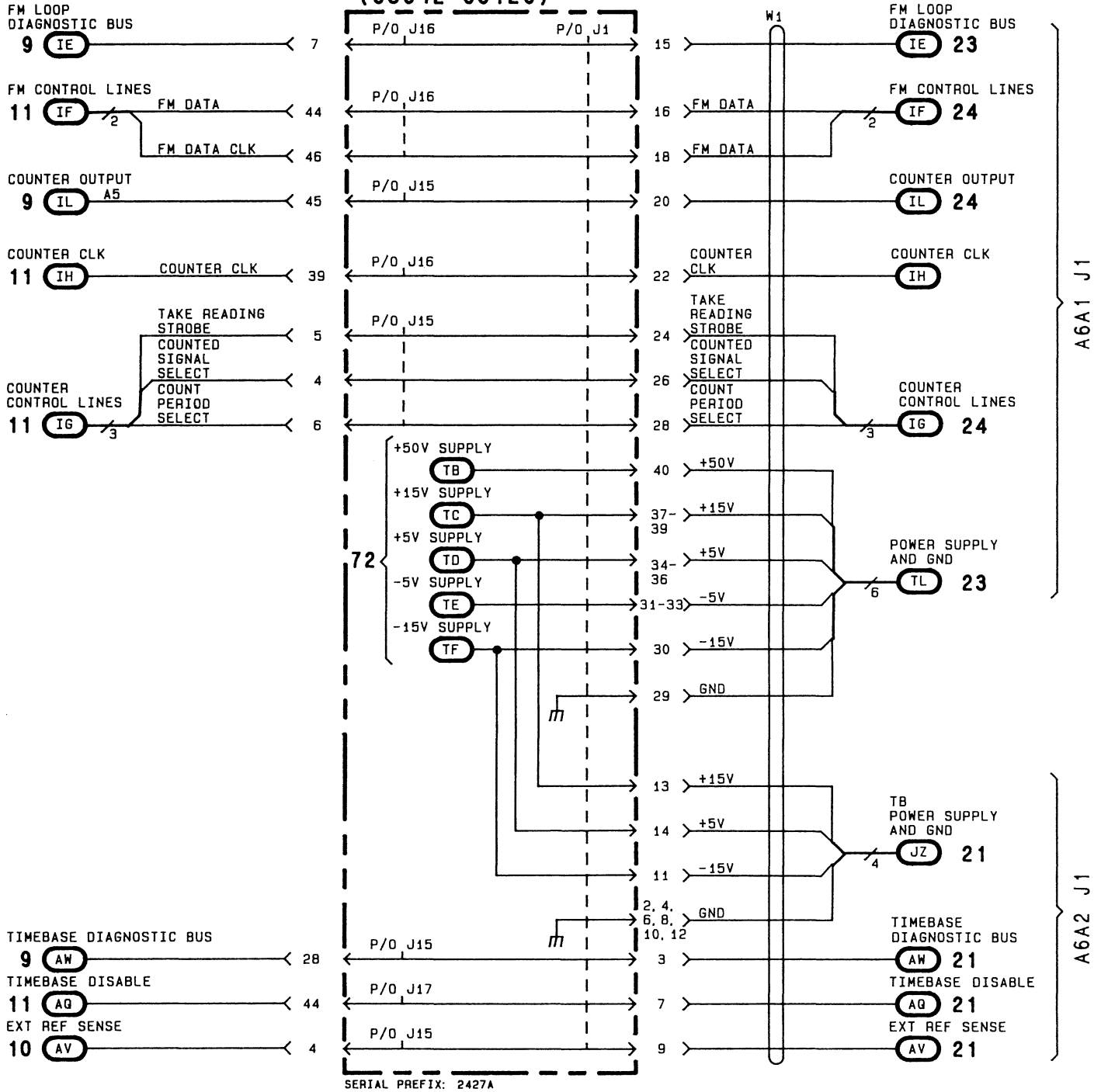
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Figure 8U-117
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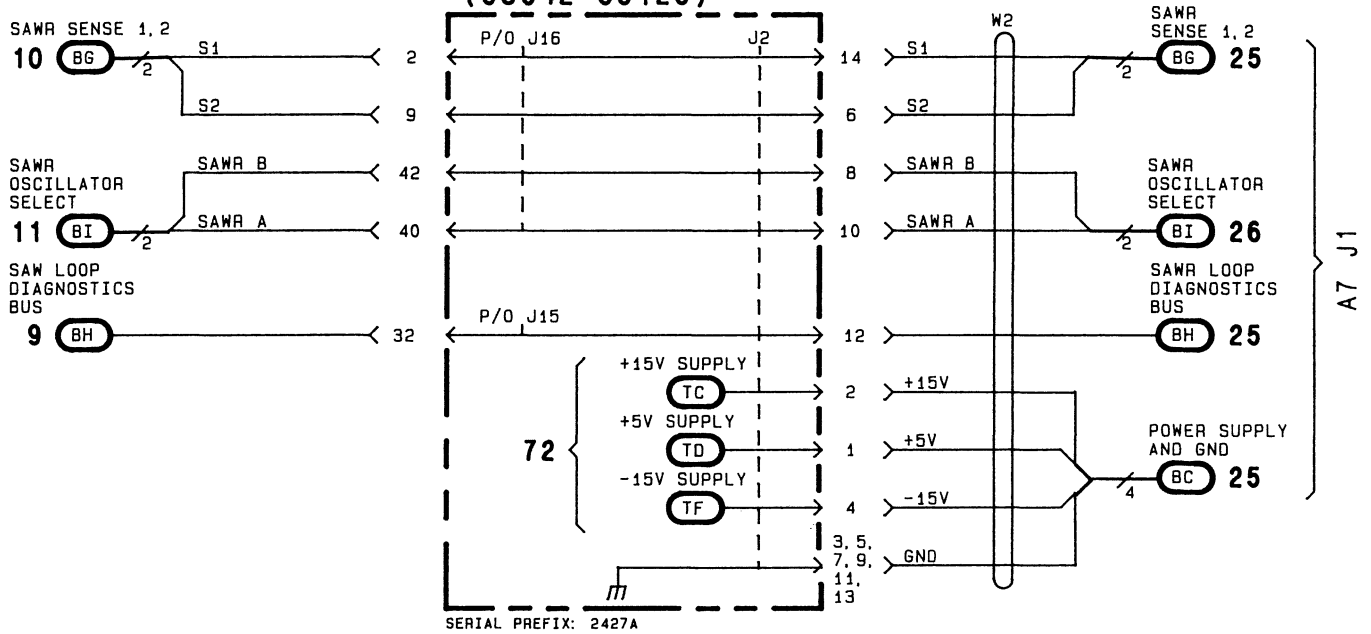
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Figure 8U-119
8U-119

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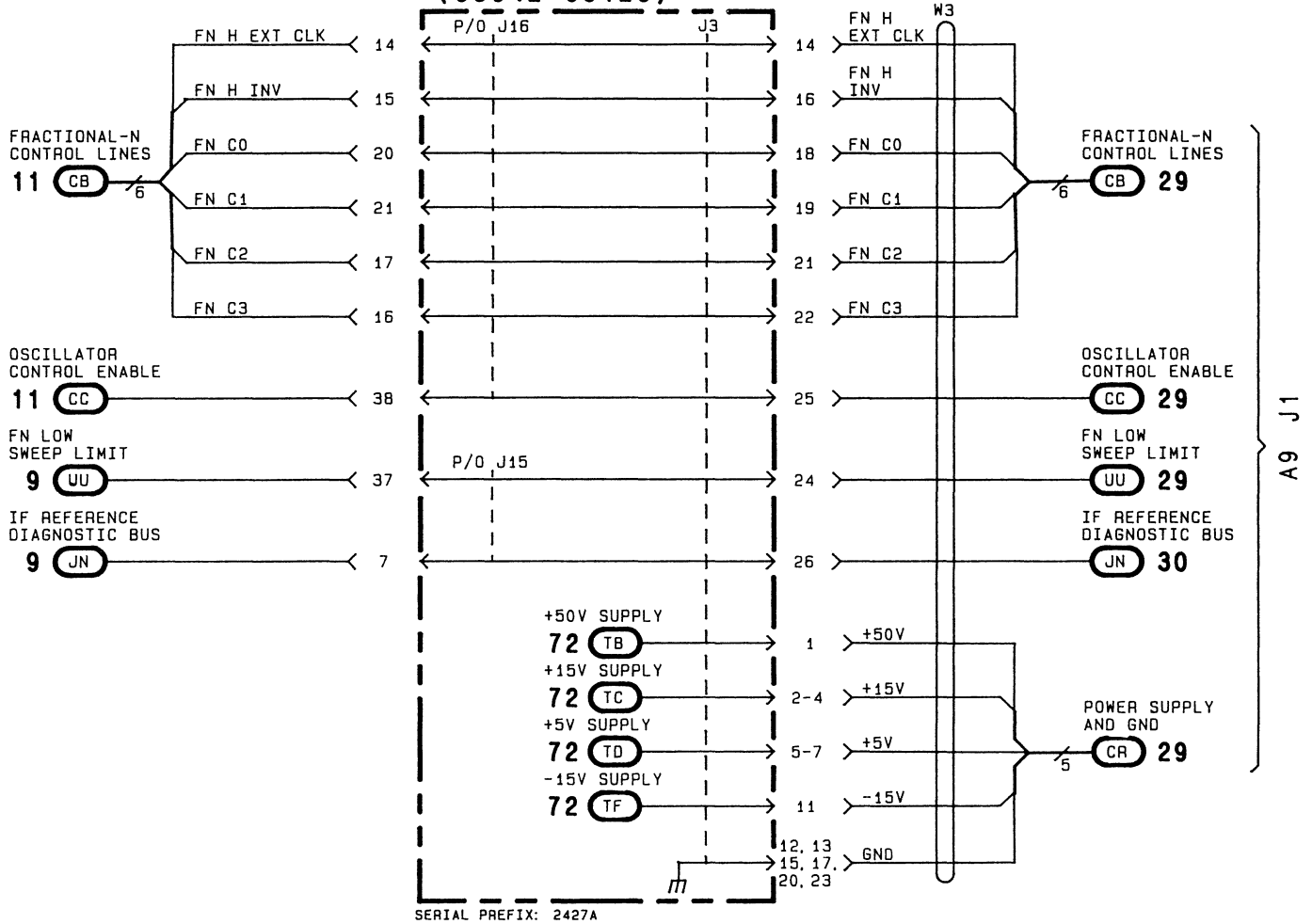
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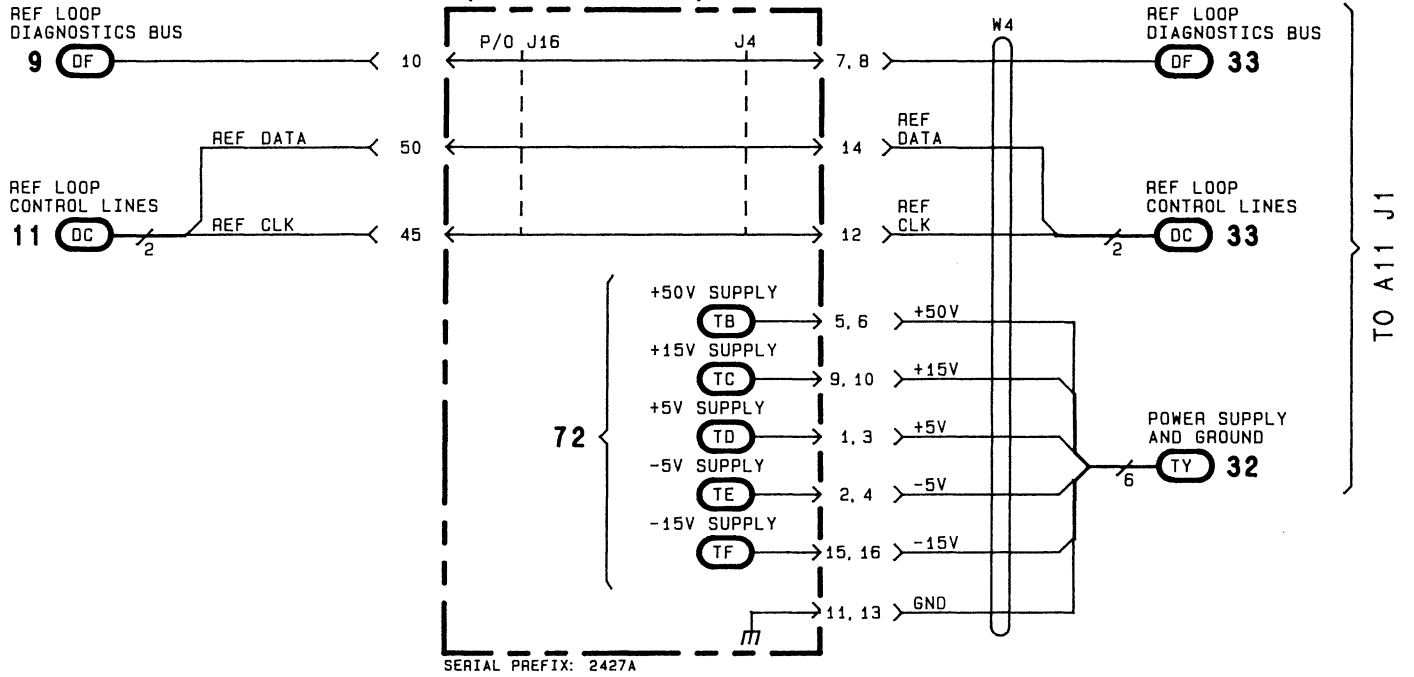


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Figure 8U-123
8U-123

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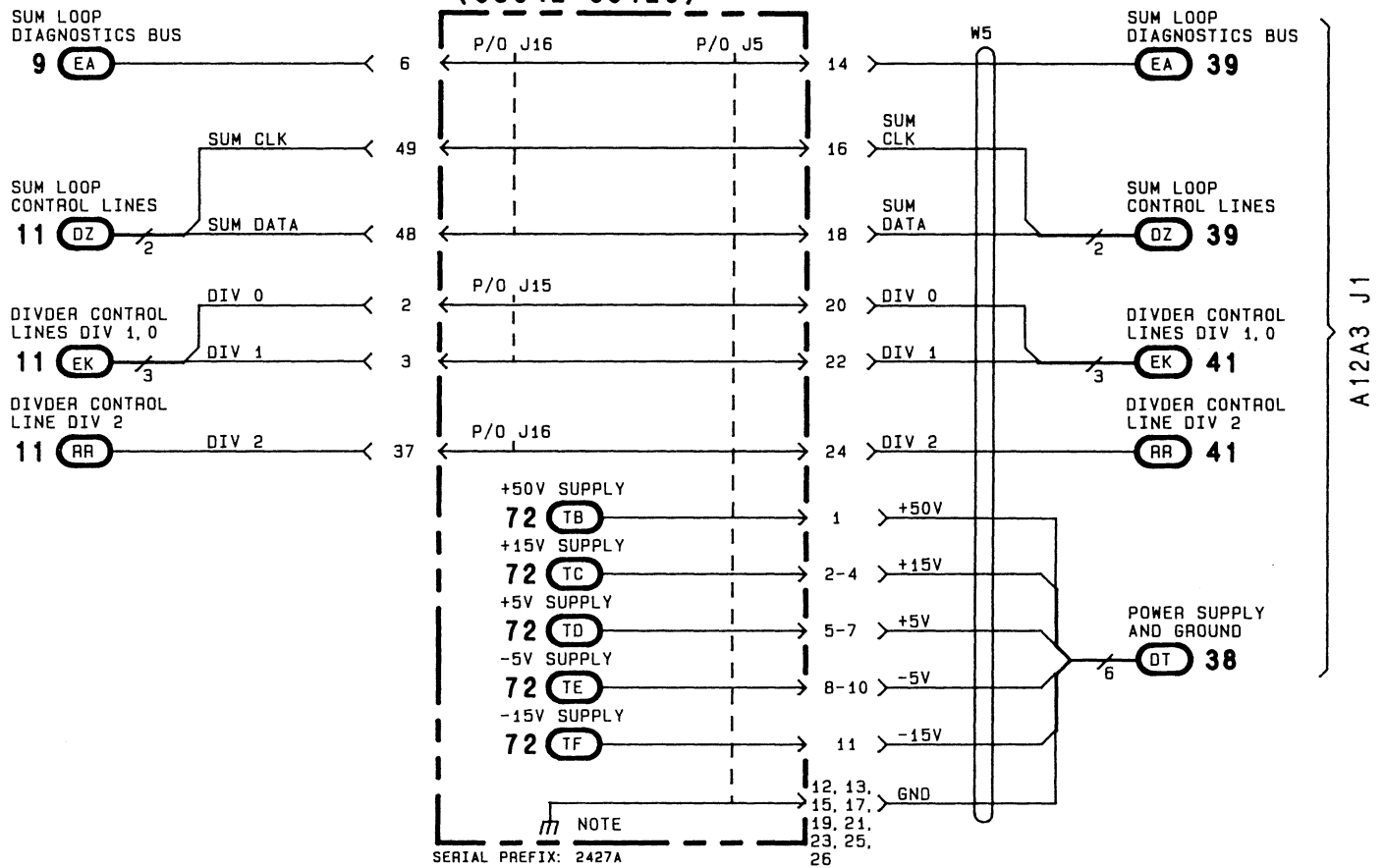
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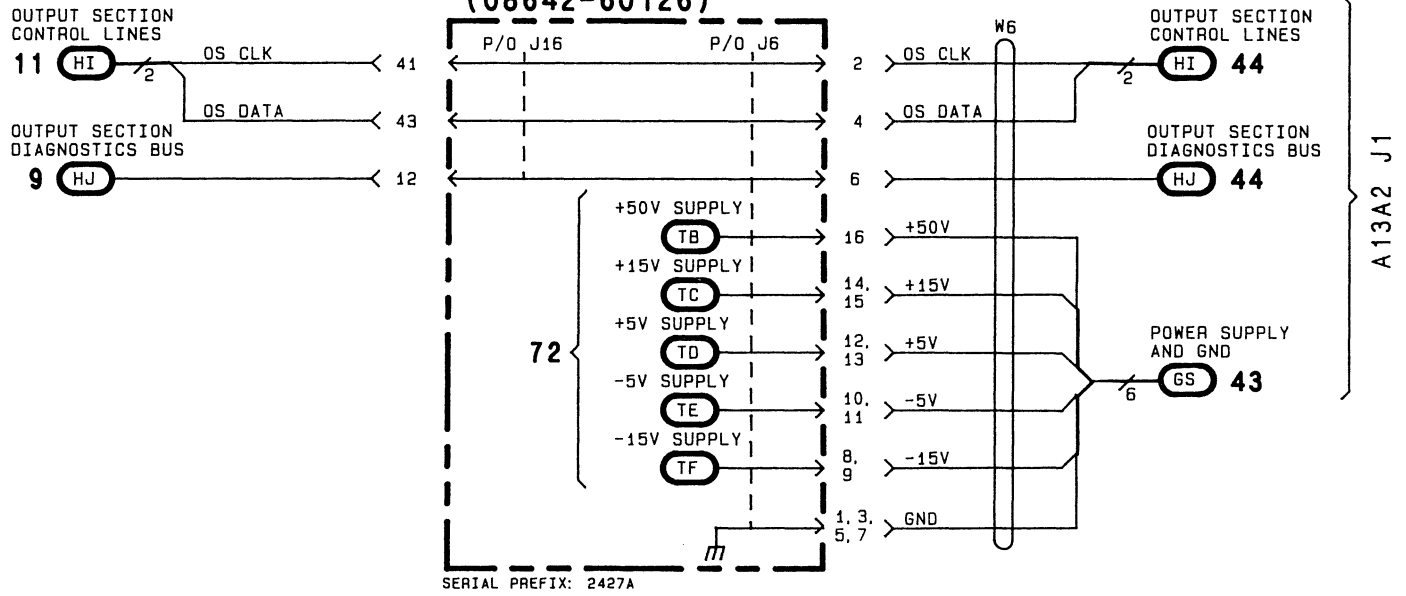
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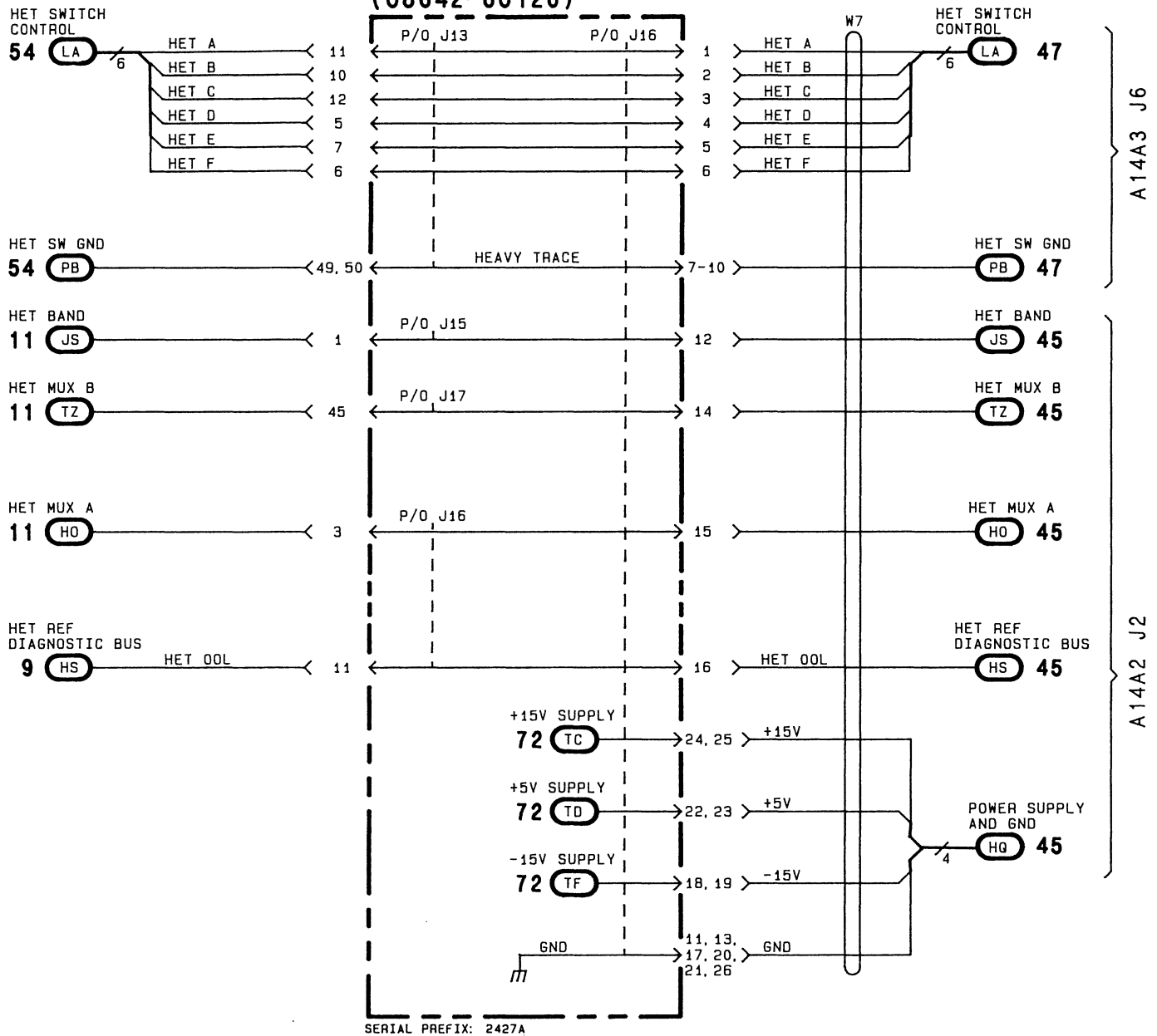
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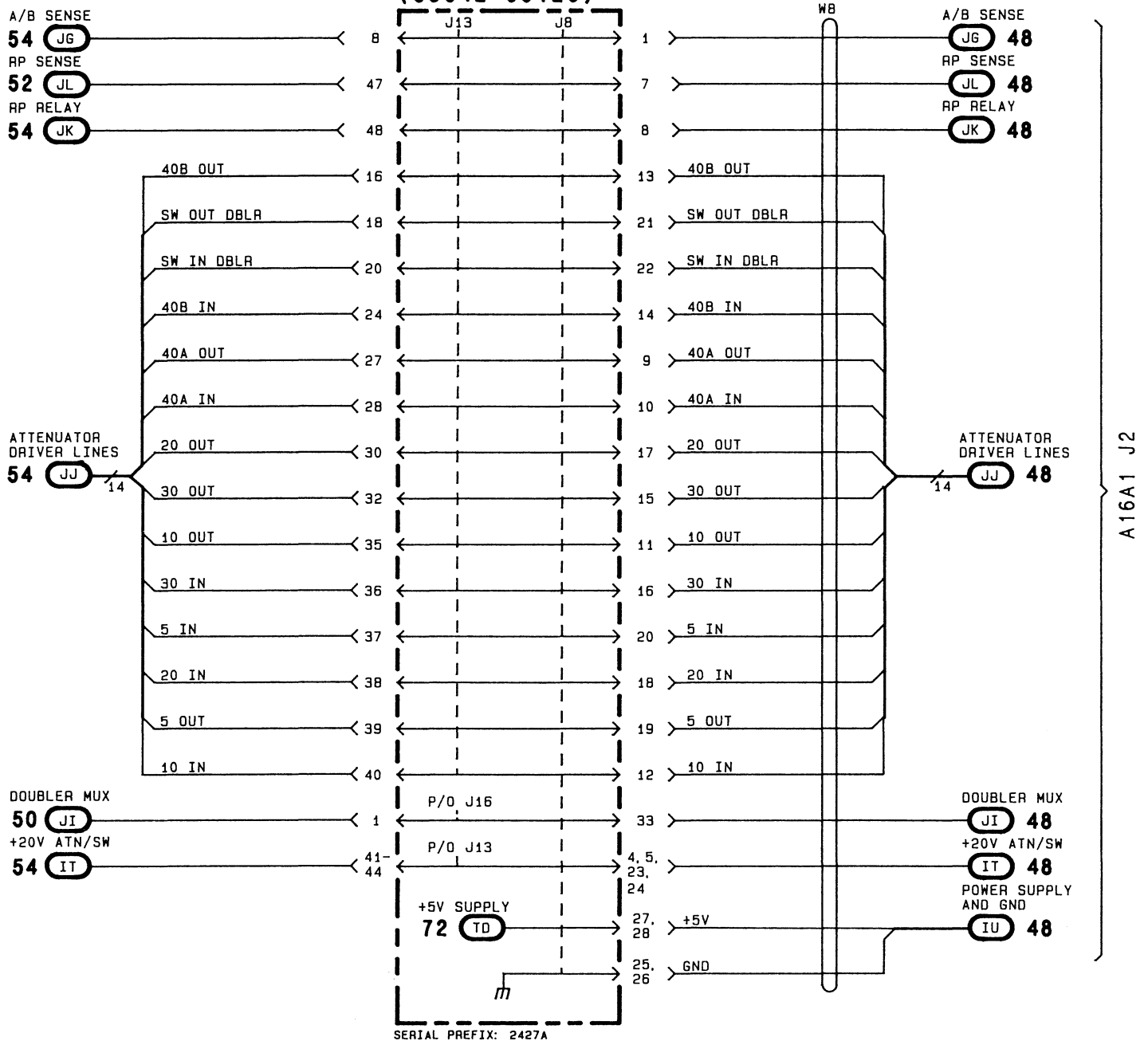
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Figure 8U-131
8U-131

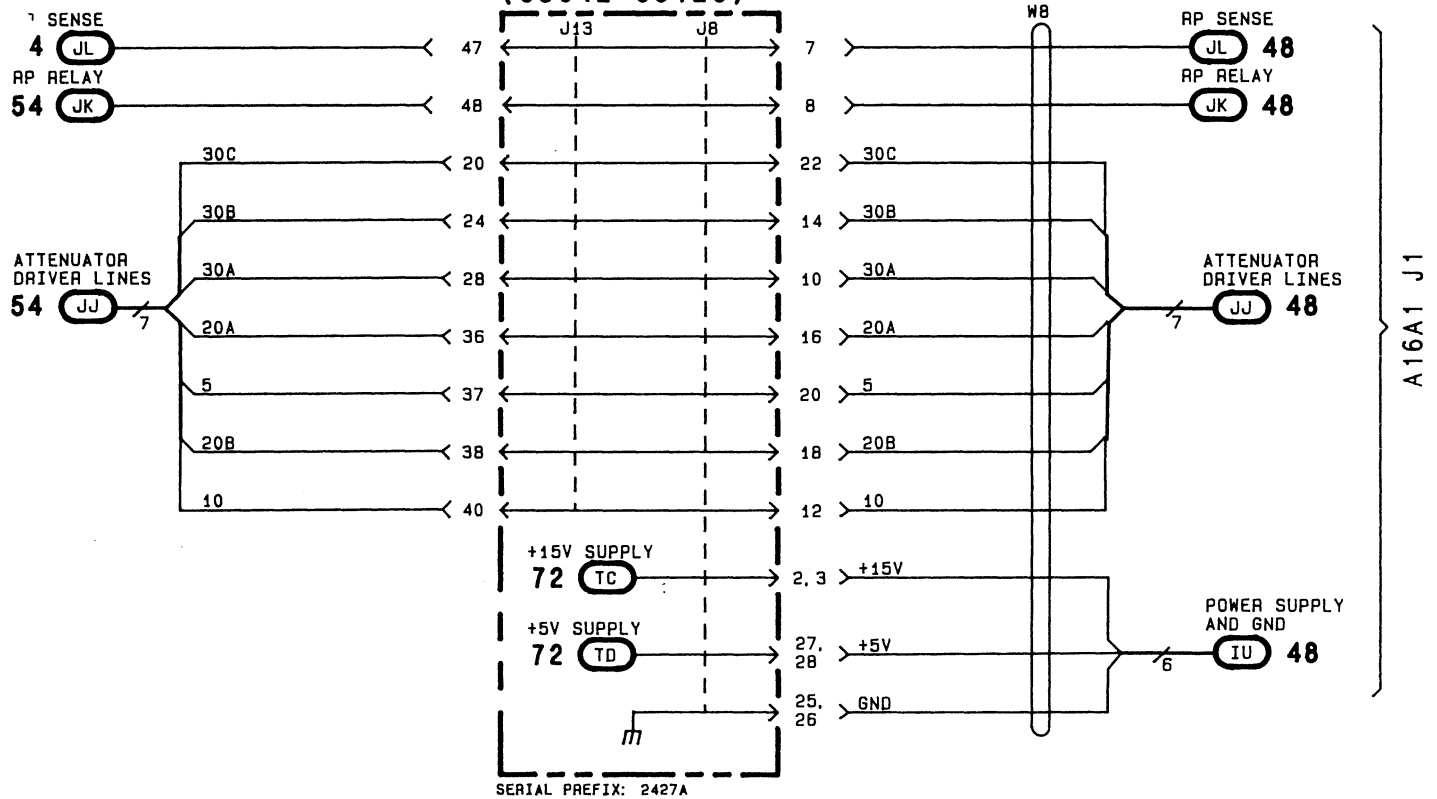
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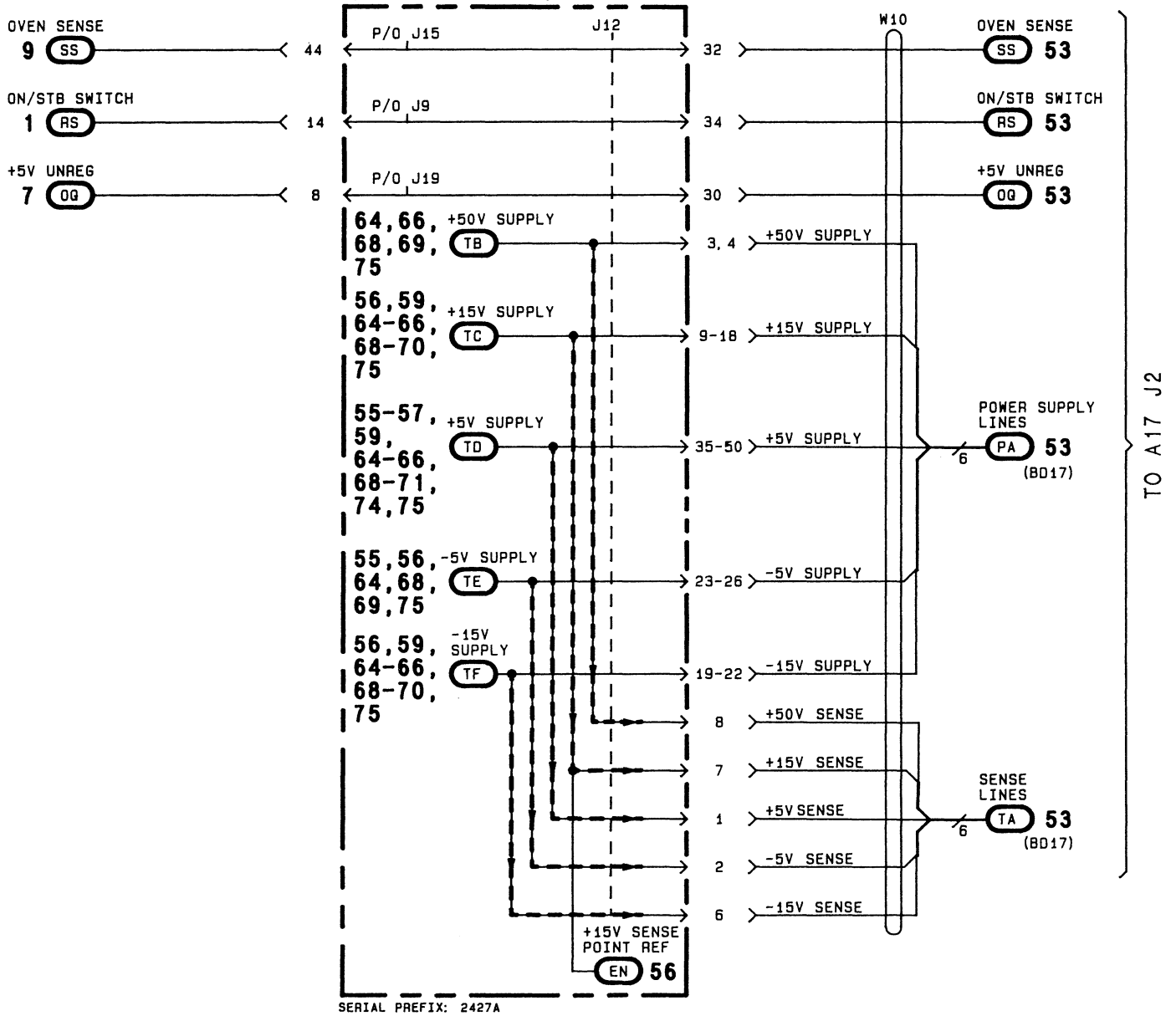


P/O A5 POWER SUPPLY/DIGITAL
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SS71
Figure 8U-133
8U-133.1

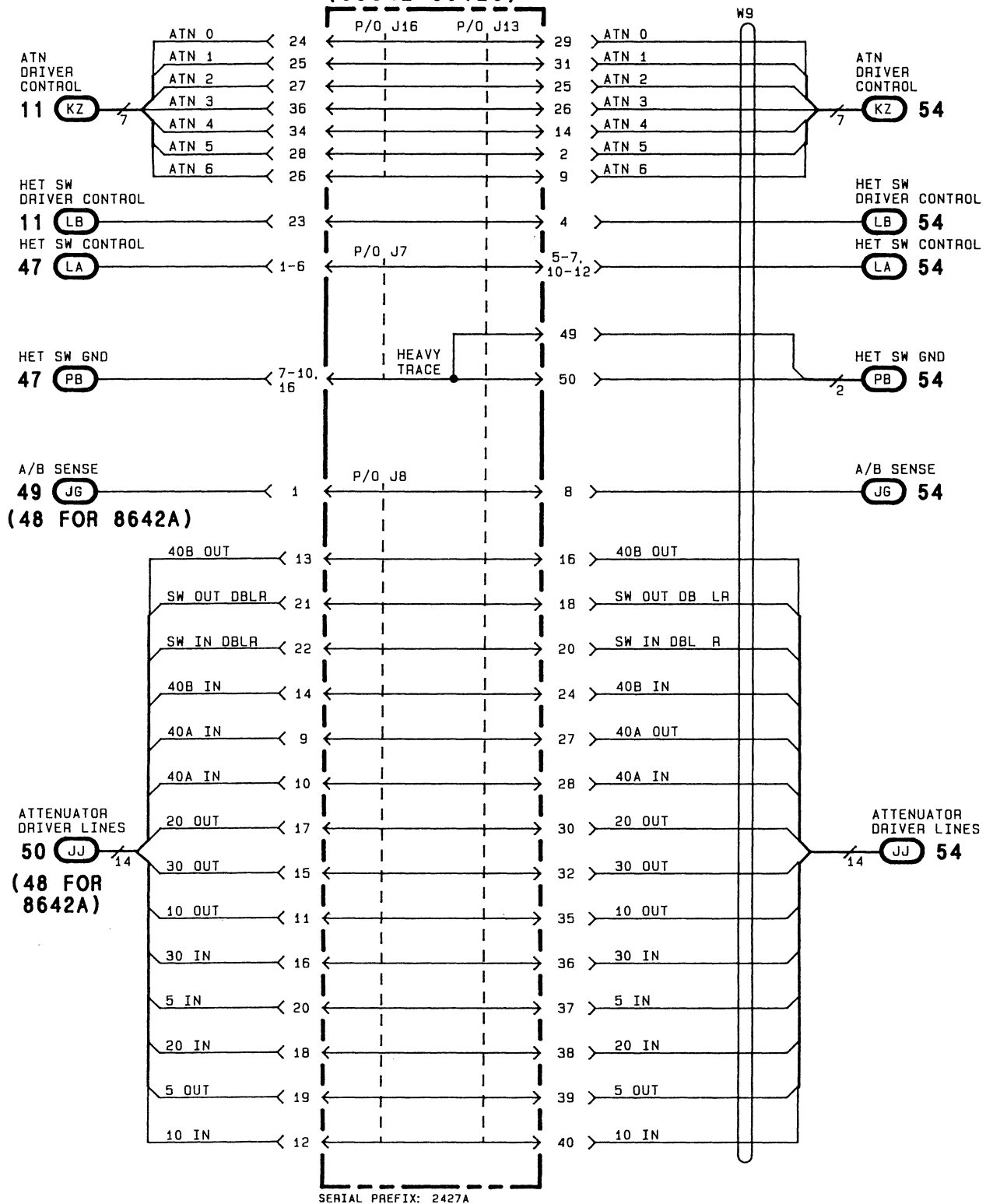
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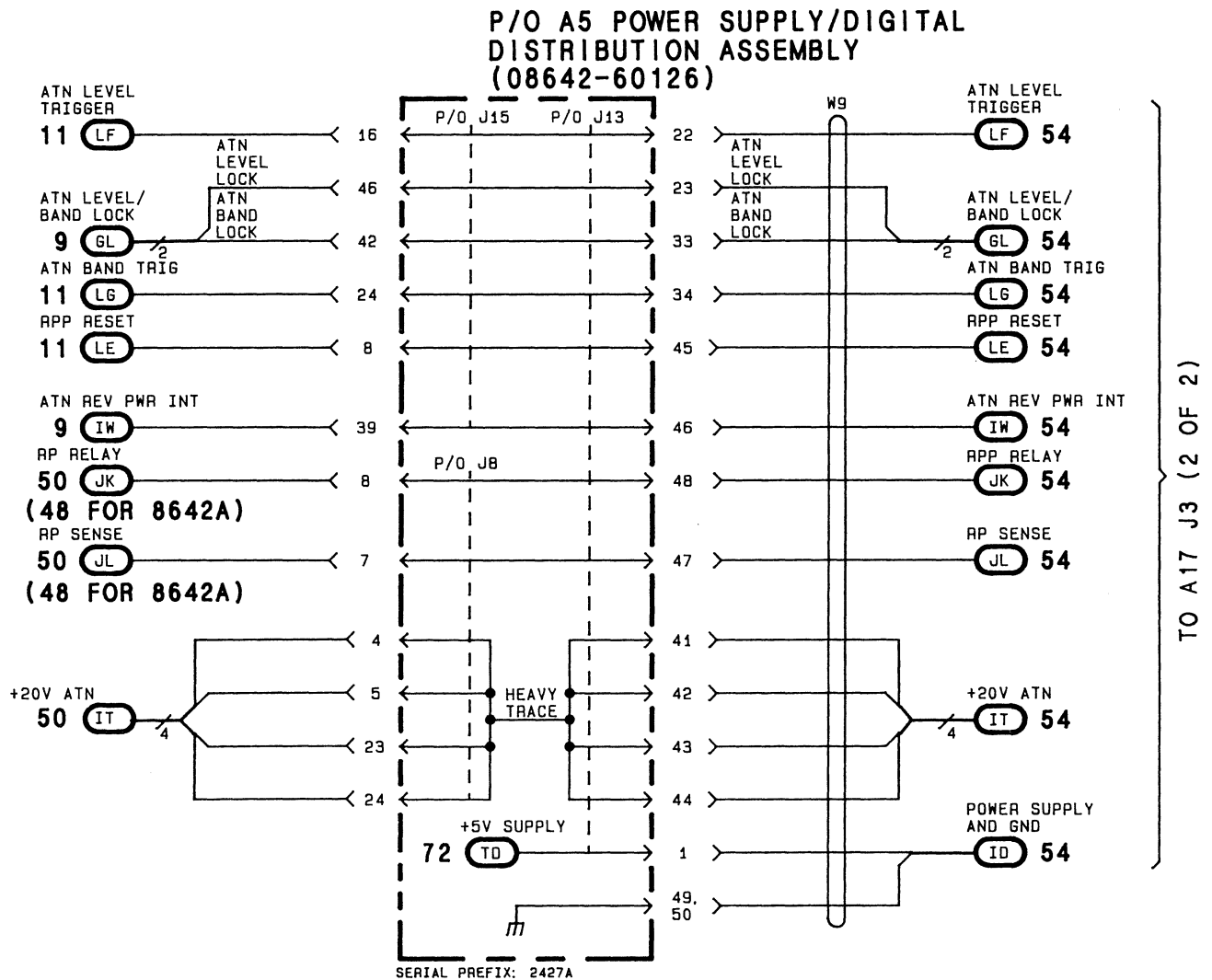


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Figure 8U-137
8U-137

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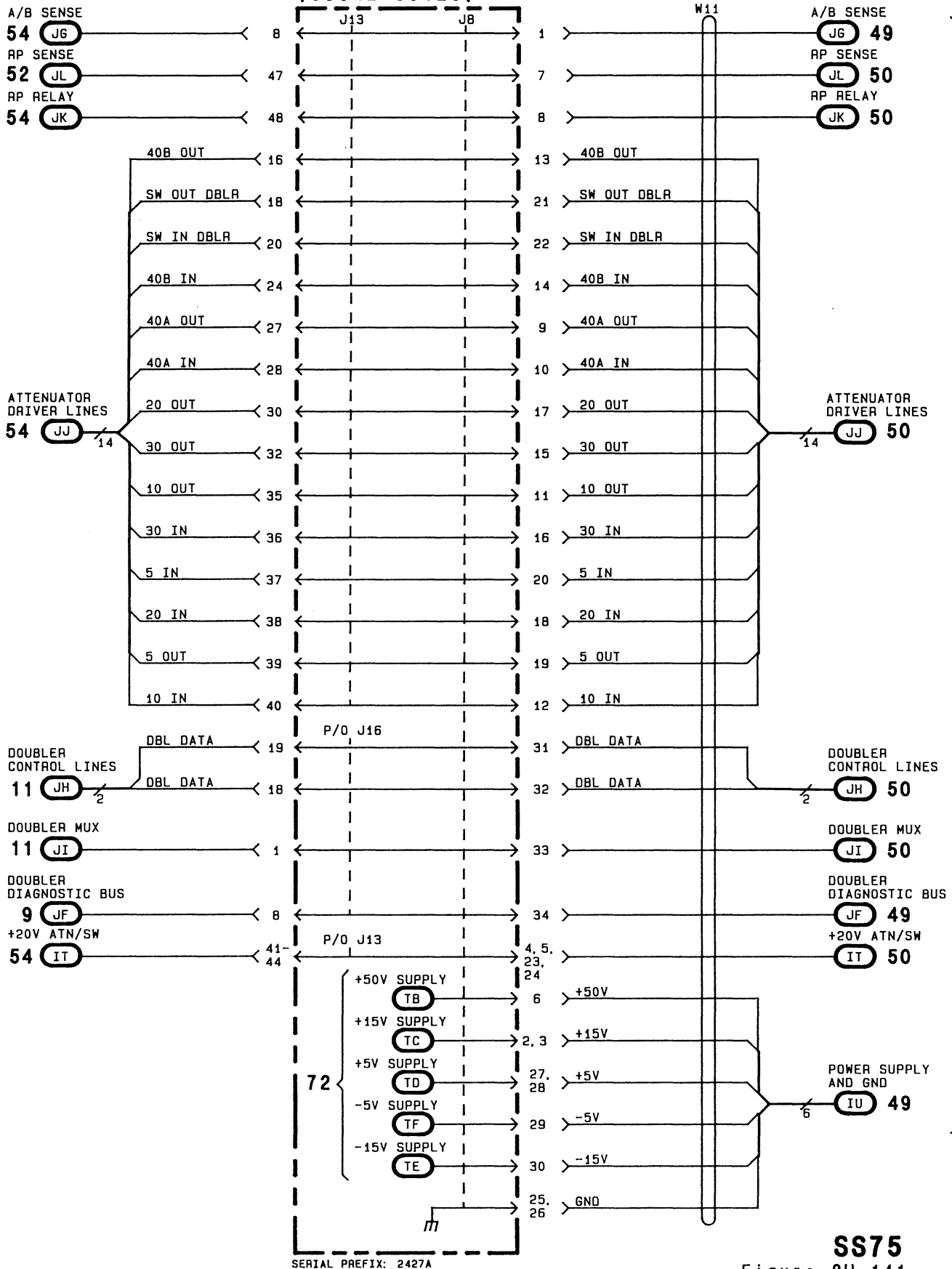


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Figure 8U-139
8U-139

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**P/O A5 POWER SUPPLY/DIGITAL
DISTRIBUTION ASSEMBLY
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TO A19A1J2

SS75

Figure 8U-141
8U-141